ACT I3

INTELLIGENT • INDUSTRIAL • INTERFACE

Application Note

AN-42

Version: 1.3
Date: 27.06.2023
Author: Achim Döbler

ACTRON

THE FACE OF YOUR PRODUCT

Contents

1 Introduction

This chapter outlines the industrial **ACT I³** display-standard, which has been defined and developed by ACTRON AG[1]. Key features of **ACT I³** are its standardized 50-pin interface, pin assignment and power supply. As a result, all **ACT I³** displays are fully interchangeable without any adjustment of the control hardware being necessary[2]. In addition to that, all **ACT I³**-displays have been highly optimized for ruggedized operation in harsh industrial environments and provide, therefore, excellent EMI-performance. Several low-impedance metal layers which are tightly connected to GND ensure superior shielding of all data lines. This measure does not only significantly reduce the amount of radiated electromagnetic energy, but also minimizes the overall susceptibility of the display to external electromagnetic noise. Low-impedance GND-reference has been achieved by 12 GND pins, which are tightly connected to all shielding layers. Furthermore, all typically inconvenient TFT-cell related voltages (e.g. VGH, VGL, VCOM) are directly generated on the tail. Moreover, the LED-backlight driver is included on the tail as well. This ensures correct LED driving conditions at all times. In addition to that, the customers don't have to develop or integrate their own LED driver. Therefore, the need of a constant current source on application side is completely eliminated. In order to particularly meet today's demanding industrial requirements, all **ACT I³** displays provide a typical luminance of 1000 cd/m^2 and a minimum lifetime of 50,000 hours at full brightness. Thus, **ACT I³** displays provide the following superior advantages over conventional solutions:

- ✓ Standardized pinout and interface
- ✓ Centered display tail
- ✓ Simple and convenient supply voltages
- ✓ Low-impedance GND-reference
- ✓ Highly EMI-optimized and EMI-shielded display design
- ✓ Automatic display detection supported
- ✓ Integrated LED backlight driver with wide supply range (5V-15V)
- ✓ Simple brightness control via PWM or digital command[3]
- ✓ Typical brightness of 1000 cd/m^2 at minimum 50,000 hours lifetime
- ✓ Guaranteed +10 years availability

[1] This document contains excerpts from the author's master's thesis "FPGA-based universal display tester", which was submitted to the Faculty of Electrical Engineering and Information Technology at the Munich University of Applied Sciences in 2016.

[2] Provided that all data lines are connected.

[3] Not available on all modules.

2 Display

In the following chapter, the **ACT I³** display interface and its associated timings are described in detail. Furthermore, some displays of this series also provide an interface for configuration purposes, which will also be covered.

2.1 Pinout

Table 1 outlines the standardized **ACT I³** pinout. Only two voltages are required: 3.3V to supply the analogue and digital parts of the display and 5V to 15V for the backlight driver. It is recommended to sufficiently filter both voltage rails on the application side with ceramic capacitors to ground[4].

PIN	NAME	FUNCTION
1	GND	Ground
2	VDD	Power supply for display (3.3V)
3	VDD	Power supply for display (3.3V)
4	VCC	Power supply for LED blacklight driver (5V - 15V)
5	VCC	Power supply for LED blacklight driver (5V - 15V)
6	PWM	Backlight driver PWM input (see section 2.4)
7	GND	Ground
8	R0	Data bit 0, red (LSB)
9	R1	Data bit 1, red
10	R2	Data bit 2, red
11	R3	Data bit 3, red
12	GND	Ground
13	R4	Data bit 4, red
14	R5	Data bit 5, red
15	R6	Data bit 6, red
16	R7	Data bit 7, red (MSB)
17	GND	Ground
18	G0	Data bit 0, green (LSB)
19	G1	Data bit 1, green
20	G2	Data bit 2, green
21	G3	Data bit 3, green
22	GND	Ground
23	G4	Data bit 4, green
24	G5	Data bit 5, green
25	G6	Data bit 6, green
26	G7	Data bit 7, green (MSB)

[4] e.g. 2.2μF X7R

27	GND	Ground
28	B0	Data bit 0, blue (LSB)
29	B1	Data bit 1, blue
30	B2	Data bit 2, blue
31	B3	Data bit 3, blue
32	GND	Ground
33	B4	Data bit 4, blue
34	B5	Data bit 5, blue
35	B6	Data bit 6, blue
36	B7	Data bit 7, blue (MSB)
37	GND	Ground
38	HS	Horizontal synchronization (line sync)
39	VS	Vertical synchronization (frame sync)
40	GND	Ground
41	DE	Data enable
42	GND	Ground
43	DCLK	Pixel clock
44	GND	Ground
45	CS	SPI chip select
46	SDIN	SPI MOSI
47	SCK	SPI clock
48	DISPLAY CONTROL	Display enable
49	RESET	Display reset
50	GND	Ground

Table 1: ACT I³ pinout

2.2 Image data interface

2.2.1 Fundamentals

All **ACT I³** displays use the display pixel interface (DPI), also known as TTL or RGB interface, for data transmission. The pixel data is transmitted in parallel, unidirectionally and synchronously. DPI is almost exclusively used for small- to medium-sized displays which do not provide a built-in framebuffer and thus generally require high data rates. The actual transmission of image data takes place as a linear, serial data stream consisting of individual pixels. Each pixel is transmitted in parallel, which means its color information is transferred as a parallel data word. Typical color depths are 8 to 24 bits. In addition to the pixel's color information, DPI also provides some control signals, which the display needs for internal synchronization. This includes a synchronization signal for new lines (horizontal synchronization) and one for new frames (vertical synchronization). Before and after visible image data, invisible areas consisting of black pixels are transmitted in horizontal as well as vertical direction. These areas are referred to as horizontal or vertical front- or back-

porch, depending on their position in the data stream and thus frame the visible image by an invisible black frame, the so-called blanking data. Some display controllers need the invisible blanking areas in order to regularly and at defined times adjust internal analogue components. Both the line and frame synchronization signals are also transmitted during the blanking, so that the display can be synchronized before the first visible pixel of a new frame. DPI also provides a data enable signal that indicates whether visible data or blanking data is being transmitted (Table 2).

DATA LINE	FUNCTION	REMARK
CLK, PCLK, DCLK	Pixel clock	-
HS, H-Sync, Line-Sync	Horizontal synchronization	Start of a new line
VS, V-Sync, Frame-Sync	Vertical synchronization	Start of a new frame
DE, Data-Enable, Data-Valid	Data or blanking	-
RGB[]	Parallel data lines	typ. 8,16,18 or 24

Table 2: Typical DPI data lines

A DPI transmission is defined by the number of data lines, eight time intervals, the pixel frequency and the polarity of all signal lines involved. Usually, all horizontal time intervals (THx) are specified as multiples of the pixel clock's period duration and all vertical time intervals (TVx) are specified as multiples of a single line duration (Table 3).

PARAMETER	FUNCTION	UNIT
f_{CLK}	Pixel clock frequency	Hz, $f_{CLK} = 1/T_{CLK}$
TH	Horizontal period	$\sum THx$
THS	H. sync pulse width	T_{CLK}
THB	H. back porch	T_{CLK}
THD	H. data (number of visible pixel in X direction)	T_{CLK}
THF	H. front porch	T_{CLK}
TV	Vertical period	$\sum TVx$
TVS	V. sync pulse width	TH
TVB	V. back porch	TH
TVD	V. data (number of visible lines)	TH
TVF	V. front porch	TH

Table 3: DPI timings

Figures 1 - 3 illustrate horizontal and vertical DPI timings.

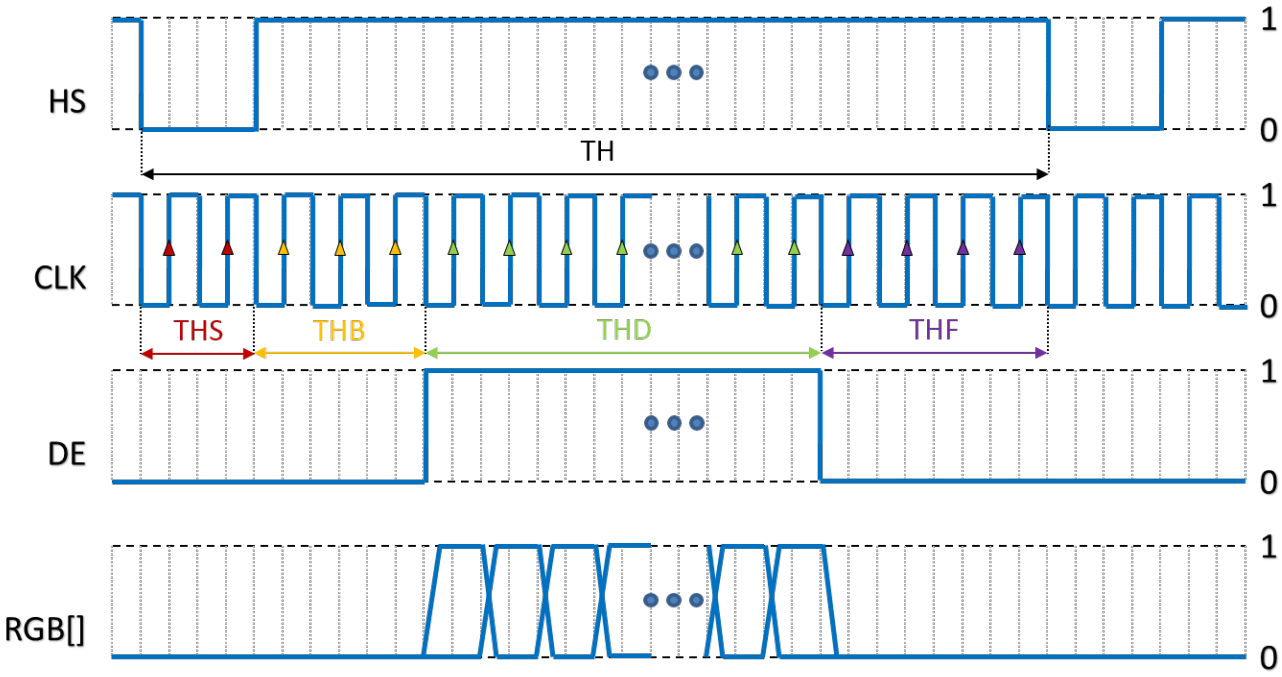

Figure 1: Horizontal DPI timings

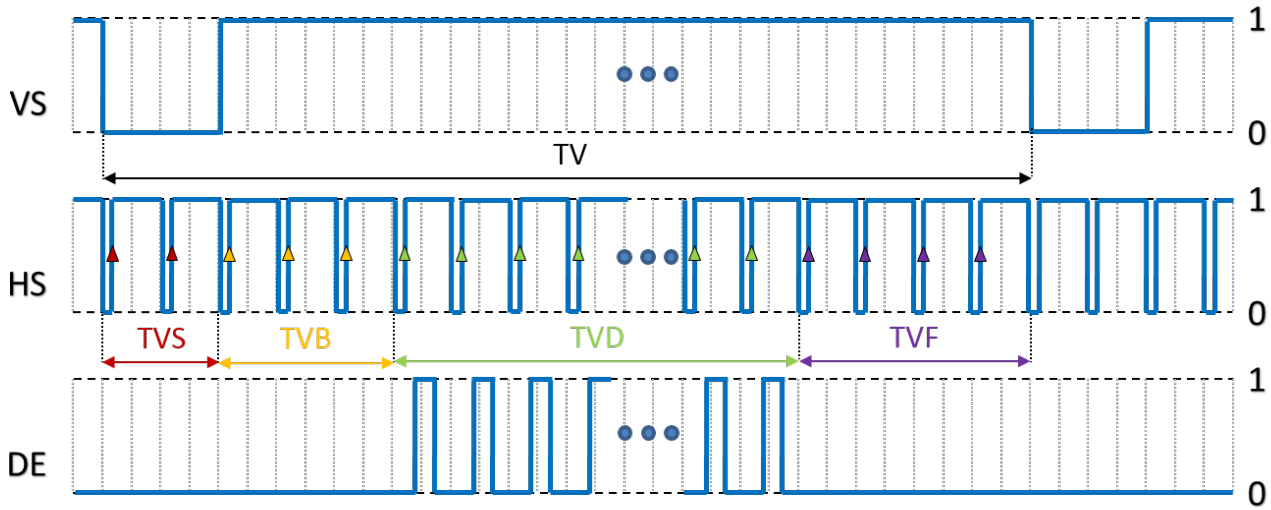

Figure 2: Vertical DPI timings

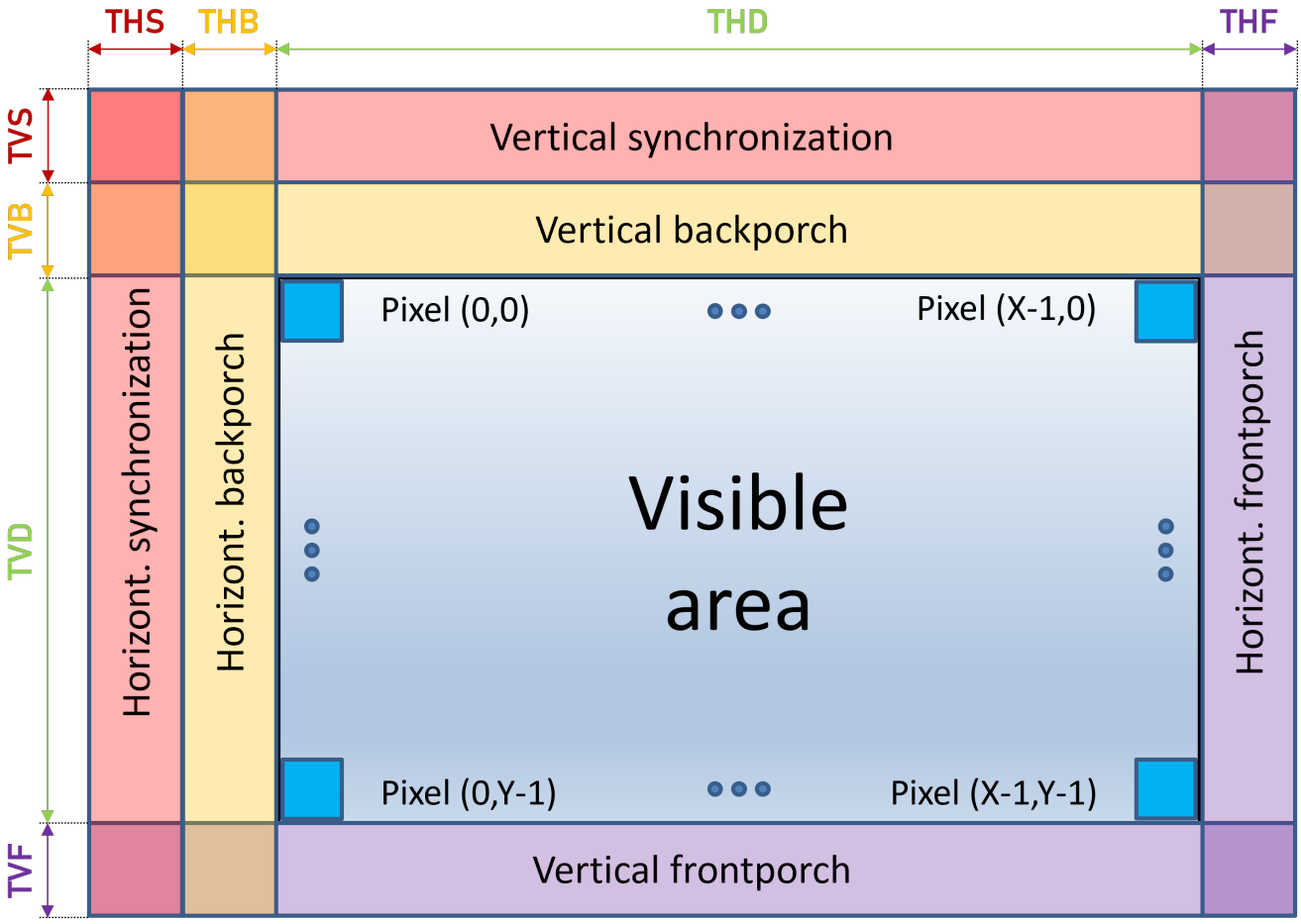

Figure 3: DPI timings

The following example highlights how to calculate the necessary DPI-display data throughput, which needs to be provided by the target platform. This example is based on the timings of a standard 4.3" 480x272 TFT-LCD.

The period duration T_{PCLK} of one pixel is calculated as follows:

Calculating the duration of one pixel

$$T_{PCLK} := \frac{1}{f_{PCLK}} \tag{1}$$

$$T_{PCLK_{4.3\text{" TFT-LCD}}} = \frac{1}{15\ \text{MHz}} = \underline{\underline{66.\overline{6}\ \text{ns}}} \tag{2}$$

The calculated duration of one pixel can then be used to determine the total duration of a single line (TH) as the sum of all horizontal time intervals:

Total duration of a single line

$$TH := THS + THB + THD + THF \tag{3}$$

$$TH_{4.3\text{" TFT-LCD}} = (41 + 2 + 480 + 2) \cdot T_{PCLK} = \underline{\underline{35\ \mu s}} \tag{4}$$

Now the duration of a complete frame (TV) and also the refresh rate (=frame rate) can be calculated as follows:

Duration of a complete frame

$$TV := TVS + TVB + TVD + TVF \tag{5}$$

$$TV_{4.3\text{" TFT-LCD}} = (10 + 2 + 272 + 2) \cdot TH = \underline{\underline{10,01\ ms}} \tag{6}$$

$$Framerate_{4.3\text{" TFT-LCD}} := \frac{1}{TV} = \frac{1}{10,01\ ms} = 99,9Hz \approx \underline{\underline{100\ Hz}} \tag{7}$$

Based on above calculated refresh rate of approx. 100 Hz, the required data throughput (including blanking) by the 4.3" display can be derived accordingly. This data throughput must be provided **continuously**, even if the image content is to remain constant:

Necessary data throughput

$$Throughput_{DPI} := f_{PCLK} \cdot dim\{RGB[]\} \cdot \text{ Bit} \tag{8}$$

$$Throughput_{4.3\text{" TFT-LCD}} = 15\text{ MHz} \cdot 24\text{ Bit} = \underline{\underline{45\text{ MByte/s}}} \tag{9}$$

Given an uncompressed transmission of image data, this approximately corresponds to the maximum data rate of USB 2.0[5] and highlights the necessary hardware performance required by DPI.

[5] Assuming an average USB 2.0 overhead of 20% and a data rate of 480 MBit/s. This results in a maximum average data rate of approx. $0.8 \cdot 480\text{MBit/s} \cdot \frac{1byte}{8bit} = 48\text{MByte/s}$.

During blanking periods, the target platform does not have to provide any data from its frame buffer (=image memory), but applies a logical 0 to all data lines and thus only transmits black pixels. This slightly reduces the effective data rate, i.e. the average data rate of the frame buffer (also known as *GRAM*). The symbol η indicates the ratio between the visible area and the entire transmitted image data including blanking. It ranges between 0 and 1. The actual value depends both on the display used as well as on its configuration. The smaller the value, the greater the proportion of blanking in the transmitted image data, and the lower the effective data rate for image transmission. If the value is exactly 1, the display has no blanking areas. A theoretically possible value 0 does not exist in practice, as this would mean the display either not having any visible area or showing only a black image.

Ratio between visible and entire display data

$$\eta := \frac{f_{GRAM}}{f_{PCLK}} = \frac{THD}{TH} \cdot \frac{TVD}{TV} \tag{10}$$

$$\eta_{\text{4.3" TFT-LCD}} = \frac{480}{525} \cdot \frac{272}{286} = 0,87 = \underline{\underline{87\%}} \tag{11}$$

Since many displays allow a wide blanking range, even at a given pixel frequency the data rate for image transmission and thus the average readout frequency of the frame buffer can be reduced by approx. 20%-30%. Of course, this only applies to the primary frame buffer, e.g. the SDRAM, and not to the cache. Although blanking causes a read-transmission pause, the cache must still be capable of providing image data at full pixel frequency.

Effective data rate of a display

$$Datenrate_{GRAM} := Datenrate_{DPI} \cdot \eta \tag{12}$$

2.2.2 Timings

Tables 4 - 7 show typical timings of different **ACT I³** display sizes. All given parameters have been explained in chapter 2.2.1. Parameter limits are subject to each individual display and can be obtained from the corresponding module specification.

Parameter	PURE	PRO	PRO X	Remark
f_{CLK}	8.0 MHz	8.0 MHz	8.0 MHz	$f_{CLK} = 1/T_{CLK}$
TH	408	373	373	$\sum THx$
THS	34	21	21	$N \cdot T_{CLK}$
THB	34	22	22	$N \cdot T_{CLK}$
THSB	68	43	43	$= THS + THB$
THD	320	320	320	$N \cdot T_{CLK}$
THF	20	10	10	$N \cdot T_{CLK}$
TV	262	254	254	$\sum TVx$
TVS	9	6	6	$N \cdot TH$
TVB	9	6	6	$N \cdot TH$
TVSB	18	12	12	$= TVS + TVB$
TVD	240	240	240	$N \cdot TH$
TVF	4	2	2	$N \cdot TH$
PCLK pol.	↑	↓	↓	Display latch edge
HS pol.	AL	AL	AL	AL=active low, AH=active high
VS pol.	AL	AL	AL	AL=active low, AH=active high
DE pol.	AL	AH	AH	AL=active low, AH=active high
DE mode	✓	✓	✓	only DE signal connected
Sync mode	✓	✓	✓	only HS/VS signal connected
DE+Sync mode	✓	✓	✓	DE, HS and VS signal connected

Table 4: ACT I³ 3.5" display timings

Parameter	PURE	PRO	PRO X	Remark
f_{CLK}	10.0 MHz	10.0 MHz	10.0 MHz	$f_{CLK} = 1/T_{CLK}$
TH	533	533	533	$\sum THx$
THS	21	21	21	$N \cdot T_{CLK}$
THB	22	22	22	$N \cdot T_{CLK}$
THSB	43	43	43	$= THS + THB$
THD	480	480	480	$N \cdot T_{CLK}$
THF	10	10	10	$N \cdot T_{CLK}$
TV	286	286	286	$\sum TVx$
TVS	6	6	6	$N \cdot TH$
TVB	6	6	6	$N \cdot TH$
TVSB	12	12	12	$= TVS + TVB$
TVD	272	272	272	$N \cdot TH$
TVF	2	2	2	$N \cdot TH$
PCLK pol.	↓	↓	↓	Display latch edge
HS pol.	AL	AL	AL	AL=active low, AH=active high
VS pol.	AL	AL	AL	AL=active low, AH=active high
DE pol.	AH	AH	AH	AL=active low, AH=active high
DE mode	✓	✓	✓	only DE signal connected
Sync mode	✗	✓	✓	only HS/VS signal connected
DE+Sync mode	✓	✓	✓	DE, HS and VS signal connected

Table 5: ACT I^3 4.3" display timings

Parameter	PURE	PRO	PRO X	Remark
f_{CLK}	27.0 MHz	27.0 MHz	27.0 MHz	$f_{CLK} = 1/T_{CLK}$
TH	862	816	816	$\sum THx$
THS	23	4	4	$N \cdot T_{CLK}$
THB	23	4	4	$N \cdot T_{CLK}$
THSB	46	8	8	$= THS + THB$
THD	800	800	800	$N \cdot T_{CLK}$
THF	16	8	8	$N \cdot T_{CLK}$
TV	513	496	496	$\sum TVx$
TVS	11	4	4	$N \cdot TH$
TVB	12	4	4	$N \cdot TH$
TVSB	23	8	8	$= TVS + TVB$
TVD	480	480	480	$N \cdot TH$
TVF	10	8	8	$N \cdot TH$
PCLK pol.	↓	↓	↓	Display latch edge
HS pol.	AL	AL	AL	AL=active low, AH=active high
VS pol.	AL	AL	AL	AL=active low, AH=active high
DE pol.	AH	AH	AH	AL=active low, AH=active high
DE mode	✓	✓	✓	only DE signal connected
Sync mode	✗	✓	✓	only HS/VS signal connected
DE+Sync mode	✓	✓	✓	DE, HS and VS signal connected

Table 6: ACT I^3 5.0" display timings

Parameter	PURE	PRO	PRO X	Remark
f_{CLK}	27.0 MHz		27.0 MHz	$f_{CLK} = 1/T_{CLK}$
TH	866		866	$\sum THx$
THS	23		23	$N \cdot T_{CLK}$
THB	23		23	$N \cdot T_{CLK}$
THSB	46		46	$= THS + THB$
THD	800		800	$N \cdot T_{CLK}$
THF	20		20	$N \cdot T_{CLK}$
TV	513		513	$\sum TVx$
TVS	11		11	$N \cdot TH$
TVB	12		12	$N \cdot TH$
TVSB	23		23	$= TVS + TVB$
TVD	480		480	$N \cdot TH$
TVF	10		10	$N \cdot TH$
PCLK pol.	↓		↑	Display latch edge
HS pol.	AL		AL	AL=active low, AH=active high
VS pol.	AL		AL	AL=active low, AH=active high
DE pol.	AH		AH	AL=active low, AH=active high
DE mode	✓		✓	only DE signal connected
Sync mode	✗		✓[a]	only HS/VS signal connected
DE+Sync mode	✓		✓	DE, HS and VS signal connected

Table 7: ACT I³ 7.0" display timings

[a] Prior configuration via SPI necessary

2.3 Configuration interface

Many **ACT I³** displays can be configured via a *serial peripherial interface* (SPI). SPI is a synchronous serial interface originally developed by Motorola[6]. There is no official SPI specification, hence many variations of this interface exist. In general, the device to be communicated with, in this case the display, is selected by the master via a so-called *chip select line* (CS) or *slave select line* (SS). Then data is transmitted serially and synchronously to a clock line (usually SCLK or SCK). The transmitted data usually contains multiple packets consisting of 8 bits each. Depending on whether the transmission is uni- or bidirectional, one or two data lines are required[7]. The data lines are usually referred to as *serial data in* (SDI) and *serial data out* (SDO) (table 8). However, since these signal names can easily lead to confusion regarding signal direction, the terms *master out slave in* (MOSI) and *master in slave out* (MISO) are also becoming more common, where the display is to be considered as a slave. As with many ICs (e.g. ADCs) a distinction must be made between the transmission of user data (image data or payload) and commands (e.g. for initialization). Essentially, one of the following methods is used for this purpose:

- Insertion of a preamble
- Use of an additional data line D/C for indicating data or command transmissions
- Encoding the D/C information in an additional (e.g. ninth) bit
- Fixed partitioning of the data frame: e.g. 1 byte for commands and 3 bytes for data

Displays with SPI are predominantly used in unidirectional communication, since reading back data is only required in very few applications (e.g. for XOR or Read-Modify-Write operations or display module identification). Therefore, depending on whether a D/C line is used, a display usually requires 3 or 4 data lines for SPI configuration. However, many displays support more than one of the above methods to distinguish between command- and data-packets, which is why data sheets can offer 3-*wire* and 4-*wire* SPI modes. It should be emphasized here that these terms exclusively imply presence (4-*wire*) or absence (3-*wire*) of a D/C line, and not, as often mistakenly assumed, whether a uni- or bidirectional SPI is used.

Signal	Function	Remark
CS, nCS, $\overline{\text{CS}}$, SS	select device	not always needed
SCLK, SCK	clock line	-
SDO, MOSI	serial data out	-
SDI, MISO	serial data in	-
D/C	indicate command or data transmission	not always needed

Table 8: Typical SPI data lines

[6]source: https://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus
[7]In rare cases, a single bidirectional data line is used instead

Principle write operation procedure (Fig. 4):

1. First, **D/C** is used to signal whether a command or user data is being transmitted.
2. The desired recipient is selected via **nCS**.
3. The first data bit is applied.
4. The transmitter passes the data bit along with a rising or falling **SCK** edge depending on the configuration. Then steps 3 and 4 are repeated n times.
5. Finally, the receiver is deselected.

Since **ACT I³** uses SPI exclusively for configuration purposes and not for transferring image data **ACT I³**-displays don't provide an internal frame buffer, no D/C line is required. Step 1 can be omitted.

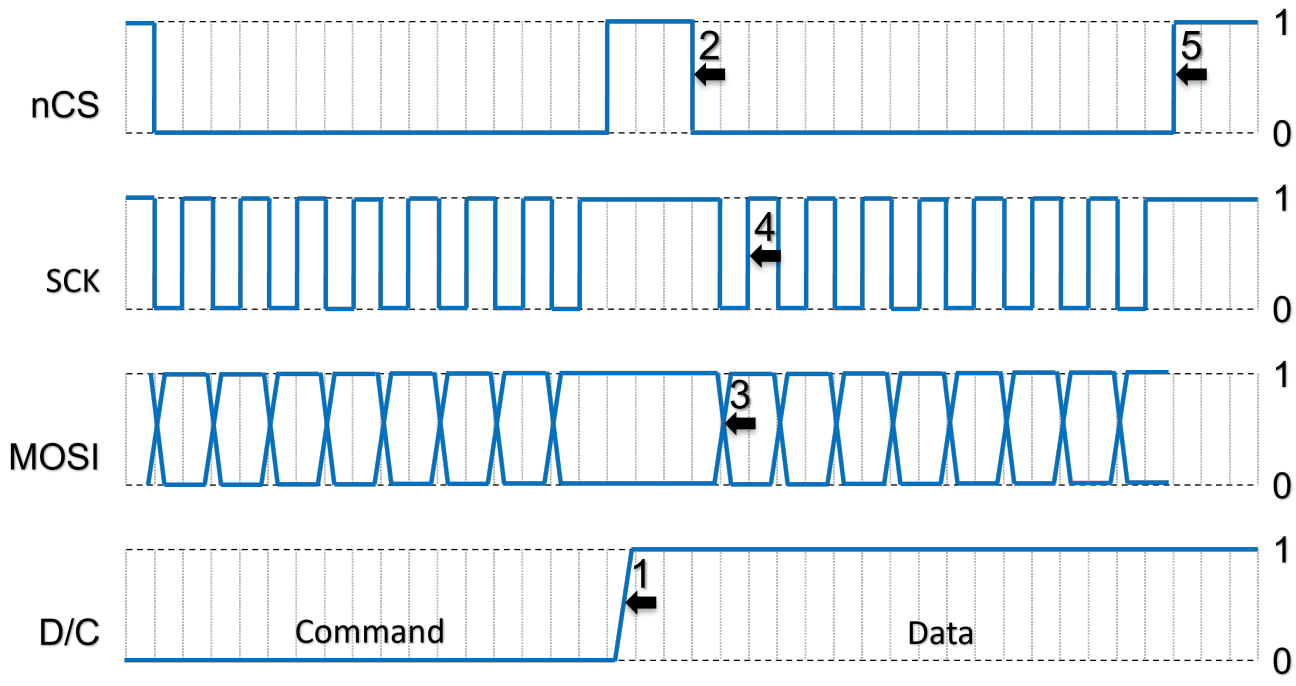

Figure 4: SPI write operation example

Advantages:

- Very simple interface that can be easily implemented with any microcontroller or emulated by software
- Only a few data lines
- Simple bus analysis possible

Disadvantages:

- Low data rates (approx. 1 - 20 MBit/s)
- Overhead[8] possible.

2.4 LED-Backlight

All **ACT I³** displays come with an integrated LED backlight driver which has a wide input voltage range of 5V to 15V. This significantly simplifies the control of the displays. The backlight constant current driver is located directly underneath the display's flex tail shielding. Therefore, electromagnetic interference usually caused by high switching frequencies of LED drivers is also reduced to a minimum.

3 Touch

3.1 I²C

The I²C bus (*inter-integrated circuit*) was originally developed by the company Philips in 1982. This bus is based on a detailed specification, so there are no fundamental variations, as for example with SPI. For licensing reasons, some manufacturers use the alternative name *two wire interface* (TWI). The I²C data transmission is bidirectional, serial and synchronous. Two data lines (table 9) are always needed: *serial clock* (SCL) and *serial data* (SDA).

Signal	Function	Remark
SCL	clock line	open-collector output
SDA	data line	open-collector output

Table 9: Typical I²C data lines

Both data lines are never actively driven high, but only via pull-up resistors. All bus participants, which are divided into master(s) and slave(s)[9], may only use open-collector outputs. This prevents the devices from driving against each other. In addition, I²C works according to the principle of the so-called *carrier sense multiple access/collision avoidance* (CSMA/CA). Before sending data, each master checks whether the bus is currently available. If this is not the case, the station aborts the transmission and attempts again later. I²C communication is based primarily on the following rules:

- Each I²C transmission basically consists of a multiple of 9 bits, because after each transmitted byte a so-called *acknowledge bit* is transmitted, by which the receiver confirms the received data byte.

[8] The term *overhead* refers to data that is transmitted in addition to the user payload data. This data is required by some buses and used for data flow control, addressing or error correction

[9] Each I²C bus requires at least one master and one slave. Usually a master is used in a combination with several slaves

- In *idle-state* both lines are pulled to a logic 1 via the pull-up resistors. All devices connected to the bus switch their open-collector outputs to high impedance.
- The clock line signal is generated by the master[10].
- Data line state may only change while SCL is low[11].
- A data transmission can only be initiated by a master.
- If SCL is high, a falling edge on SDA triggers the so-called *start signal* and thus indicates a transmission start.
- If SCL is high, a rising edge on SDA triggers the so-called *stop signal* and thus indicates a transmission end.

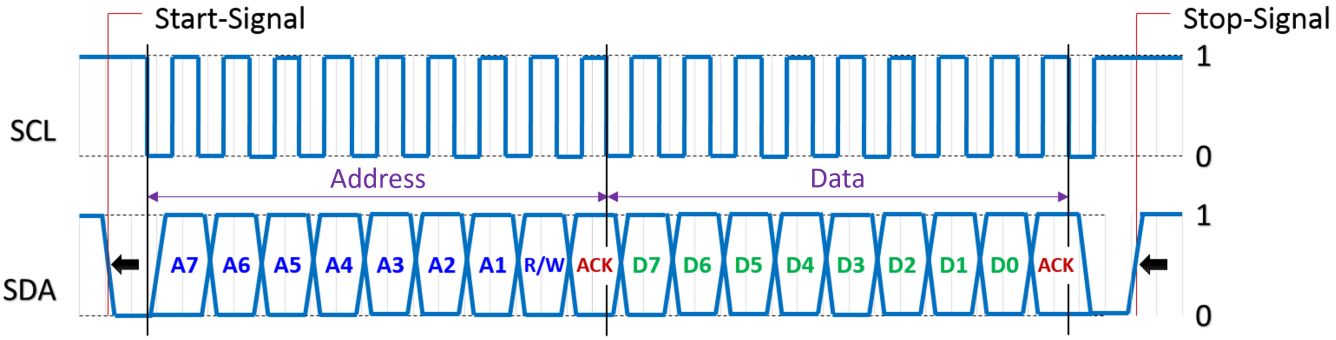

Figure 5: Timing of an I²C interface

Principle sequence of an I²C data transmission (Fig. 6 and 7):

1. The master issues a start signal. All devices recognize this signal and wait for the address to be received.
2. The master transmits the 7-bit address[12] of the slave to be addressed.
3. Then the master sends the R/W bit that indicates whether it wants to send or receive data (0=send, 1=receive).
4. When the address is received, the addressed slave acknowledges by pulling SDA low.
5. Depending on the transmitted R/W bit, either the master or slave now sends one or more data bytes.
6. After the last byte and its acknowledge signal, the master terminates the transmission with a stop signal and thus releases the I²C bus.

[10] The slave can force a reduction of the data rate via so-called *clock stretching*
[11] exceptions are the start and stop signal
[12] I²C also supports a 10-bit address, which is not covered in this document

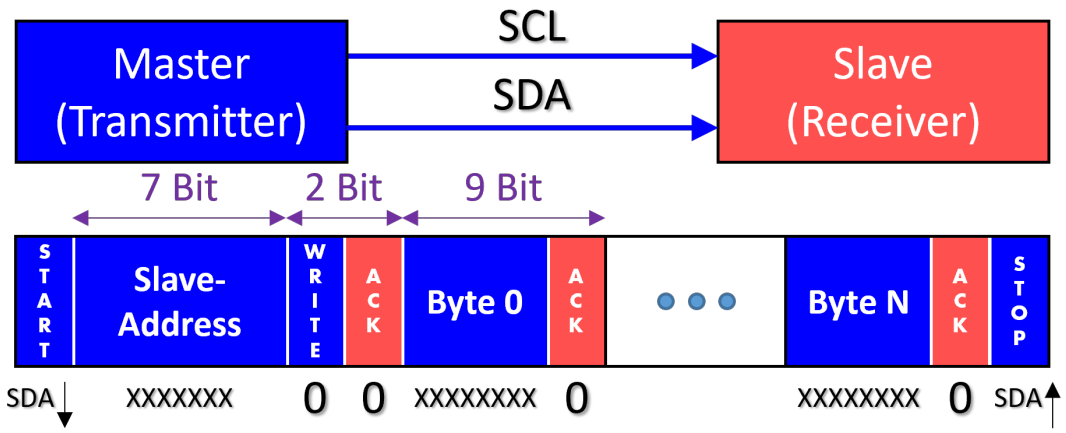

Figure 6: Master to slave I²C-transfer sequence

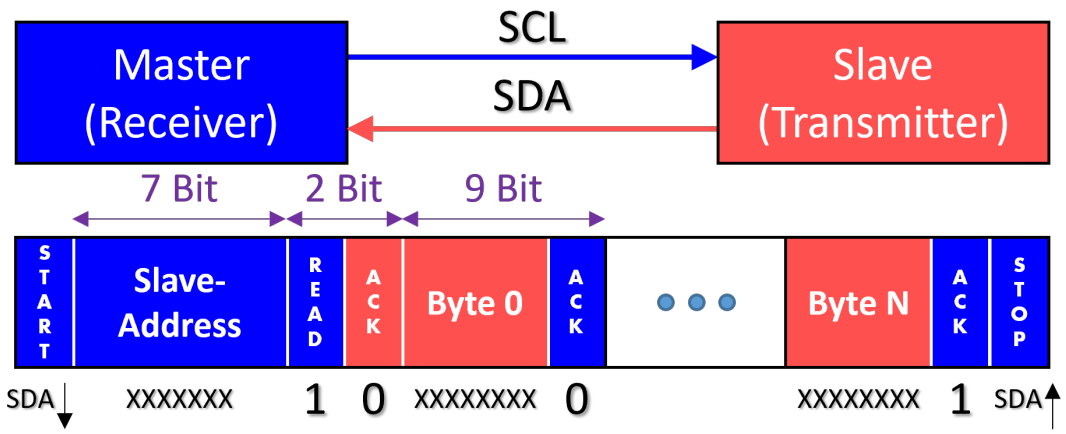

Figure 7: Slave to master I²C-transfer sequence

Advantages:

- Well specified bus
- Only two data lines regardless of the number of devices
- Easy bus analysis possible

Disadvantages:

- Very low data rates (approx. 0.1 - 1 MBit/s)
- Bus requires overhead

List of Figures

List of Tables

Version	Date	Remark
v1.3	27.06.2023	▪ Corrected 7” ProX PCLK polarity in table 7 to rising edge.
v1.2	05.02.2023	▪ Changed document language to English. ▪ Updated document. ▪ Added **ACT I³** Pro- and ProX-Series.
v1.1	25.11.2016	▪ Correction of a few errors.
v1.0	24.11.2016	▪ First release. ▪ Documentation created using LaTeX.