EXAMINED BY : Kevin Kuo	EMERGING DISPLAY TECHNOLOGIES CORPORATION	FILE NO . CAS-0008808
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		VERSION : 3

CUSTOMER ACCEPTANCE SPECIFICATIONS

MODEL NO. :

ET028013DMA

(RoHS)

FOR MESSRS :

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CUSTOMER'S APPROVAL

DATE :

_____

BY :

_____

RECORDS OF REVISION

DOC . FIRST ISSUE

APR.25, 2019

DATE	REVISED PAGE NO.	SUMMARY
SEP.02, 2019	2	3.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	MIN.	MAX.	UNIT	REMARK
POWER SUPPLY VOLTAGE FOR DIGITAL	IOVCC-VSSD	-0.3	4.6	V	
POWER SUPPLY VOLTAGE FOR ANALOG	VCC-VSSA	-0.3	4.6	V	
INPUT VOLTAGE	VIN	-0.3	IOVCC+0.5	V	
LED BACKLIGHT POWER DISSIPATION	PLED	—	396	mW	
LED BACKLIGHT FORWARD CURRENT	ILED	—	120	mA	

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ITEM	SYMBOL	MIN.	MAX.	UNIT	REMARK
POWER SUPPLY VOLTAGE FOR ANALOG	VCC-VSSA	-0.3	4.6	V	
POWER SUPPLY VOLTAGE FOR DIGITAL	VDD-VSSD	-0.3	4.6	V	
POWER DISSIPATION FOR LED BACKLIGHT	PD	—	396	mW	
FORWARD CURRENT FOR LED BACKLIGHT	ILED	—	120	mA	

NOTE (1) : LCM SHOULD BE GROUNDED DURING HANDLING LCM→ LCM SHOULD BE GROUNDED DURING LCM HANDLING

3.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

ITEM	REMARK
VIBRATION	5~20Hz, 1HR 20~500Hz(20Hz), 1HR 20~500Hz(500Hz), 1HR X, Y, Z, TOTAL 3HR
SHOCK	10 ms XYZ DIRECTIONS 1 TIME EACH

→

ITEM	REMARK
VIBRATION	10~100 Hz XYZ DIRECTIONS 1 HR EACH
SHOCK	10 ms XYZ DIRECTIONS 1 TIME EACH

	3	4. ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
INPUT POWER SUPPLY	VCC-VSSA	OPERATION VOLTAGE	2.4	2.8	3.3	V	
INTERFACE OPERATION VOLTAGE	IOVCC-VSSD	I/O SUPPLY VOLTAGE	1.65	2.8	3.3	V	
INPUT CURRENT	I_{CC}	—	—	9	15	mA	NOTE (1)
INPUT VOLTAGE	V_{IH}	H LEVEL	0.7*I_{OVCC}	—	I_{OVCC}	V	
	V_{IL}	L LEVEL	VSSD	—	0.3* I_{OVCC}	V	
OUTPUT VOLTAGE	V_{OH}	I_{OH}=-1.0mA	0.8* I_{OVCC}	—	I_{OVCC}	V	
	V_{OL}	I_{OL}=1.0mA	VSSD	—	0.2* I_{OVCC}	V	
POWER SUPPLY FOR LED BACKLIGHT	A-K	ILED=80mA	2.8	3.1	3.4	V	NOTE (2)
LED LIFE TIME	—	IF=20mA (PER.LED)	30K	—	—	hrs	NOTE (3) NOTE (4)

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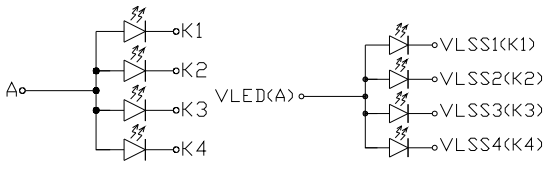
ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
POWER SUPPLY VOLTAGE FOR ANALOG	VCC-VSSA	OPERATION VOLTAGE	2.4	2.8	3.3	V	
POWER SUPPLY VOLTAGE FOR DIGITAL	VDD-VSSD	I/O SUPPLY VOLTAGE	1.65	2.8	3.3	V	
POWER SUPPLY CURRENT	ICC+IDD	VCC=VDD=2.8V	—	9	15	mA	
LOGIC HIGH INPUT VOLTAGE	V_{IH}	H LEVEL	0.7*VDD	—	VDD	V	NOTE (1)
LOGIC LOW INPUT VOLTAGE	V_{IL}	L LEVEL	VSSD	—	0.3* VDD	V	NOTE (1)
LOGIC HIGH OUTPUT VOLTAGE	V_{OH}	I_{OH}=-1.0mA	0.8* VDD	—	VDD	V	
LOGIC LOW OUTPUT VOLTAGE	V_{OL}	I_{OL}=1.0mA	VSSD	—	0.2* VDD	V	
POWER SUPPLY VOLTAGE FOR LED BACKLIGHT	VLED-VLSS	ILED=80mA	2.8	3.1	3.4	V	NOTE (2)
LED LIFE TIME	—	IF=20mA (PER LED)	30K	—	—	HRS	NOTE (3) NOTE (4)

NOTE (1) : $I_{CC}=I_{IOVCC}+I_{VCC}$→APPLIED TO TERMINALS, RESX, D0~D17, SDA, RDX, WRX, DCX, CSX, TE

NOTE (2) :



RECORDS OF REVISION

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APR.25, 2019

DATE	REVISED PAGE NO.	SUMMARY
SEP.02, 2019	5~9	5.1 8080 SERIES MCU PARALLEL INTERFACE CHARACTERISTICS: 18/16/9/8-BIT BUS & 5.2 SERIAL INTERFACE CHARACTERISTICS (3-LINE SERIAL) & 5.3 SERIAL INTERFACE CHARACTERISTICS (4-LINE SERIAL) & 5.4 RGB INTERFACE CHARACTERISTICS & 5.5 RESET TIMING IOVCC→VDD
	10,11	ADD 5.6 POWER ON/OFF SEQUENCE
	12,13	6. OPTICAL CHARACTERISTICS NOTE (2)→ 6. OPTICAL CHARACTERISTICS DELETE 6.1 OPTICAL CHARACTERISTICS
	15	8. BLOCK DIMENSION
	17,18	10.1 LCD MODULE CONNECTOR IOVCC→VDD PIN NO.17~34: FUNCTION: -IF NOT USED, PLEASE FIX THIS PIN AT VDDI OR DGND → -CONNECTED UNUSED PINS TO THE VSSD LEVEL
	19	11.1 POWER SUPPLY FOR LCM IOVCC→VDD
	20	12. INSPECTION CRITERION→12. INSPECTION CRITERIA RESPECTS→RESPECT
	27	13.1 STANDARD SPECIFICATIONS FOR RELIABILITY OF LCD MODULE ADD NOTE (1)
		13.2 TESTING CONDITIONS AND INSPECTION CRITERIA FOR THE FINAL TEST THE TESTING SAMPLE MUST BE STORED AT ROOM TEMPERATURE FOR 24 HOURS, STANDARD SPECIFICATIONS FOR RELIABILITY HAVE BEEN EXECUTED IN ORDER TO ENSURE STABILITY. →FOR THE FINAL TEST THE TESTING SAMPLE MUST BE STORED AT ROOM EMPERATURE FOR 24 HOURS, AFTER THE TESTS LISTED IN TABLE 13.1, STANDARD SPECIFICATIONS FOR RELIABILITY HAVE BEEN EXECUTED IN ORDER TO ENSURE STABILITY.

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
COLOR CHROMATICITY (CENTER)	WHITE	Wy	θx = 0° θy = 0° ILED=80mA NTSC：60%	0.27	0.32	0.37	—	NOTE (5)
	RED	Rx		0.58	0.63	0.68	—

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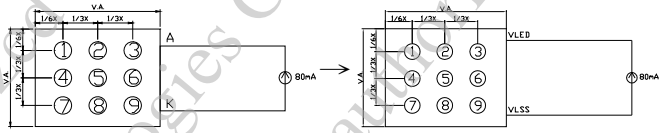
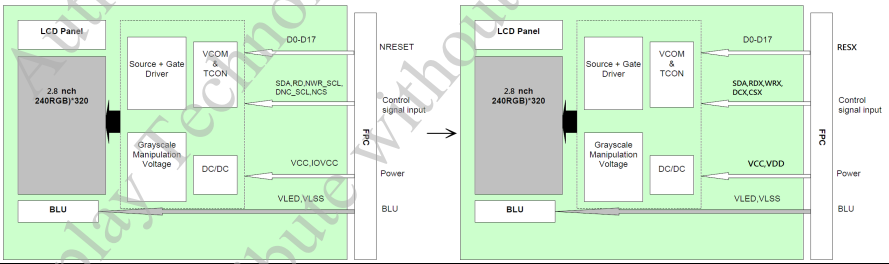
ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
COLOR CHROMATICITY (CENTER)	WHITE	Wy	θx = 0°, θy = 0° VDD-VSSD=2.8V VCC-VSSA=2.8V ILED=80mA NTSC：60%	0.26	0.31	0.36	—	NOTE (5)
	RED	Rx		0.58	0.62	0.68	—

NOTE (7)：(a)DEFINITION OF BRIGHTNESS UNIFORMITY





RECORDS OF REVISION

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APR.25, 2019

DATE	REVISED PAGE NO.	SUMMARY
OCT.28, 2019	12	6. OPTICAL CHARACTERISTICS

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
COLOR CHROMATICITY (CENTER)	RED	Rx	θx = 0°, θy = 0° VDD-VSSD=2.8V VCC-VSSA=2.8V ILED=80mA NTSC：60%	0.58	0.62	0.68	—	NOTE (5)

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ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
COLOR CHROMATICITY (CENTER)	RED	Rx	θx = 0°, θy = 0° VDD-VSSD=2.8V VCC-VSSA=2.8V ILED=80mA NTSC：60%	0.57	0.62	0.67	—	NOTE (5)

TABLE OF CONTENTS

1. GENERAL SPECIFICATIONS

1.1 DATA SHEETS FOR CONTROLLER/DRIVER
PLEASE REFER TO :

SITRONIX ST7789V2

1.2 MATERIAL SAFETY DESCRIPTION
ASSEMBLIES SHALL COMPLY WITH EUROPEAN ROHS REQUIREMENTS, INCLUDING PROHIBITED MATERIALS/COMPONENTS CONTAINING LEAD, MERCURY, CADMIUM, HEXAVALENT CHROMIUM, POLYBROMINATED BIPHENYLS (PBB) AND POLYBROMINATED
DIPHENYL ETHERS (PBDE), BIS(2-ETHYLHEXYL) PHTHALATE (DEHP), BUTYL BENZYL PHTHALATE (BBP), DIBUTYL PHTHALATE (DBP), DIISOBUTYL PHTHALATE (DIBP).

2. MECHANICAL SPECIFICATIONS

(1) DIAGONALS	2.8 inch
(2) NUMBER OF DOTS	240W * (RGB) * 320H DOTS
(3) MODULE SIZE	50W * 69.2H * 2.9D mm (NOT INCLUDED FPC)
(4) VIEWING AREA	44.8W * 59.2H mm
(5) ACTIVE AREA	43.2W * 57.6H mm
(6) DOT SIZE	0.06W * 0.18H mm
(7) PIXEL SIZE	0.18W * 0.18H mm
(8) LCD TYPE	TFT , TRANSMISSIVE, NORMALLY BLACK
(9) COLOR	262K (18BIT)
(10) VIEWING DIRECTION	SUPER WIDE VIEW
(11) BACK LIGHT	LED , COLOR : WHITE
(12) INTERFACE MODE	RGB : 16/18 BIT MCU : 8/16/18 BIT PARALLEL DATA SPI DATA

3. ABSOLUTE MAXIMUM RATINGS

3.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	MIN.	MAX.	UNIT	REMARK
POWER SUPPLY VOLTAGE FOR ANALOG	VCC-VSSA	-0.3	4.6	V	
POWER SUPPLY VOLTAGE FOR DIGITAL	VDD-VSSD	-0.3	4.6	V	
STATIC ELECTRICITY	—	—	—	V	NOTE (1)
POWER DISSIPATION FOR LED BACKLIGHT	PD	—	396	mW	
FORWARD CURRENT FOR LED BACKLIGHT	ILED	—	120	mA	

NOTE (1)：LCM SHOULD BE GROUNDED DURING LCM HANDLING.

3.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

ITEM	OPERATING		STORAGE		REMARK
	MIN.	MAX.	MIN.	MAX.	
AMBIENT TEMPERATURE	-20°C	70°C	-30°C	80°C	NOTE (1), (2)
HUMIDITY	—	—	—	—	WITHOUT CONDENSATION NOTE (3)
VIBRATION	—	2.45m/S^2 (0.25G)	—	11.76m/S^2 (1.2 G)	10~100 Hz XYZ DIRECTIONS 1 HR EACH
SHOCK	—	29.4 m/S^2 (3G)	—	490m/S^2 (50 G)	10 ms XYZ DIRECTIONS 1 TIME EACH
CORROSIVE GAS	NOT ACCEPTABLE		NOT ACCEPTABLE		

NOTE (1)：Ta AT -30°C：48HR MAX.
80°C：168HR MAX.
NOTE (2)：BACKGROUND COLOR CHANGES SLIGHTLY DEPENDING ON AMBIENT TEMPERATURE THIS PHENOMENON IS REVERSIBLE.
NOTE (3)：Ta ≤ 60°C：90%RH (96HRS MAX .)
Ta > 60°C：ABSOLUTE HUMIDITY MUST BE LOWER THAN THE HUMIDITY OF 90%RH AT 60°C. (96 HRS MAX.)

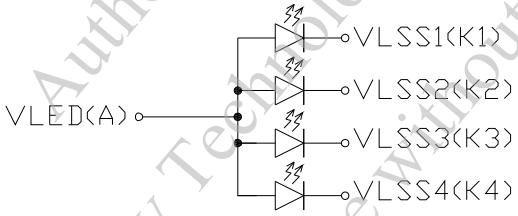
4. ELECTRICAL CHARACTERISTICS

Ta = 25 °C

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
POWER SUPPLY VOLTAGE FOR ANALOG	VCC-VSSA	OPERATION VOLTAGE	2.4	2.8	3.3	V	
POWER SUPPLY VOLTAGE FOR DIGITAL	VDD-VSSD	I/O SUPPLY VOLTAGE	1.65	2.8	3.3	V	
POWER SUPPLY CURRENT	ICC+IDD	VCC=VDD=2.8V	—	9	15	mA	
LOGIC HIGH INPUT VOLTAGE	V_{IH}	H LEVEL	0.7*VDD	—	VDD	V	NOTE (1)
LOGIC LOW INPUT VOLTAGE	V_{IL}	L LEVEL	VSSD	—	0.3* VDD	V	NOTE (1)
LOGIC HIGH OUTPUT VOLTAGE	V_{OH}	I_{OH}=-1.0mA	0.8* VDD	—	VDD	V	
LOGIC LOW OUTPUT VOLTAGE	V_{OL}	I_{OL}=1.0mA	VSSD	—	0.2* VDD	V	
POWER SUPPLY VOLTAGE FOR LED BACKLIGHT	VLED-VLSS	ILED=80mA	2.8	3.1	3.4	V	NOTE (2)
LED LIFE TIME	—	IF=20mA (PER LED)	30K	—	—	HRS	NOTE (3) NOTE (4)

NOTE (1)：APPLIED TO TERMINALS, RESX, D0~D17, SDA, RDX, WRX, DCX, CSX, TE.

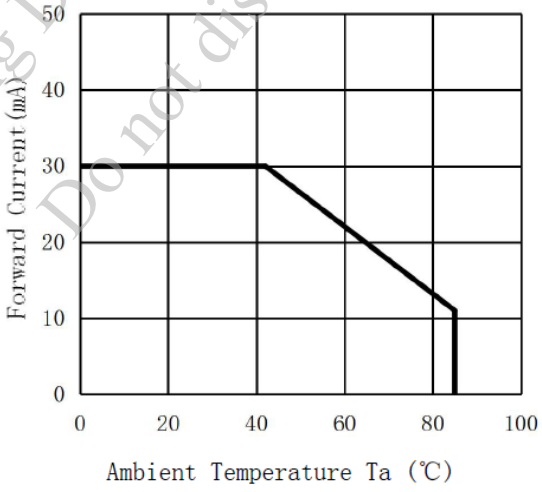
NOTE (2)：INTERNAL CIRCUIT DIAGRAM OF BACKLIGHT



NOTE (3)：CONDITIONS, TA=25°C, CONTINUOUS LIGHTING.

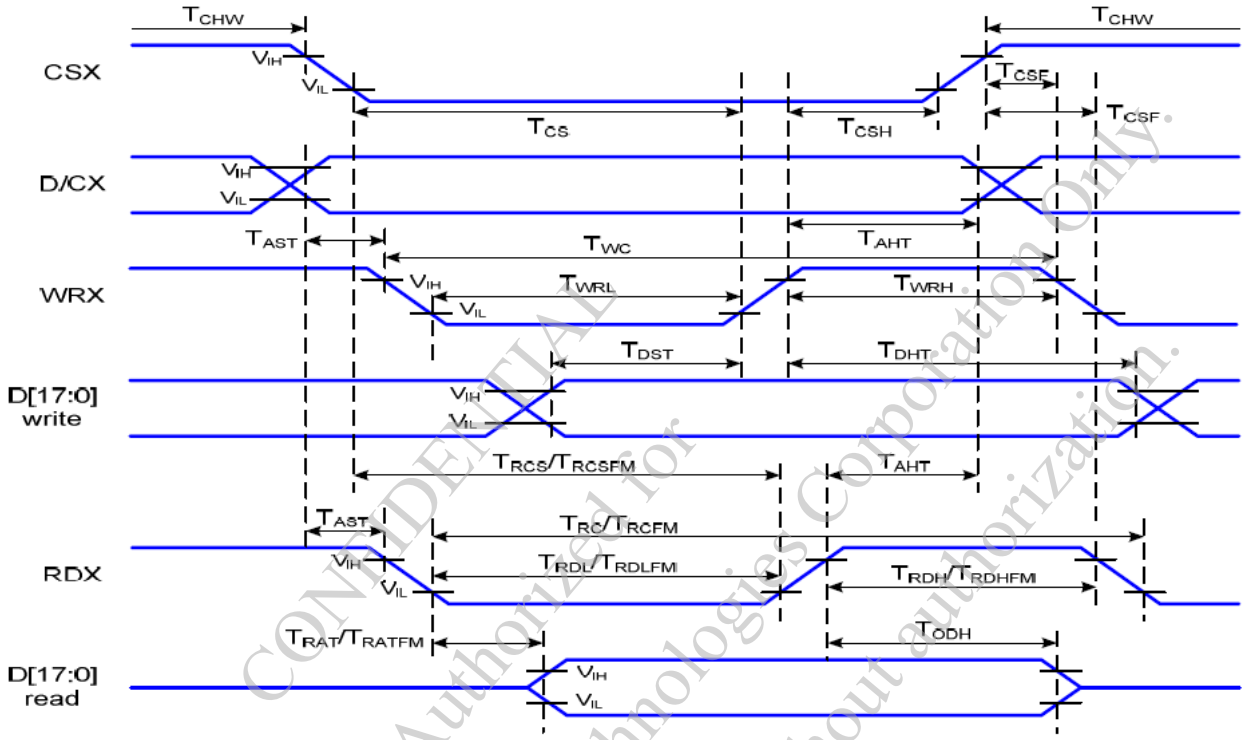
NOTE (4)：DEFINITIONS OF FAILURE.
LCD LUMINANCE BECOMES HALF OF THE INITIAL VALUE.

NOTE (5)：AMBIENT TEMP. VS. ALLOWABLE FORWARD CURRENT. (PER LED)



5. TIMING CHARACTERISTICS

5.1 8080 SERIES MCU PARALLEL INTERFACE CHARACTERISTICS: 18/16/9/8-BIT BUS

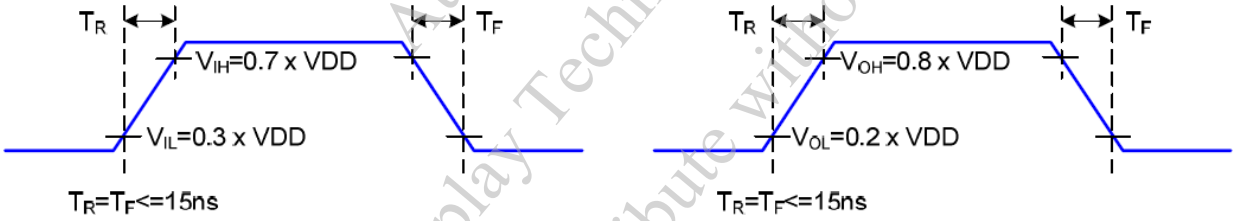


PARALLEL INTERFACE TIMING CHARACTERISTICS (8080-SERIES MCU INTERFACE)

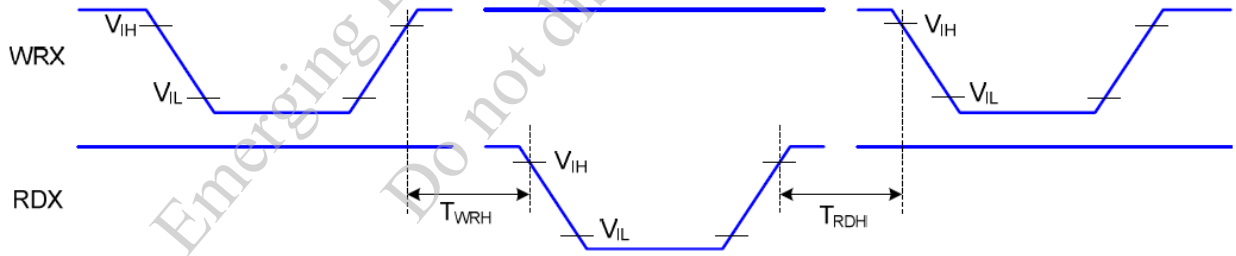
VDD=2.6 TO 3.0V, VCC=2.6 TO 3.0V, VSSD=VSSA=0V, Ta=25°C

SIGNAL	SYMBOL	PARAMETER	MIN.	MAX.	UNIT	DESCRIPTION
D/CX	T_{AST}	ADDRESS SETUP TIME	0	—	ns	—
	T_{AHT}	ADDRESS HOLD TIME (WRITE/READ)	10	—	ns	
CSX	T_{CHW}	CHIP SELECT "H" PULSE WIDTH	0	—	ns	—
	T_{CS}	CHIP SELECT SETUP TIME (WRITE)	15	—	ns	
	T_{RCS}	CHIP SELECT SETUP TIME (READ ID)	45	—	ns	
	T_{RCSFM}	CHIP SELECT SETUP TIME (READ FM)	355	—	ns	
	T_{CSF}	CHIP SELECT WAIT TIME (WRITE/READ)	10	—	ns	
	T_{CSH}	CHIP SELECT HOLD TIME	10	—	ns	
WRX	T_{WC}	WRITE CYCLE	66	—	ns	—
	T_{WRH}	CONTROL PULSE "H" DURATION	15	—	ns	
	T_{WRL}	CONTROL PULSE "L" DURATION	15	—	ns	
RDX (ID)	T_{RC}	READ CYCLE (ID)	160	—	ns	WHEN READ ID DATA
	T_{RDH}	CONTROL PULSE "H" DURATION (ID)	90	—	ns	
	T_{RDL}	CONTROL PULSE "L" DURATION (ID)	45	—	ns	
RDX (FM)	T_{RCFM}	READ CYCLE (FM)	450	—	ns	WHEN READ FROM FRAME MEMORY
	T_{RDHFM}	CONTROL PULSE "H" DURATION (FM)	90	—	ns	
	T_{RDLFM}	CONTROL PULSE "L" DURATION (FM)	355	—	ns	
D[17:0]	T_{DST}	DATA SETUP TIME	10	—	ns	FOR CL=30pF
	T_{DHT}	DATA HOLD TIME	10	—	ns	
	T_{RAT}	READ ACCESS TIME (ID)	—	40	ns	
	T_{RATFM}	READ ACCESS TIME (FM)	—	340	ns	
	T_{ODH}	OUTPUT DISABLE TIME	20	80	ns	

8080 PARALLEL INTERFACE CHARACTERISTICS



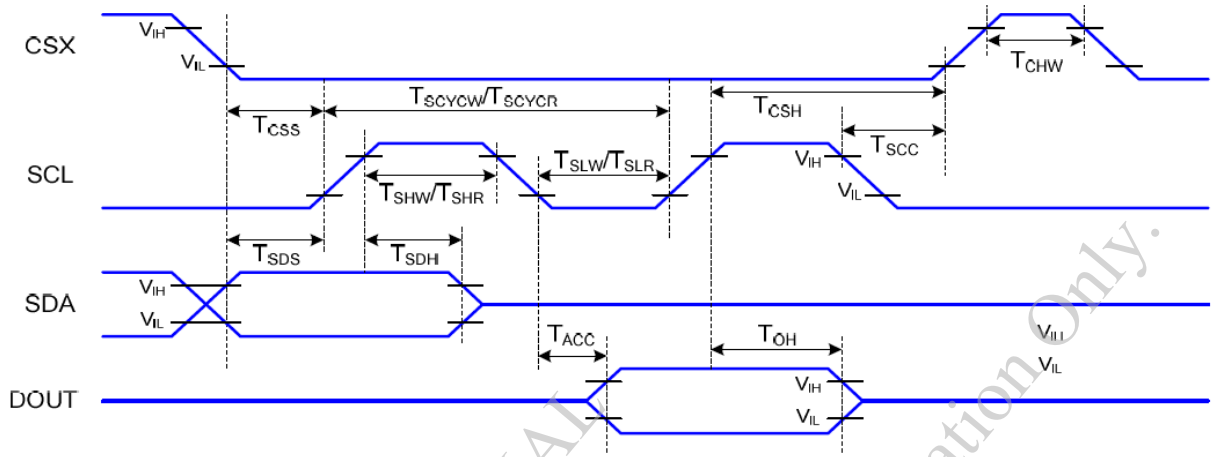
RISING AND FALLING TIMING FOR I/O SIGNAL



WRITE-TO-READ AND READ-TO-WRITE TIMING

NOTE：THE RISING TIME AND FALLING TIME (TR, TF) OF INPUT SIGNAL AND FALL TIME ARE SPECIFIED AT 15 ns OR LESS. LOGIC HIGH AND LOW LEVELS ARE SPECIFIED AS 30% AND 70% OF VDD FOR INPUT SIGNALS.

5.2 SERIAL INTERFACE CHARACTERISTICS (3-LINE SERIAL)



3-LINE SERIAL INTERFACE TIMING CHARACTERISTICS

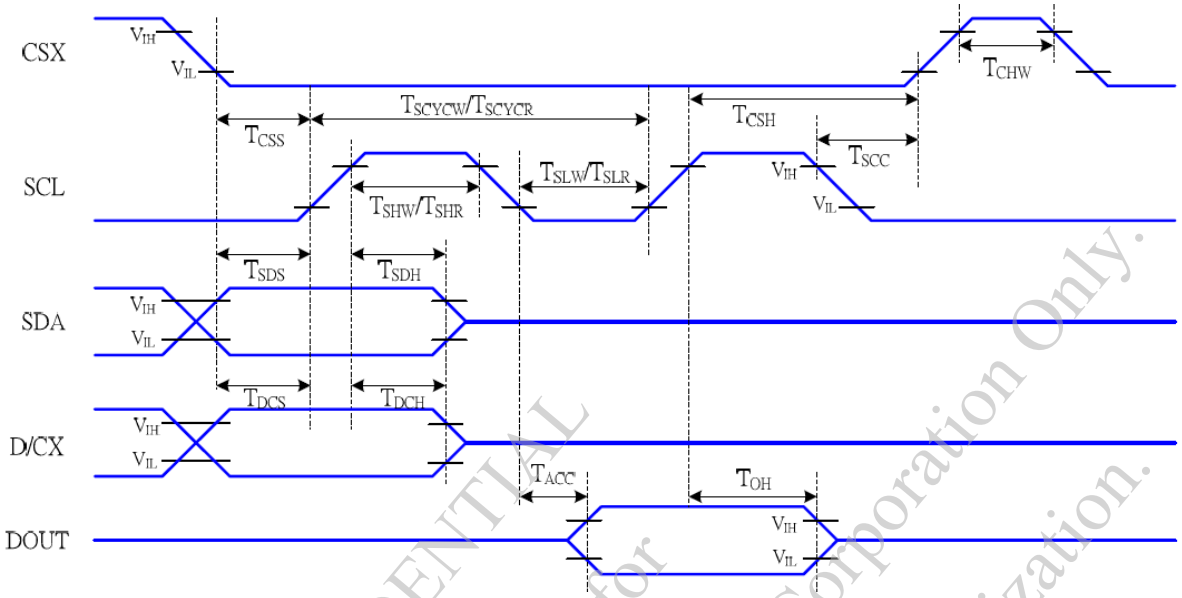
VDD=2.6 TO 3.0V, VCC=2.6 TO 3.0V, VSSD=VSSA=0V, Ta=25°C

SIGNAL	SYMBOL	PARAMETER	MIN.	MAX.	UNIT	DESCRIPTION
CSX	T_{CSS}	CHIP SELECT SETUP TIME (WRITE)	15	—	ns	—
	T_{CSH}	CHIP SELECT HOLD TIME (WRITE)	15	—	ns	
	T_{CSS}	CHIP SELECT SETUP TIME (READ)	60	—	ns	
	T_{SCC}	CHIP SELECT HOLD TIME (READ)	65	—	ns	
	T_{CHW}	CHIP SELECT "H" PULSE WIDTH	40	—	ns	
SCL	T_{SCYCW}	SERIAL CLOCK CYCLE (WRITE)	16	—	ns	—
	T_{SHW}	SCL "H" PULSE WIDTH (WRITE)	7	—	ns	
	T_{SLW}	SCL "L" PULSE WIDTH (WRITE)	7	—	ns	
	T_{SCYCR}	SERIAL CLOCK CYCLE (READ)	150	—	ns	
	T_{SHR}	SCL "H" PULSE WIDTH (READ)	60	—	ns	
	T_{SLR}	SCL "L" PULSE WIDTH (READ)	60	—	ns	
SDA (DIN)	T_{SDS}	DATA SETUP TIME	7	—	ns	—
	T_{SDH}	DATA HOLD TIME	7	—	ns	
DOUT	T_{ACC}	ACCESS TIME	10	50	ns	FOR MAXIMUM CL=30pF FOR MINIMUM CL=8pF
	T_{OH}	OUTPUT DISABLE TIME	15	50	ns	

3-LINE SERIAL INTERFACE CHARACTERISTICS

NOTE：THE RISING TIME AND FALLING TIME (TR, TF) OF INPUT SIGNAL ARE SPECIFIED AT 15 ns OR LESS. LOGIC HIGH AND LOW LEVELS ARE SPECIFIED AS 30% AND 70% OF VDD FOR INPUT SIGNALS.

5.3 SERIAL INTERFACE CHARACTERISTICS (4-LINE SERIAL)



4-LINE SERIAL INTERFACE TIMING CHARACTERISTICS

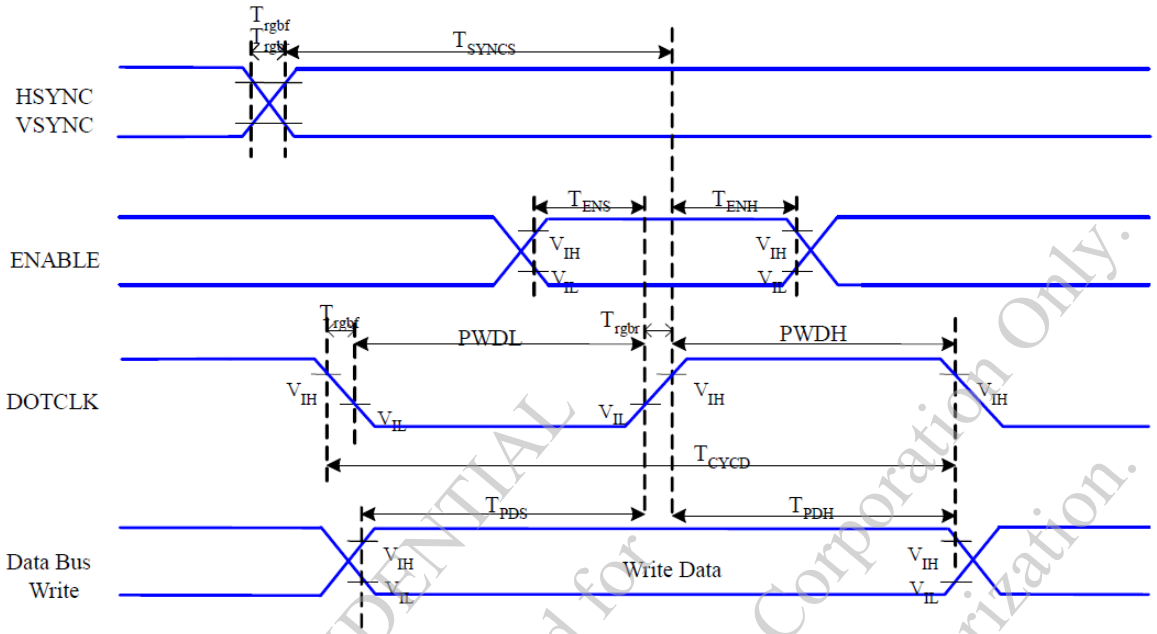
VDD=2.6 TO 3.0V, VCC=2.6 TO 3.0V, VSSD=VSSA=0V, Ta=25°C

SIGNAL	SYMBOL	PARAMETER	MIN.	MAX.	UNIT	DESCRIPTION
CSX	T_{CSS}	CHIP SELECT SETUP TIME (WRITE)	15	—	ns	—
	T_{CSH}	CHIP SELECT HOLD TIME (WRITE)	15	—	ns	
	T_{CSS}	CHIP SELECT SETUP TIME (READ)	60	—	ns	
	T_{SCC}	CHIP SELECT HOLD TIME (READ)	65	—	ns	
	T_{CHW}	CHIP SELECT “H” PULSE WIDTH	40	—	ns	
SCL	T_{SCYCW}	SERIAL CLOCK CYCLE (WRITE)	16	—	ns	-WRITE COMMAND & DATA RAM
	T_{SHW}	SCL “H” PULSE WIDTH (WRITE)	7	—	ns	
	T_{SLW}	SCL “L” PULSE WIDTH (WRITE)	7	—	ns	
	T_{SCYCR}	SERIAL CLOCK CYCLE (READ)	150	—	ns	-READ COMMAND & DATA RAM
	T_{SHR}	SCL “H” PULSE WIDTH (READ)	60	—	ns	
	T_{SLR}	SCL “L” PULSE WIDTH (READ)	60	—	ns	
D/CX	T_{DCS}	D/CX SETUP TIME	10	—	ns	—
	T_{DCH}	D/CX HOLD TIME	10	—	ns	
SDA (DIN)	T_{SDS}	DATA SETUP TIME	7	—	ns	—
	T_{SDH}	DATA HOLD TIME	7	—	ns	
DOUT	T_{ACC}	ACCESS TIME	10	50	ns	FOR MAXIMUM CL=30pF FOR MINIMUM CL=8pF
	T_{OH}	OUTPUT DISABLE TIME	15	50	ns	

4-LINE SERIAL INTERFACE CHARACTERISTICS

NOTE：THE RISING TIME AND FALLING TIME (TR, TF) OF INPUT SIGNAL ARE SPECIFIED AT 15 ns OR LESS. LOGIC HIGH AND LOW LEVELS ARE SPECIFIED AS 30% AND 70% OF VDD FOR INPUT SIGNALS.

5.4 RGB INTERFACE CHARACTERISTICS



RGB INTERFACE TIMING CHARACTERISTICS

VDD=2.6 TO 3.0V, VCC=2.6 TO 3.0V, VSSD=VSSA=0V, Ta=25°C

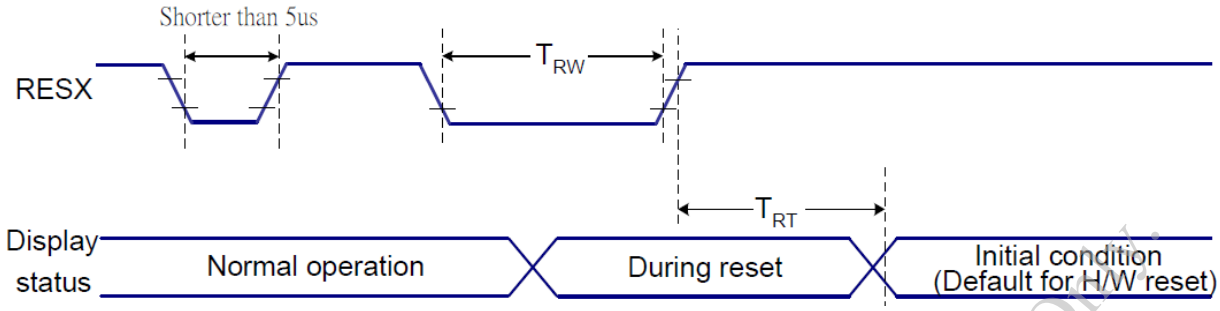
SIGNAL	SYMBOL	PARAMETER	MIN.	MAX.	UNIT	DESCRIPTION
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC SETUP TIME	30	—	ns	—
ENABLE	T_{ENS}	ENABLE SETUP TIME	25	—	ns	—
	T_{ENH}	ENABLE HOLD TIME	25	—	ns	
DOTCLK	PWDH	DOTCLK HIGH-LEVEL PULSE WIDTH	60	—	ns	—
	PWDL	DOTCLK LOW-LEVEL PULSE WIDTH	60	—	ns	
	T_{CYCD}	DOTCLK CYCLE TIME	120	—	ns	
	Trghr, Trghf	DOTCLK RISE/FALL TIME	—	20	ns	
DB	T_{PDS}	PD DATA SETUP TIME	50	—	ns	—
	T_{PDH}	PD DATA HOLD TIME	50	—	ns	

18/16 BITS RGB INTERFACE TIMING CHARACTERISTICS

SIGNAL	SYMBOL	PARAMETER	MIN.	MAX.	UNIT	DESCRIPTION
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC SETUP TIME	35	—	ns	—
ENABLE	T_{ENS}	ENABLE SETUP TIME	35	—	ns	—
	T_{ENH}	ENABLE HOLD TIME	35	—	ns	
DOTCLK	PWDH	DOTCLK HIGH-LEVEL PULSE WIDTH	35	—	ns	—
	PWDL	DOTCLK LOW-LEVEL PULSE WIDTH	35	—	ns	
	T_{CYCD}	DOTCLK CYCLE TIME	80	—	ns	
	Trghr, Trghf	DOTCLK RISE/FALL TIME	—	10	ns	
DB	T_{PDS}	PD DATA SETUP TIME	35	—	ns	—
	T_{PDH}	PD DATA HOLD TIME	35	—	ns	

6 BITS RGB INTERFACE TIMING CHARACTERISTICS

5.5 RESET TIMING



RESET TIMING

VDD=2.6 TO 3.0V, VCC=2.6 TO 3.0V, VSSD=VSSA=0V, Ta=25°C

RELATED PINS	SYMBOL	PARAMETER	MIN.	MAX.	UNIT
RESX	TRW	RESET PULSE DURATION	10	—	us
	TRT	RESET CANCEL	—	5 (NOTE 1, 5)	ms
			—	120 (NOTE 1, 6, 7)	ms

RESET TIMING

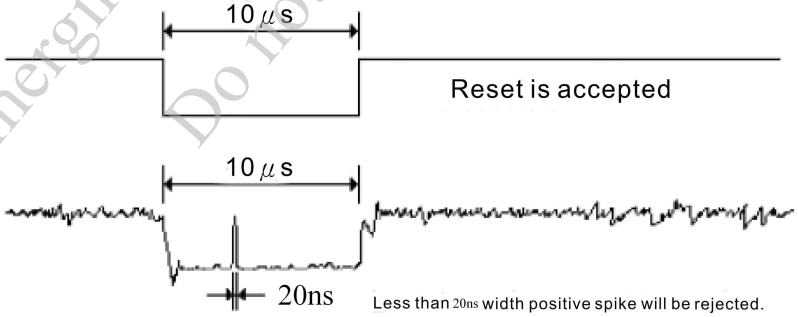
NOTE (1)：THE RESET CANCEL INCLUDES ALSO REQUIRED TIME FOR LOADING ID BYTES, VCOM SETTING AND OTHER SETTINGS FROM NVM (OR SIMILAR DEVICE) TO REGISTERS. THIS LOADING IS DONE EVERY TIME WHEN THERE IS HW RESET CANCEL TIME (tRT) WITHIN 5 ms AFTER A RISING EDGE OF RESX.

NOTE (2)：SPIKE DUE TO AN ELECTROSTATIC DISCHARGE ON RESX LINE DOES NOT CAUSE IRREGULAR SYSTEM RESET ACCORDING TO THE TABLE BELOW:

RESX PULSE	ACTION
SHORTER THAN 5us	RESET REJECTED
LONGER THAN 9us	RESET
Between 5us AND 9us	RESET STARTS

NOTE (3)：DURING THE RESETTING PERIOD, THE DISPLAY WILL BE BLANKED (THE DISPLAY IS ENTERING BLANKING SEQUENCE, WHICH MAXIMUM TIME IS 120 ms, WHEN RESET STARTS IN SLEEP OUT –MODE. THE DISPLAY REMAINS THE BLANK STATE IN SLEEP IN –MODE.) AND THEN RETURN TO DEFAULT CONDITION FOR HARDWARE RESET.

NOTE (4)：SPIKE REJECTION ALSO APPLIES DURING A VALID RESET PULSE AS SHOWN BELOW:



NOTE (5)：WHEN RESET APPLIED DURING SLEEP IN MODE.

NOTE (6)：WHEN RESET APPLIED DURING SLEEP OUT MODE.

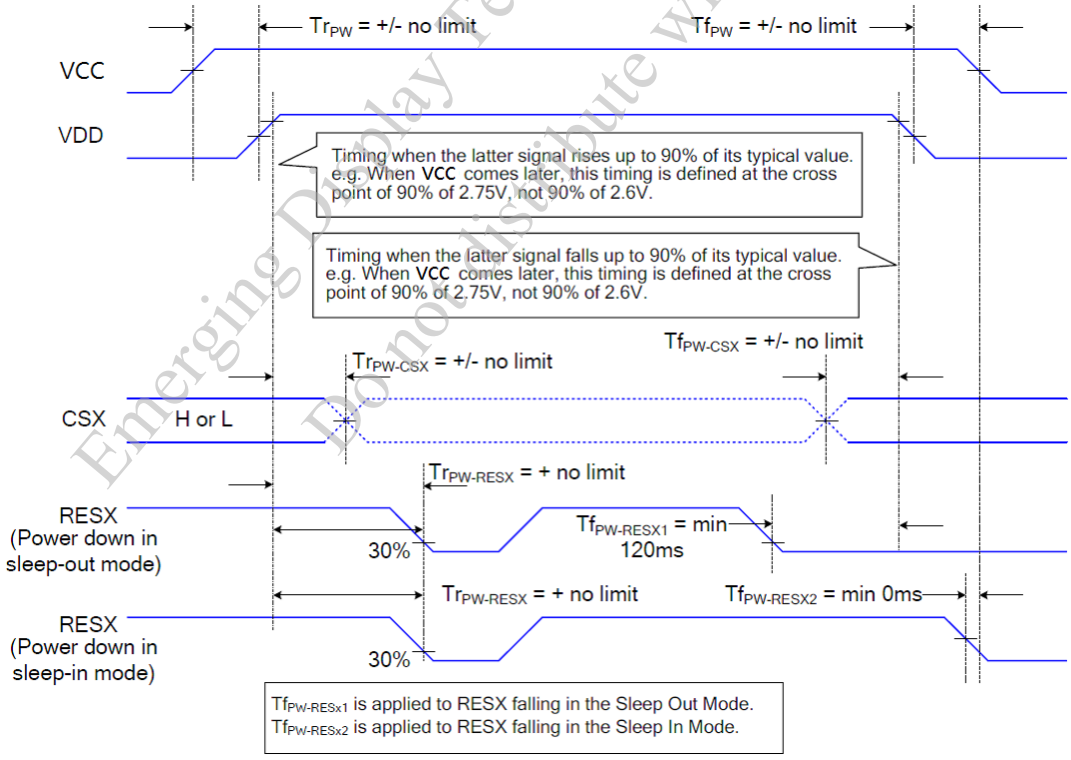
NOTE (7)：IT IS NECESSARY TO WAIT 5msec AFTER RELEASING RESX BEFORE SENDING COMMANDS. ALSO SLEEP OUT COMMAND CANNOT BE SENT FOR 120msec.

5.6 POWER ON/OFF SEQUENCE

VDD AND VCC CAN BE APPLIED IN ANY ORDER.
VCC AND VDD CAN BE POWER DOWN IN ANY ORDER.
DURING POWER OFF, IF LCD IS IN THE SLEEP OUT MODE, VCC AND VDD MUST BE POWERED DOWN MINIMUM 120ms AFTER RESX HAS BEEN RELEASED.
DURING POWER OFF, IF LCD IS IN THE SLEEP IN MODE, VDD OR VCC CAN BE POWERED DOWN MINIMUM 0ms AFTER RESX HAS BEEN RELEASED.
CSX CAN BE APPLIED AT ANY TIMING OR CAN BE PERMANENTLY GROUNDED. RESX HAS PRIORITY OVER CSX.

NOTE (1) : THERE WILL BE NO DAMAGE TO THE DISPLAY MODULE IF THE POWER SEQUENCES ARE NOT MET.
NOTE (2) : THERE WILL BE NO ABNORMAL VISIBLE EFFECTS ON THE DISPLAY PANEL DURING THE POWER ON/OFF SEQUENCES.
NOTE (3) : THERE WILL BE NO ABNORMAL VISIBLE EFFECTS ON THE DISPLAY BETWEEN END OF POWER ON SEQUENCE AND BEFORE RECEIVING SLEEP OUT COMMAND. ALSO BETWEEN RECEIVING SLEEP IN COMMAND AND POWER OFF SEQUENCE.
NOTE (4) : IF RESX LINE IS NOT HELD STABLE BY HOST DURING POWER ON SEQUENCE AS DEFINED IN THE SEQUENCE BELOW, THEN IT WILL BE NECESSARY TO APPLY A HARDWARE RESET (RESX) AFTER HOST POWER ON SEQUENCE IS COMPLETE TO ENSURE CORRECT OPERATION. OTHERWISE FUNCTION IS NOT GUARANTEED.

THE POWER ON/OFF SEQUENCE IS ILLUSTRATED BELOW



5.6.1 UNCONTROLLED POWER OFF

THE UNCONTROLLED POWER-OFF MEANS A SITUATION WHICH REMOVED A BATTERY WITHOUT THE CONTROLLED POWER OFF SEQUENCE. IT WILL NEITHER DAMAGE THE MODULE OR THE HOST INTERFACE.

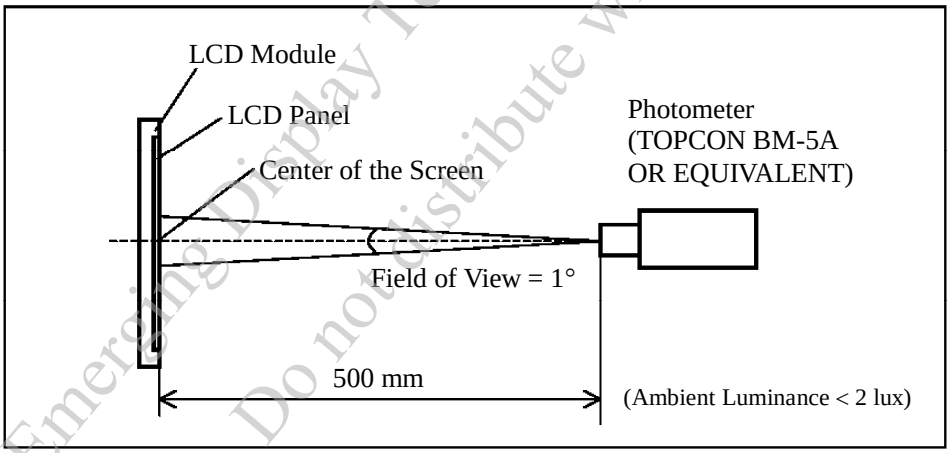
IF UNCONTROLLED POWER-OFF HAPPENED, THE DISPLAY WILL GO BLANK AND THERE WILL NOT ANY VISIBLE EFFECT ON THE DISPLAY (BLANK DISPLAY) AND REMAINS BLANK UNTIL “POWER ON SEQUENCE” POWERS IT UP.

6. OPTICAL CHARACTERISTICS

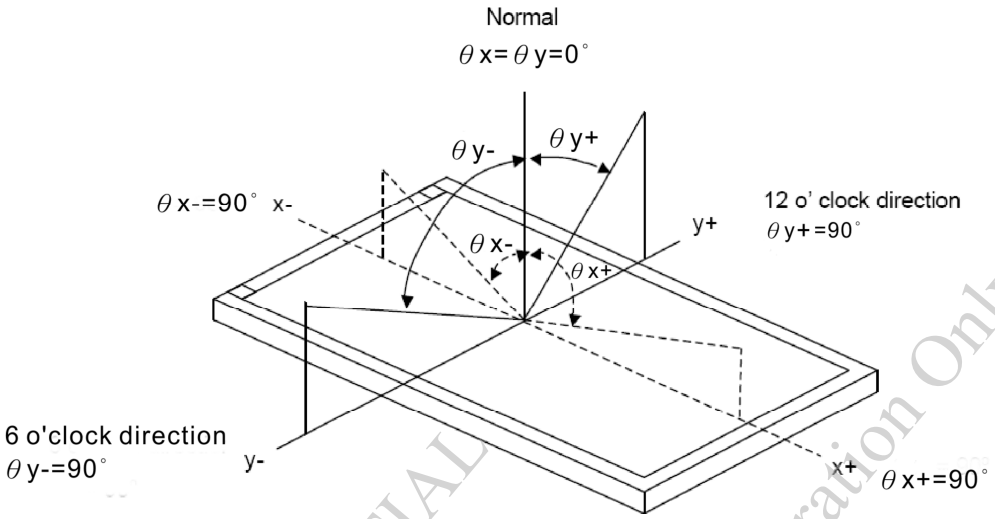
Ta = 25 °C

ITEM		SYMBOL	CONDITION		MIN.	TYP.	MAX.	UNIT	REMARK
VIEWING ANGLE	HOR.	θx+	CENTER CR≥10	θy=0°	—	80	—	deg.	NOTE (2) NOTE (3)
		θx-			—	80	—		
	VER.	θy+		θx=0°	—	80	—		
		θy-			—	80	—		
CONTRAST RATIO (CENTER)		CR	θx = 0°, θy = 0° VDD-VSSD=2.8V VCC-VSSA=2.8V ILED=80mA NTSC：60%		600	800	—		NOTE (3)
RESPONSE TIME		T_R+T_F			—	30	40	ms	NOTE (4)
COLOR CHROMATICITY (CENTER)	WHITE	Wx			0.25	0.30	0.35	—	NOTE (5)
		Wy			0.26	0.31	0.36		
	RED	Rx			0.57	0.62	0.67	—	
		Ry			0.29	0.34	0.39		
	GREEN	Gx			0.27	0.32	0.37	—	
		Gy			0.56	0.61	0.66		
	BLUE	Bx			0.10	0.15	0.20	—	
		By			—	0.05	0.10		
THE BRIGHTNESS OF MODULE (CENTER)		B			450	500	—	cd/m^2	NOTE (6)
THE UNIFORMITY OF MODULE		—			70	75	—	%	NOTE (7)

NOTE (1)：TEST CONDITION：
AFTER STABILIZING AND LEAVING THE PANEL ALONE AT A GIVEN TEMPERATURE FOR 30 MINUTES. MEASUREMENT SHOULD BE EXECUTED IN A STABLE, WINDLESS, AND DARK ROOM.



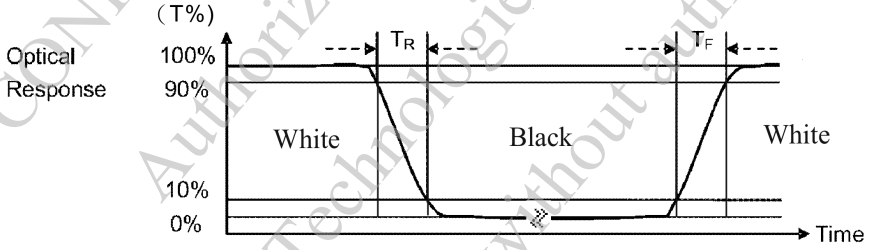
NOTE (2)：DEFINITION OF VIEWING ANGLE :



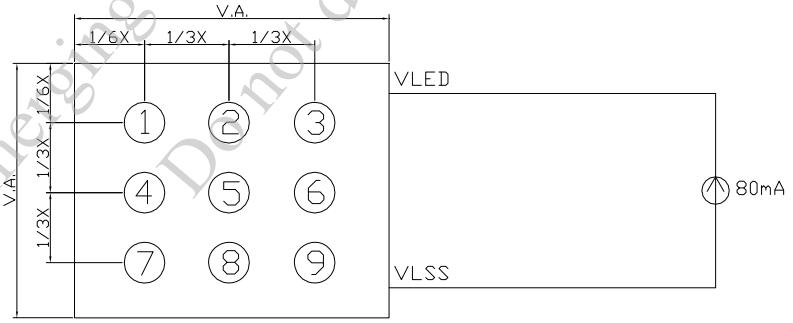
NOTE (3)：DEFINITION OF CONTRAST RATIO (CR) :
MEASURED AT THE CENTER POINT OF MODULE

$$\text{CONTRAST RATIO(CR)} = \frac{\text{BRIGHTNESS MEASURED WHEN LCD IS AT "WHITE STATE"}}{\text{BRIGHTNESS MEASURED WHEN LCD IS AT "BLACK STATE"}}$$

NOTE (4)：DEFINITION OF RESPONSE TIME : T_R AND T_F
THE FIGURE BELOW IS THE OUTPUT SIGNAL OF THE PHOTO DETECTOR.



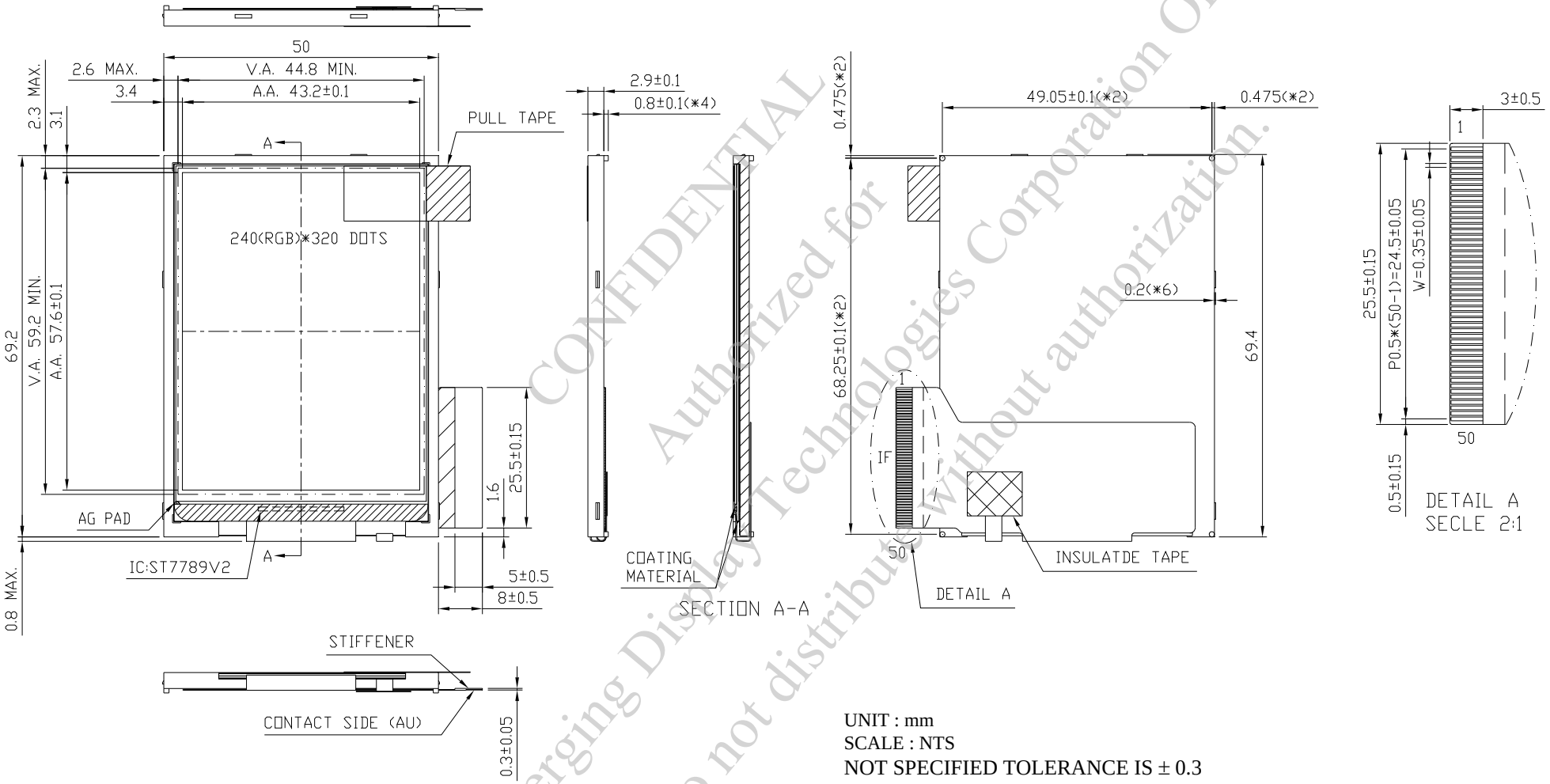
NOTE (5)：DEFINITION OF COLOR CHROMATICITY
(a)100% RGB PIXEL DATA TRANSMISSION WHEN ALL THE INPUT TERMINALS OF MODULE
ARE ELECTRICALLY POWERED ON.
(b)MEASURED AT THE CENTER POINT OF MODULE
NOTE (6)：MEASURED THE BRIGHTNESS OF WHITE STATE AT CENTER POINT.
NOTE (7)：(a)DEFINITION OF BRIGHTNESS UNIFORMITY



(b)THE BRIGHTNESS UNIFORMITY CALCULATING METHOD

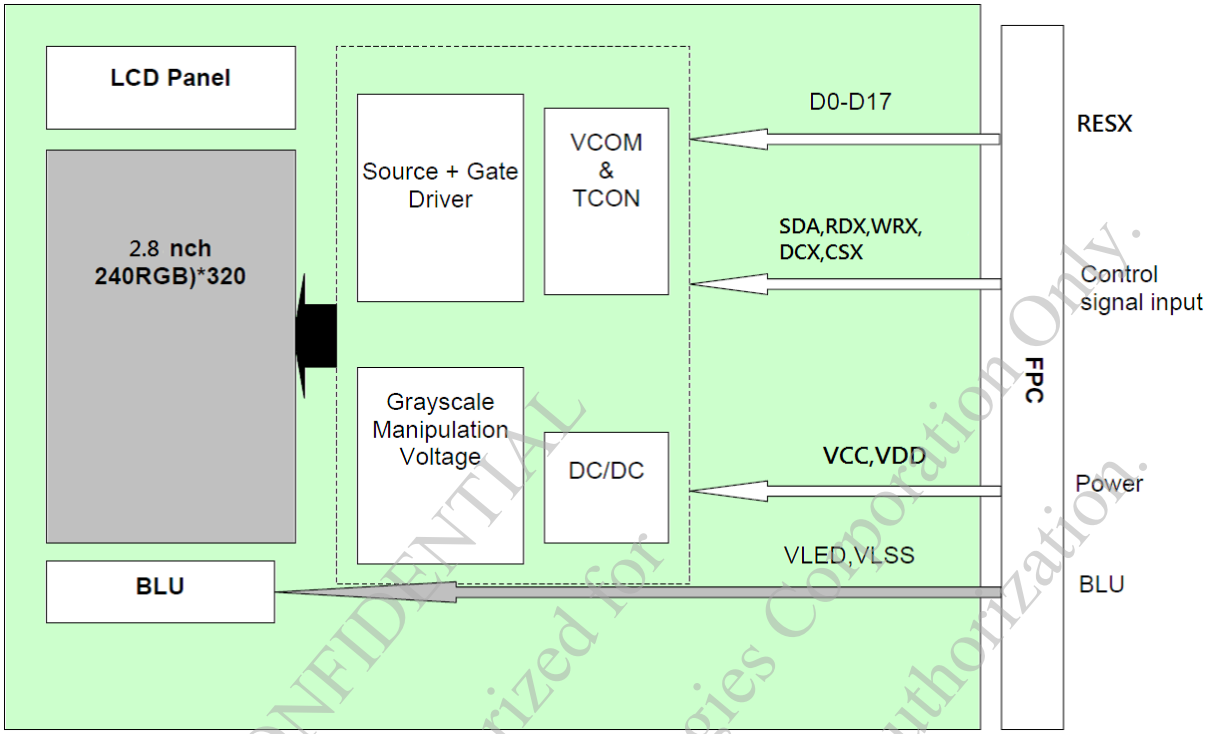
$$\text{UNIFORMITY}：\frac{\text{MINIMUM BRIGHTNESS}}{\text{MAXIMUM BRIGHTNESS}} *100\%$$

7. OUTLINE DIMENSIONS

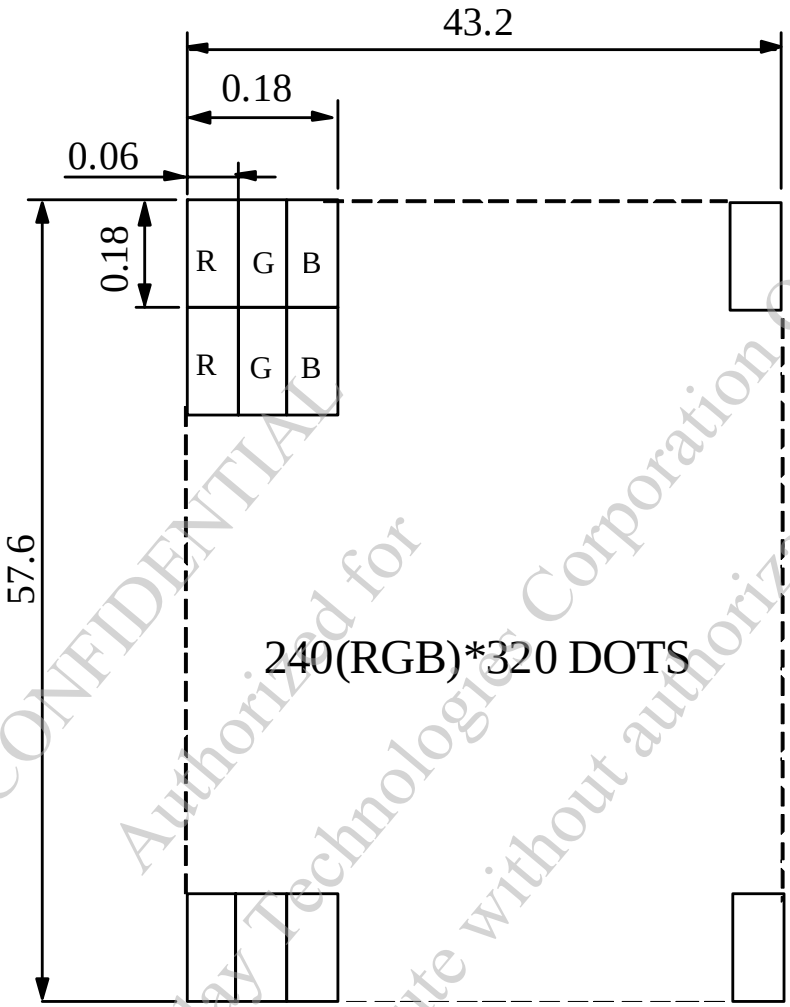


UNIT : mm
SCALE : NTS
NOT SPECIFIED TOLERANCE IS ± 0.3
NOTE : RECOMMED MATCH CONNECTOR KYOCERA:04 6240 050 SERIES

8. BLOCK DIMENSION



9. DETAIL DRAWING OF DOT MATRIX



UNIT : mm
SCALE : NTS
NOT SPECIFIED TOLERANCE IS ± 0.1
DOTS MATRIX TOLERANCE IS ± 0.01

10. INTERFACE SIGNALS

10.1 LCD MODULE CONNECTOR

PIN NO.	SYMBOL	I/O/P	FUNCTION
1	ID	O	MAKER'S IDENTIFICATION (MAY ESTABLISH "H", "L" OR "NC") IF THE CUSTOMER HAS MORE THAN TWO MAKERS WHO APPLIED DIFFERENT S/W, CAN USE THIS PIN TO DETECT THE CODE BY THE MPU AND DECIDE THE MAKER'S ID. MOST IMPORTANTLY, THE CUSTOMER MUST DESIGN THIS PIN ON THE MAIN BOARD AS WELL AND LEAVE IT OPEN AS NOT USED. NOTE : EDT MODULE'S SETTING IS"H".
2	VSSD	I	DIGITAL GROUND
3	VDD	I	DIGITAL IO PAD POWER SUPPLY
4	VSSA	I	ANALOG GROUND
5	VCC	I	ANALOG POWER SUPPLY
6	VSYNC	I	VERTICAL (FRAME) SYNCHRONIZING INPUT SIGNAL FOR RGB INTERFACE OPERATION. IF NOT USED, PLEASE FIX TO THE VDD OR VSSD.
7	HSYNC	I	HORIZONTAL (LINE) SYNCHRONIZING INPUT SIGNAL FOR RGB INTERFACE OPERATION. IF NOT USED, PLEASE FIX TO VDD OR VSSD.
8	ENABLE	I	DATA ENABLE SIGNAL FOR RGB INTERFACE OPERATION. IF NOT USED, PLEASE FIX THIS PIN AT VDD OR VSSD.
9	DOTCLK	I	DOT CLOCK SIGNAL FOR RGB INTERFACE OPERATION. IF NOT USED, PLEASE FIX THIS PIN AT VDD OR VSSD.
10	DCX	I	DISPLAY DATA/COMMAND SELECTION PIN IN PARALLEL INTERFACE. THIS PIN IS USED TO BE SERIAL INTERFACE CLOCK. DCX='1': DISPLAY DATA OR PARAMETER. DCX='0': COMMAND DATA. IF NOT USED, PLEASE FIX THIS PIN AT VDD OR VSSD.
11	RESX	I	THIS SIGNAL WILL RESET THE DEVICE AND IT MUST BE APPLIED TO PROPERLY INITIALIZE THE CHIP. -SIGNAL IS ACTIVE LOW.
12	SDA	I/O	WHEN IM3: LOW, SPI INTERFACE INPUT/OUTPUT PIN. WHEN IM3: HIGH, SPI INTERFACE INPUT PIN. THE DATA IS LATCHED ON THE RISING EDGE OF THE SCL SIGNAL. IF NOT USED, PLEASE FIX THIS PIN AT VDD OR VSSD LEVEL.
13	WRX	I	WRITE ENABLE IN MCU PARALLEL INTERFACE. DISPLAY DATA/COMMAND SELECTION PIN IN 4-LINE SERIAL INTERFACE. SECOND DATA LANE IN 2 DATA LANE SERIAL INTERFACE. IF NOT USED, PLEASE FIX THIS PIN AT VDD OR VSSD.
14	RDX	I	READ ENABLE IN 8080 MCU PARALLEL INTERFACE. IF NOT USED, PLEASE FIX THIS PIN AT VDD OR VSSD.
15	CSX	I	CHIP SELECTION PIN LOW ENABLE. HIGH DISABLE.
16	TE	O	TEARING EFFECT OUTPUT, IF NOT USED, PLEASE OPEN THIS PIN.

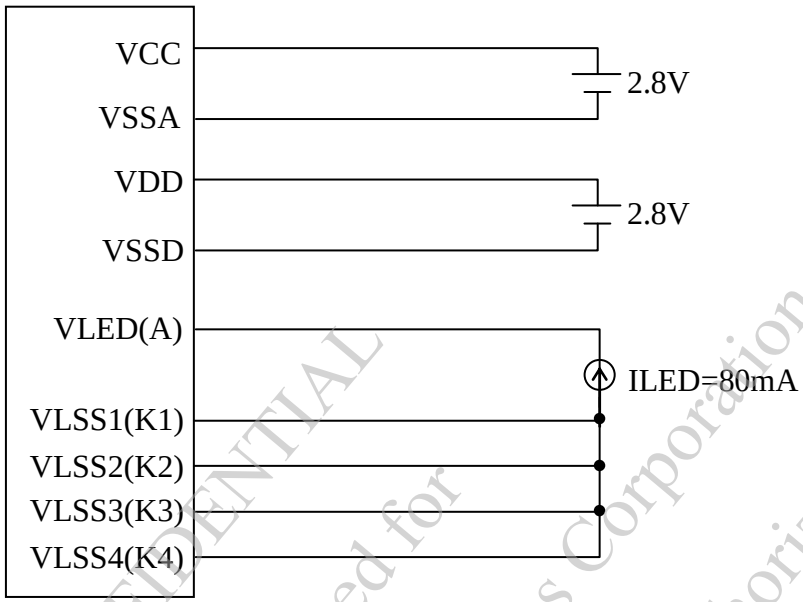
<table>
<tr><th>PIN NO.</th><th>SYMBOL</th><th>I/O/P</th><th>FUNCTION</th></tr>
<tr><td>17</td><td>D0</td><td>I/O</td><td rowspan="17">-DB[17:0] ARE USED AS MCU PARALLEL INTERFACE DATA BUS.
8-BIT I/F: WHEN IM3:0, DB[7:0] ARE USED; WHEN IM3:1, DB[17:10] ARE USED.
9-BIT I/F: WHEN IM3:0, DB[8:0] ARE USED; WHEN IM3:1, DB[17:9] ARE USED.
16-BIT I/F: WHEN IM3:0, DB[15:0] ARE USED; WHEN IM3:1, DB[17:10] AND DB[8:1] ARE USED.
18-BIT I/F: DB[17:0] ARE USED.

-DB[17:0] ARE USED AS RGB INTERFACE DATA BUS.
6-BIT RGB I/F: DB[5:0] ARE USED.
16-BIT RGB I/F: DB[17:13], DB[11:1] ARE USED.
18-BIT RGB I/F: DB[17:0] ARE USED.

-CONNECTED UNUSED PINS TO THE VSSD LEVEL.</td></tr>
<tr><td>18</td><td>D1</td><td>I/O</td></tr>
<tr><td>19</td><td>D2</td><td>I/O</td></tr>
<tr><td>20</td><td>D3</td><td>I/O</td></tr>
<tr><td>21</td><td>D4</td><td>I/O</td></tr>
<tr><td>22</td><td>D5</td><td>I/O</td></tr>
<tr><td>23</td><td>D6</td><td>I/O</td></tr>
<tr><td>24</td><td>D7</td><td>I/O</td></tr>
<tr><td>25</td><td>D8</td><td>I/O</td></tr>
<tr><td>26</td><td>D9</td><td>I/O</td></tr>
<tr><td>27</td><td>D10</td><td>I/O</td></tr>
<tr><td>28</td><td>D11</td><td>I/O</td></tr>
<tr><td>29</td><td>D12</td><td>I/O</td></tr>
<tr><td>30</td><td>D13</td><td>I/O</td></tr>
<tr><td>31</td><td>D14</td><td>I/O</td></tr>
<tr><td>32</td><td>D15</td><td>I/O</td></tr>
<tr><td>33</td><td>D16</td><td>I/O</td></tr>
<tr><td>34</td><td>D17</td><td>I/O</td></tr>
<tr><td>35</td><td>SDO</td><td>O</td><td>SERIAL DATA OUTPUT. IF NOT USE, LET IT TO OPEN.</td></tr>
<tr><td>36</td><td>NC</td><td>NC</td><td>NO USE, LET IT OPEN</td></tr>
<tr><td>37</td><td>NC</td><td>NC</td><td>NO USE, LET IT OPEN</td></tr>
<tr><td>38</td><td>NC</td><td>NC</td><td>NO USE, LET IT OPEN</td></tr>
<tr><td>39</td><td>NC</td><td>NC</td><td>NO USE, LET IT OPEN</td></tr>
<tr><td>40</td><td>NC</td><td>NC</td><td>NO USE, LET IT OPEN</td></tr>
<tr><td>41</td><td>NC</td><td>NC</td><td>NO USE, LET IT OPEN</td></tr>
<tr><td>42</td><td>IM3</td><td>I</td><td rowspan="4">SYSTEM INTERFACE SELECTS.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU INTERFACE MODE</th><th>DATA PIN</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>80-8BIT PARALLEL I/F</td><td>DB[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>80-16BIT PARALLEL I/F</td><td>DB[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80-9BIT PARALLEL I/F</td><td>DB[8:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80-18BIT PARALLEL I/F</td><td>DB[17:0],</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">1</td><td rowspan="2">0</td><td rowspan="2">1</td><td>3-LINE 9BIT SERIAL I/F</td><td>SDA: IN/OUT</td></tr>
<tr><td>2 DATA LANE SERIAL I/F</td><td>SDA: IN/OUT
WRX: IN</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-LINE 8BIT SERIAL I/F</td><td>SDA: IN/OUT</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>80-16BIT PARALLEL I/F II</td><td>DB[17:10],
DB[8:1]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>80-8BIT PARALLEL I/F II</td><td>DB[17:10]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80-18BIT PARALLEL I/F II</td><td>DB[17:0],</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80-9BIT PARALLEL I/F II</td><td>DB[17:9]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-LINE 9BIT SERIAL I/F II</td><td>SDA: IN/SDO: OUT</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-LINE 8BIT SERIAL I/F II</td><td>SDA: IN/SDO: OUT</td></tr>
</table>
IF NOT USED, PLEASE FIX THIS PIN TO VDD OR VSSD LEVEL.</td></tr>
<tr><td>43</td><td>IM2</td><td>I</td></tr>
<tr><td>44</td><td>IM1</td><td>I</td></tr>
<tr><td>45</td><td>IM0</td><td>I</td></tr>
<tr><td>46</td><td>VLSS4(K4)</td><td>I</td><td>POWER SUPPLY FOR LED(-)</td></tr>
<tr><td>47</td><td>VLSS3(K3)</td><td>I</td><td>POWER SUPPLY FOR LED(-)</td></tr>
<tr><td>48</td><td>VLSS2(K2)</td><td>I</td><td>POWER SUPPLY FOR LED(-)</td></tr>
<tr><td>49</td><td>VLSS1(K1)</td><td>I</td><td>POWER SUPPLY FOR LED(-)</td></tr>
<tr><td>50</td><td>VLED(A)</td><td>I</td><td>POWER SUPPLY FOR LED(+)</td></tr>
</table>

11. POWER SUPPLY

11.1 POWER SUPPLY FOR LCM



NOTE : VDD ≤ VCC

12. INSPECTION CRITERIA

12.1 APPLICATION

THIS INSPECTION STANDARD IS TO BE APPLIED TO THE LCD MODULE DELIVERED FROM EMERGING DISPLAY TECHNOLOGIES CORP.(E.D.T) TO CUSTOMERS

12.2 INSPECTION CONDITIONS

12.2.1 (1)OBSERVATION DISTANCE：45±5cm

(2)VIEWING ANGLE：±45°

±45° (FOR SECTION WITHIN VIEWING AREA), REFER TO FIG.A

90° (FOR SECTION OUTSIDE OF VIEWING AREA), REF TO FIG.B

PERPENDICULAR TO MODULE SURFACE

VIEWING ANGLE SHOULD BE SMALLER THAN 45°

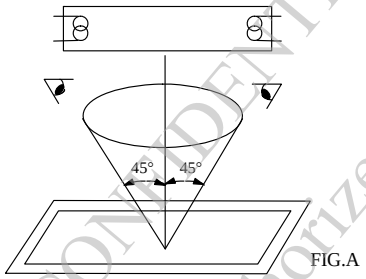


FIG.A

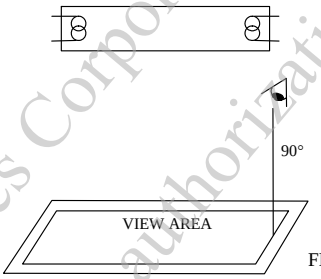


FIG.B

THE INSPECTION CRITERIA IS ACCORDING TO LINE OF SIGHT. INSPECTION SHALL BE MADE WITHIN THE HALF SECTION OF THE VIEWING CONE GENERATED BY LINE SEGMENT OF 45° WITH RESPECT TO THE VERTICAL AXIS FROM CENTER VERTEX OF LCD, THE FLUORESCENT LAMP AND THE CONE AXIS MUST BE PERPENDICULAR TO THE LCD SURFACE.

IF THE DEFECTS ARE OUTSIDE OF VIEWING AREA, IT SHALL BE INSPECTED BY 90° WITH RESPECT TO THE VERTICAL AXIS FROM EDGE OF VIEWING AREA.

12.2.2 ENVIRONMENT CONDITIONS：

AMBIENT TEMPERATURE		25±5°C
AMBIENT HUMIDITY		65 ± 20%RH
AMBIENT ILLUMINATION	COSMETIC INSPECTION	600~800 lux
	FUNCTIONAL INSPECTION	300~500 lux
INSPECTION TIME		10 secs

12.2.3 INSPECTION LOT

QUANTITY PER DELIVERY LOT FOR EACH MODEL

12.2.4 INSPECTION METHOD

A SAMPLING INSPECTION SHALL BE MADE ACCORDING TO THE FOLLOWING PROVISIONS TO JUDGE THE ACCEPTABILITY

(a)APPLICABLE STANDARD：

ANSI/ ASQ Z1.4 NORMAL INSPECTION LEVEL II

(b)AQL : MAJOR DEFECT：AQL 0.65

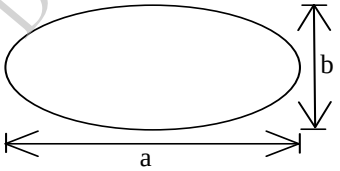
MINOR DEFECT：AQL 1.0

12.3 INSPECTION STANDARDS

12.3.1 VISUAL DEFECTS CLASSIFICATION

TYPE OF DEFECT	INSPECTION ITEM	DEFECT FEATURE	AQL
MAJOR DEFECT	1.DISPLAY ON	• DEFECT TO MISS SPECIFIED DISPLAY FUNCTION, FOR ALL AND SPECIFIED DOTS EX: DISCONNECTION, SHORT CIRCUIT ETC	0.65
	2.BACKLIGHT	• NO LIGHT • FLICKERING AND OTHER ABNORMAL ILLUMINATION	
	3.DIMENSIONS	• SUBJECT TO INDIVIDUAL ACCEPTANCE SPECIFICATIONS	
MINOR DEFECT	1.DISPLAY ZONE	• BLACK/WHITE SPOT • BUBBLES ON POLARIZER • NEWTON RING • BLACK/WHITE LINE • SCRATCH • CONTAMINATION • LEVER COLOR SPREAD	1.0
	2.BEZEL ZONE	• STAINS • SCRATCHES • FOREIGN MATTER	
	3.SOLDERING	• INSUFFICIENT SOLDER • SOLDERED IN INCORRECT POSITION • CONVEX SOLDERING SPOT • SOLDER BALLS • SOLDER SCRAPS	
	4.DISPLAY ON (ALL ON)	• LIGHT LINE	

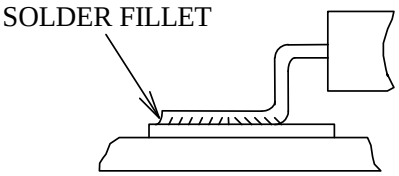
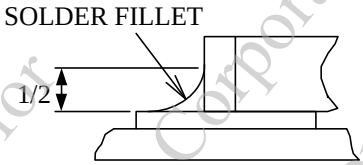
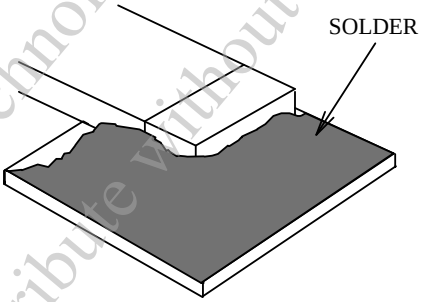
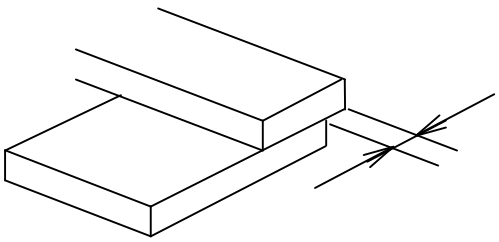
12.3.2 MODULE DEFECTS CLASSIFICATION

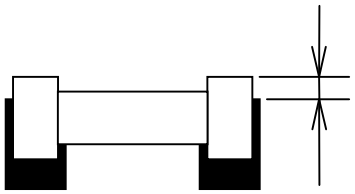
<table>
<tr><th>NO.</th><th>ITEM</th><th>CRITERIA</th></tr>
<tr><td>1</td><td>DISPLAY ON INSPECTION</td><td>(1)INCORRECT PATTERN
(2)MISSING SEGMENT
(3)DIM SEGMENT
(4)OPERATING VOLTAGE BEYOND SPEC</td></tr>
<tr><td>2</td><td>OVERALL DIMENSIONS</td><td>(1)OVERALL DIMENSION BEYOND SPEC</td></tr>
<tr><td>3</td><td>DOT DEFECT</td><td>(1)INSPECTION PATTERN: FULL WHITE, FULL BLACK, RED, GREEN AND BLUE SCREENS.
(2)
<table>
<tr><th>ITEMS</th><th>ACCEPTABLE COUNT</th></tr>
<tr><td>BRIGHT DOT</td><td>N ≤ 1</td></tr>
<tr><td>DARK DOT</td><td>N ≤ 3</td></tr>
<tr><td>TOAL BRIGHT AND DARK DOTS</td><td>N ≤ 3</td></tr>
</table>
NOTE：
1. THE DEFINITION OF DOT：
THE SIZE OF A DEFECTIVE DOT OVER 1/2 OF WHOLE DOT IS REGARDED AS ONE DEFECTIVE DOT.
THE BRIGHT DOT DEFECT MUST BE VISIBLE THROUGH A 5% ND FILTER
2. BRIGHT DOT：
DOTS APPEAR BRIGHT AND UNCHANGED IN SIZE IN WHICH LCD PANEL IS DISPLAYING UNDER BLACK PATTERN.
3. DARK DOT：
DOTS APPEAR DARK AND UNCHANGED IN SIZE IN WHICH LCD PANEL IS DISPLAYING UNDER PURE RED, GREEN, BLUE PICTURE.</td></tr>
<tr><td>4</td><td>FOREIGN BLACK/WHITE/ BRIGHT LINE/ SCRATCH OF VIEWING AREA</td><td>
<table>
<tr><th>LENGTH：L</th><th>WIDTH：W</th><th>PERMISSIBLE NO.</th></tr>
<tr><td>—</td><td>W ≤ 0.05</td><td>IGNORE</td></tr>
<tr><td>L ≤ 3.0</td><td>0.05 < W ≤ 0.1</td><td>3</td></tr>
<tr><td>3.0 < L</td><td>0.1 < W</td><td>NONE</td></tr>
</table>
WIDTH：W mm, LENGTH： L mm
THE DISTANCE BETWEEN DEFECTS SHOULD BE MORE THAN 10mm APART.</td></tr>
<tr><td>5</td><td>FOREIGN MATTER \ BLACK SPOTS \ WHITE SPOTS \ DENT (INCLUDING LIGHT LEAKAGE DUE TO POLARIZING PLATES PINHOLES, ETC.)</td><td>
<table>
<tr><th>AVERAGE DIAMETER (mm): D</th><th>NUMBER OF PIECES PERMITTED</th></tr>
<tr><td>D ≤ 0.15</td><td>IGNORE</td></tr>
<tr><td>0.15 < D ≤ 0.3</td><td>3</td></tr>
<tr><td>0.3 < D</td><td>NONE</td></tr>
</table>
NOTE：DIAMETER D=(a+b)/2
 

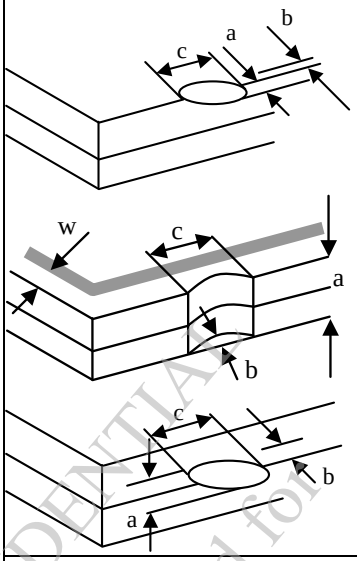
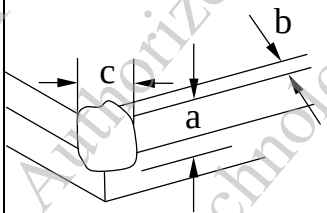
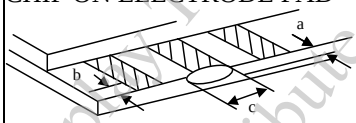
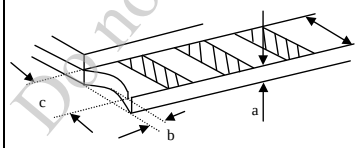
THE DISTANCE BETWEEN DEFECTS SHOULD BE MORE THAN 10mm APART.</td></tr>
</table>

<table>
<tr><th>NO.</th><th>ITEM</th><th>CRITERIA</th></tr>
<tr><td>6</td><td>BUBBLES OF POLARIZER /DIRT/CF FAIL /SURFACE STAINS</td><td>
<table>
<tr><th></th><th>AVERAGE DIAMETER (mm)：D</th><th>NUMBER OF PIECES PERMITTED</th></tr>
<tr><td rowspan="3">BUBBLE ON THE POLARIZER</td><td>D ≤ 0.15</td><td>IGNORE</td></tr>
<tr><td>0.15 < D ≤ 0.3</td><td>N ≤ 3</td></tr>
<tr><td>0.3 < D</td><td>NOTE</td></tr>
<tr><td rowspan="3">SURFACE STAINS / DIRT/ DENT</td><td>D < 0.25</td><td>IGNORE</td></tr>
<tr><td>0.25 < D ≤ 0.35</td><td>N ≤ 3</td></tr>
<tr><td>0.35 < D</td><td>NONE</td></tr>
<tr><td rowspan="3">CF FAIL / SPOT</td><td>D < 0.1</td><td>IGNORE</td></tr>
<tr><td>0.1 < D ≤ 0.3</td><td>N ≤ 3</td></tr>
<tr><td>0.3 < D</td><td>NONE</td></tr>
</table>
NOTE : (1)POLARIZER BUBBLE IS DEFINED AS THE BUBBLE APPEARS ON ACTIVE DISPLAY AREA. THE DEFECT OF POLARIZER BUBBLE SHALL BE IGNORED IF THE POLARIZER BUBBLE APPEARS ON THE OUTSIDE OF ACTIVE DISPLAY AREA.
(2)THE EXTRANEOUS SUBSTANCE IS DEFINED AS IT CAN BE OBSERVED WHEN THE MODULE IS POWER ON.
(3)THE DEFINITION OF AVERAGE DIAMETER, D IS DEFINED AS FOLLOWING.
AVERAGE DIAMETER (D)=(a+b)/2


(4)THE DISTANCE BETWEEN DEFECTS SHOULD BE MORE THAN 10mm APART.</td></tr>
<tr><td>7</td><td>LINE DEFECT ON DISPLAY</td><td>OBVIOUS VERTICAL OR HORIZONTAL LINE DEFECT IS NOT ALLOWED</td></tr>
<tr><td>8</td><td>MURA ON DISPLAY</td><td>IT’S OK IF MURA IS SLIGHT VISIBLE THROUGH 5% ND FILTER</td></tr>
<tr><td>9</td><td>UNEVEN COLOR SPREAD, COLORATION</td><td>(1)TO BE DETERMINED BASED UPON THE STANDARD SAMPLE.</td></tr>
<tr><td>10</td><td>BEZEL APPEARANCE</td><td>(1)BEZEL MAY NOT HAVE RUST, BE DEFORMED OR HAVE FINGER PRINTS STAINS HAVE OTHER CONTAMINATION.
(2)BEZEL MUST COMPLY WITH JOB SPECIFICATIONS.</td></tr>
<tr><td>11</td><td>PCB</td><td>(1)THERE MAY NOT BE MORE THAN 2mm OF SEALANT OUTSIDE THE SEAL AREA ON THE PCB, AND THERE SHOULD BE NO MORE THAN THREE PLACES.
(2)NO OXIDATION OR CONTAMINATION PCB TERMINALS
(3)PARTS ON PCB MUST BE THE SAME AS ON THE PRODUCTION CHARACTERISTIC CHART.
THERE SHOULD BE NO WRONG PARTS, MISSING PARTS OR EXCESS PARTS.
(4)THE JUMPER ON THE PCB SHOULD CONFORM TO THE PRODUCT CHARACTERISTIC CHART.
(5)IF SOLDER GETS ON BEZEL TAB PADS, LED PAD, ZEBRA PAD OR SCREW HOLD PAD; MAKE SURE IT IS SMOOTHED DOWN.</td></tr>
</table>

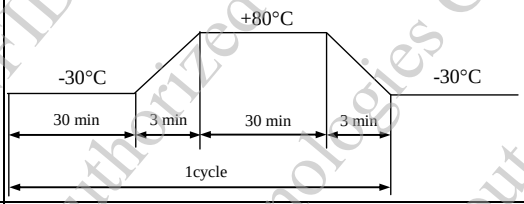
NO.	ITEM	CRITERIA
12	SOLDERING	(1)NO SOLDERING FOUND ON THE SPECIFIED PLACE (2)INSUFFICIENT SOLDER (a)LSI, IC A POOR WETTING OF SOLDER IS BETWEEN LOWER BEND OR "HEEL" OF LEAD AND PAD  (b)CHIP COMPONENT · SOLDER IS LESS THAN 50% OF SIDES AND FRONT FACE WETTING  · SOLDER WETS 3 SIDES OF TERMINAL, BUT LESS THAN 25% OF SIDES AND FRONT SURFACE AREA ARE COVERED  (3)PARTS ALIGNMENT (a)LSI, IC LEAD WIDTH IS MORE THAN 50% BEYOND PAD OUTLINE 

NO.	ITEM	CRITERIA
12	SOLDERING	(b)CHIP COMPONENT COMPONENT IS OFF CENTER, AND MORE THAN 50% OF THE LEADS IS OFF THE PAD OUTLINE  (4)NO UNMELTED SOLDER PASTE MAY BE PRESENT ON THE PCB. (5)NO COLD SOLDER JOINTS, MISSING SOLDER CONNECTIONS, OXIDATION OR ICICLE. (6)NO RESIDUE OR SOLDER BALLS ON PCB. (7)NO SHORT CIRCUITS IN COMPONENTS ON PCB.
13	BACKLIGHT	(1)NO LIGHT (2)FLICKERING AND OTHER ABNORMAL ILLUMINATION (3)SPOTS OR SCRATCHES THAT APPEAR WHEN LIT MUST BE JUDGED USING LCD SPOT, LINES AND CONTAMINATION STANDARDS. (4)BACKLIGHT DOESN'T LIGHT OR COLOR IS WRONG.
14	GENERAL APPEARANCE	(1)NO OXIDATION, CONTAMINATION, CURVES OR, BENDS ON INTERFACE PIN (OLB) OF TCP. (2)NO CRACKS ON INTERFACE PIN (OLB) OF TCP. (3)NO CONTAMINATION, SOLDER RESIDUE OR SOLDER BALLS ON PRODUCT. (4)THE IC ON THE TCP MAY NOT BE DAMAGED, CIRCUITS. (5)THE UPPERMOST EDGE OF THE PROTECTIVE STRIP ON THE INTERFACE PIN MUST BE PRESENT OR LOOK AS IF IT CAUSE THE INTERFACE PIN TO SEVER. (6)THE RESIDUAL ROSIN OR TIN OIL OF SOLDERING (COMPONENT OR CHIP COMPONENT) IS NOT BURNED INTO BROWN OR BLACK COLOR. (7)SEALANT ON TOP OF THE ITO CIRCUIT HAS NOT HARDENED. (8)PIN TYPE MUST MATCH TYPE IN SPECIFICATION SHEET. (9)LCD PIN LOOSE OR MISSING PINS. (10)PRODUCT PACKAGING MUST THE SAME AS SPECIFIED ON PACKAGING SPECIFICATION SHEET. (11)PRODUCT DIMENSION AND STRUCTURE MUST CONFORM TO PRODUCT SPECIFICATION SHEET. (12)THE APPEARANCE OF HEAT SEAL SHOULD NOT ADMIT ANY DIRT AND BREAK.

<table>
<tr><th>NO.</th><th>ITEM</th><th>CRITERIA</th></tr>
<tr><td rowspan="4">15</td><td rowspan="4">CRACKED GLASS</td><td colspan="2">THE LCD WITH EXTENSIVE CRACK IS NOT ACCEPTABLE</td></tr>
<tr><td>GENERAL GLASS CHIP：
 
</td><td>
<table>
<tr><th>a</th><th>b</th><th>c</th></tr>
<tr><td>≤ t/2</td><td>< VIEWING AREA</td><td>≤ 1/8X</td></tr>
<tr><td>t/2 > , ≤ 2t</td><td>≤ W/2</td><td>≤ 1/8X</td></tr>
</table>
*W=DISTANCE BETWEEN SEALANT AREA AND LCD PANEL EDGE
X = LCD SIDE LENGTH
t = GLASS THICKNESS
</td></tr>
<tr><td>CORNER PART：
 
</td><td>
<table>
<tr><th>a</th><th>b</th><th>c</th></tr>
<tr><td>≤ t/2</td><td>< VIEWING AREA</td><td>≤ 1/8X</td></tr>
<tr><td>> t/2 , ≤ 2t</td><td>≤ W/2</td><td>≤ 1/8X</td></tr>
</table>
*W=DISTANCE BETWEEN SEALANT AREA AND LCD PANEL EDGE
X = LCD SIDE LENGTH
t = GLASS THICKNESS
</td></tr>
<tr><td>CHIP ON ELECTRODE PAD
 
</td><td>
<table>
<tr><th>a</th><th>b</th><th>c</th></tr>
<tr><td>≤ t</td><td>≤ 0.5mm</td><td>≤ 1/8X</td></tr>
</table>
* X=LCD SIDE WIDTH
t =GLASS THICKNESS
</td></tr>
<tr><td></td><td> 
</td><td>
<table>
<tr><th>a</th><th>b</th><th>c</th></tr>
<tr><td>≤ t</td><td>≤ 1/8X</td><td>≤ L</td></tr>
</table>
*X=LCD SIDE WIDTH
t = GLASS THICKNESS
L=ELECTRODE PAD LENGTH
①IF GLASS CHIPPING THE ITO TERMINAL, OVER 2/3 OF THE ITO MUST REMAIN AND BE, INSPECTED ACCORDING TO ELECTRODE TERMINAL SPECIFICATIONS
②IF THE PRODUCT WILL BE HEAT SEALED BY THE CUSTOMER, THE ALIGNMENT MARK MUST NOT BE DEMAGED
</td></tr>
</table>

13. RELIABILITY TEST

13.1 STANDARD SPECIFICATIONS FOR RELIABILITY OF LCD MODULE

NO.	ITEM	DESCRIPTION
1	HIGH TEMPERATURE OPERATION	THE SAMPLE SHOULD BE ALLOWED TO STAND AT +70°C FOR 240 hrs
2	LOW TEMPERATURE OPERATION	THE SAMPLE SHOULD BE ALLOWED TO STAND AT -20°C FOR 240 hrs
3	HIGH TEMPERATURE STORAGE	THE SAMPLE SHOULD BE ALLOWED TO STAND AT +80°c FOR 240 hrs
4	LOW TEMPERATURE STORAGE	THE SAMPLE SHOULD BE ALLOWED TO STAND AT -30°C FOR 240 hrs
5	HIGH TEMPERATURE / HIGH HUMIDITY STORAGE	THE SAMPLE SHOULD BE ALLOWED TO STAND AT 60°C, 90% RH 240 hrs
6	THERMAL SHOCK (NOT OPERATED)	THE SAMPLE SHOULD BE ALLOWED TO STAND THE FOLLOWING 10 CYCLES OF OPERATION： 
7	ESD (ELECTROSTATIC DISCHARGE) (NOT OPERATED)	AIR DISCHARGE ± 12KV CONTACT DISCHARGE ± 8KV ACCORDING TO IEC-61000-4-2

NOTE (1)：THE TEST SAMPLES HAVE RECOVERY TIME FOR 2 HOURS AT ROOM TEMPERATURE BEFORE THE FUNCTION CHECK. IN THE STANDARD CONDITIONS, THERE IS NO DISPLAY FUNCTION NG ISSUE OCCURRED.

13.2 TESTING CONDITIONS AND INSPECTION CRITERIA

FOR THE FINAL TEST THE TESTING SAMPLE MUST BE STORED AT ROOM EMPERATURE FOR 24 HOURS, AFTER THE TESTS LISTED IN TABLE 13.1, STANDARD SPECIFICATIONS FOR RELIABILITY HAVE BEEN EXECUTED IN ORDER TO ENSURE STABILITY.

NO.	ITEM	TEST MODEL	INSPECTION CRITERIA
1	CURRENT CONSUMPTION	REFER TO SPECIFICATION	THE CURRENT CONSUMPTION SHOULD CONFORM TO THE PRODUCT SPECIFICATION.
2	CONTRAST	REFER TO SPECIFICATION	AFTER THE TESTS HAVE BEEN EXECUTED, THE CONTRAST MUST BE LARGER THAN HALF OF ITS INITIAL VALUE PRIOR TO THE TESTS.
3	APPEARANCE	VISUAL INSPECTION	DEFECT FREE

14. CAUTION

14.1 OPERATION

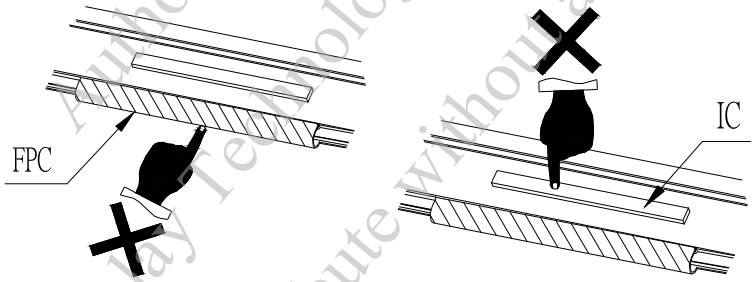
14.1.1 DO NOT CONNECT OR DISCONNECT MODULES TO OR FROM THE MAIN SYSTEM WHILE POWER IS BEING SUPPLIED.

14.1.2 USE THE MODULE WITHIN SPECIFIED TEMPERATURE ; LOWER TEMPERATURE CAUSES THE RETARDATION OF BLINKING SPEED OF THE DISPLAY ; HIGHER TEMPERATURE MAKES OVERALL DISPLAY DISCOLOR . WHEN THE TEMPERATURE RETURNS TO NORMALITY, THE DISPLAY WILL OPERATE NORMALLY.

14.1.3 ADJUST THE LC DRIVING VOLTAGE TO OBTAIN THE OPTIMUM CONTRAST .

14.1.4 POWER ON SEQUENCE INPUT SIGNALS SHOULD NOT BE SUPPLIED TO LCD MODULE BEFORE POWER SUPPLY VOLTAGE IS APPLIED AND REACHES THE SPECIFIED VALUE (5±0.25V).
IF ABOVE SEQUENCE IS NOT FOLLOWED , CMOS LSIS OF LCD MODULES MAY BE DAMAGED DUE TO LATCH - UP PROBLEM .

14.1.5 NOT ALLOWED TO INFLICT ANY EXTERNAL STRESS AND TO CAUSE ANY MECHANICAL INTERFERENCE ON THE BENDING AREA OF FPC DURING THE TAIL BENDING BACKWARDS!
DO NOT STRESS FPC AND IC ON THE MODULE!



14.2 NOTICE

14.2.1 USE A GROUNDED SOLDERING IRON WHEN SOLDERING CONNECTOR I/O TERMINALS. FOR SOLDERING OR REPAIRING , TAKE PRECAUTION AGAINST THE TEMPERATURE OF THE SOLDERING IRON AND THE SOLDERING TIME TO PREVENT PEELING OFF THE THROUGH-HOLE-PAD.

14.2.2 DO NOT DISASSEMBLE . EDT SHALL NOT BE HELD RESPONSIBLE IF THE MODULE IS DISASSEMBLED AND UPON THE REASSEMBLY THE MODULE FAILED .

14.2.3 DO NOT CHARGE STATIC ELECTRICITY, AS THE CIRCUIT OF THIS MODULE CONTAINS CMOS LSIS. A WORKMAN'S BODY SHOULD ALWAYS BE STATIC-PROTECTED BY USE OF AN ESD STRAP. WORKING CLOTHES FOR SUCH PERSONNEL SHOULD BE OF STATIC-PROTECTED MATERIAL.

14.2.4 ALWAYS GROUND THE ELECTRICALLY-POWERED DRIVER BEFORE USING IT TO INSTALL THE LCD MODULE. WHILE CLEANING THE WORK STATION BY VACUUM CLEANER, DO NOT BRING THE SUCKING MOUTH NEAR THE MODULE ; STATIC ELECTRICITY OF THE ELECTRICALLY-POWERED DRIVER OR THE VACUUM CLEANER MAY DESTROY THE MODULE .

14.2.5 DON’T GIVE EXTERNAL SHOCK.

14.2.6 DON’T APPLY EXCESSIVE FORCE ON THE SURFACE.

14.2.7 LIQUID IN LCD IS HAZARDOUS SUBSTANCE. MUST NOT LICK AND SWALLOW. WHEN THE LIQUID IS ATTACHED TO YOUR, SKIN, CLOTHS ETC. WASH IT OUT THOROUGHLY AND IMMEDIATELY.

14.2.8 DON’T OPERATE IT ABOVE THE ABSOLUTE MAXIMUM RATING.

14.2.9 STORAGE IN A CLEAN ENVIRONMENT, FREE FROM DUST, ACTIVE GAS, AND SOLVENT.

14.2.10 STORE WITHOUT ANY PHYSICAL LOAD.

14.2.11 REWIRING : NO MORE THAN 3 TIMES.