EXAMINED BY : Kevin Kuo	EMERGING DISPLAY TECHNOLOGIES CORPORATION	FILE NO . CAS-0009054
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APPROVED BY:		TOTAL PAGE : 30
		VERSION : 1

CUSTOMER ACCEPTANCE SPECIFICATIONS

MODEL NO. :

ET070015DMA

(RoHS)

FOR MESSRS :

_____

CUSTOMER'S APPROVAL

DATE :

_____

BY :

_____

EMERGING DISPLAY TECHNOLOGIES CORPORATION	MODEL NO.	VERSION	PAGE
	ET070015DMA	1	0-1

RECORDS OF REVISION

DOC . FIRST ISSUE

AUG.10, 2020

DATE	REVISED PAGE NO.	SUMMARY

TABLE OF CONTENTS

1. GENERAL SPECIFICATIONS

1.1 DATA SHEETS FOR LCD PANEL CONTROLLER/DRIVER
PLEASE REFER TO :

FITI JD9366

1.2 MATERIAL SAFETY DESCRIPTION
ASSEMBLIES SHALL COMPLY WITH EUROPEAN ROHS REQUIREMENTS, INCLUDING PROHIBITED MATERIALS/COMPONENTS CONTAINING LEAD, MERCURY, CADMIUM, HEXAVALENT CHROMIUM, POLYBROMINATED BIPHENYLS (PBB) AND POLYBROMINATED
DIPHENYL ETHERS (PBDE), BIS(2-ETHYLHEXYL) PHTHALATE (DEHP), BUTYL BENZYL PHTHALATE (BBP), DIBUTYL PHTHALATE (DBP), DIISOBUTYL PHTHALATE (DIBP).

2. MECHANICAL SPECIFICATIONS

2.1 TFT LCD MODULE MECHANICAL SPECIFICATIONS

(1)	DISPLAY SIZE	7 inch
(2)	NUMBER OF DOTS	800W(RGB) * 1280H DOTS
(3)	MODULE SIZE	101.85W * 164H *2.7D mm
(4)	VIEWING AREA	95W * 151.52H mm
(5)	ACTIVE AREA	94.2W * 150.72H mm
(6)	DOT SIZE	0.03925W * 0.11775H mm
(7)	PIXEL SIZE	0.11775W * 0.11775H mm
(8)	LCD TYPE	TFT, IPS, TRANSMISSIVE, ANTE-GLARE, NORMALLY BLACK
(9)	COLOR	16.7M
(10)	VIEWING DIRECTION	SUPER WIDE VIEW
(11)	BACK LIGHT	LED , COLOR : WHITE
(12)	INTERFACE MODE	MIPI

3. ABSOLUTE MAXIMUM RATINGS

3.1 TFT MODULE ELECTRICAL ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	MIN.	MAX.	UNIT
INTERFACE SUPPLY VOLTAGE	VDD-VSS	-0.3	3.6	V

3.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

ITEM	OPERATING		STORAGE		REMARK
	MIN.	MAX.	MIN.	MAX.	
AMBIENT TEMPERATURE	-20°C	70°C	-30°C	80°C	NOTE (1) , (2) , (3)
HUMIDITY	NOTE (3)		NOTE (3)		WITHOUT CONDENSATION
VIBRATION	—	2.45 m/s^2 (0.25 G)	—	11.76m/s^2 (1.2 G)	10~100 Hz XYZ DIRECTIONS 1 HR EACH
SHOCK	—	29.4 m/s^2 (3 G)	—	490.0 m/s^2 (50 G)	10 ms XYZ DIRECTIONS 1 TIME EACH
CORROSIVE GAS	NOT ACCEPTABLE		NOT ACCEPTABLE		

NOTE (1)：THE ABSOLUTE MAXIMUM RATINGS OF THIS PRODUCT SHOULD NOT BE EXCEEDED AT ANY TIME. IF THESE RATINGS ARE EXCEEDED, THE PRODUCT'S PERFORMANCE IS NOT GUARANTEED AND THE PRODUCT MAY EXPERIENCE PERMANENT DAMAGE.

NOTE (2)：BACKGROUND COLOR CHANGES SLIGHTLY DEPENDING ON AMBIENT TEMPERATURE THIS PHENOMENON IS REVERSIBLE.

NOTE (3)：Ta ≤ 60°C：90%RH MAX. (96HRS MAX).
Ta > 60°C：ABSOLUTE HUMIDITY MUST BE LOWER THAN THE HUMIDITY OF 90%RH AT 60°C (96HRS MAX).

4. ELECTRICAL CHARACTERISTICS

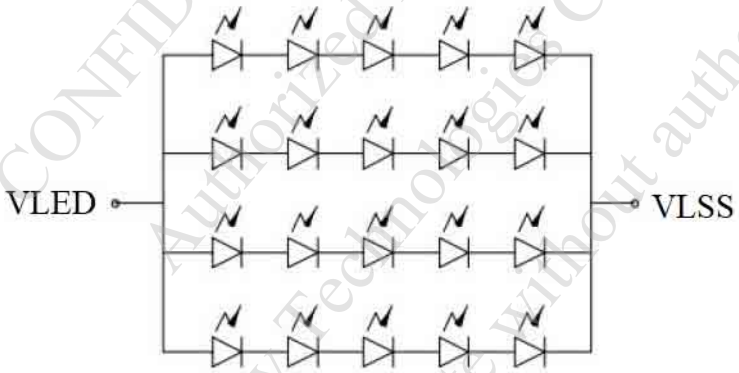
4.1 LCD MODULE ELECTRICAL CHARACTERISTICS

Ta=25°C

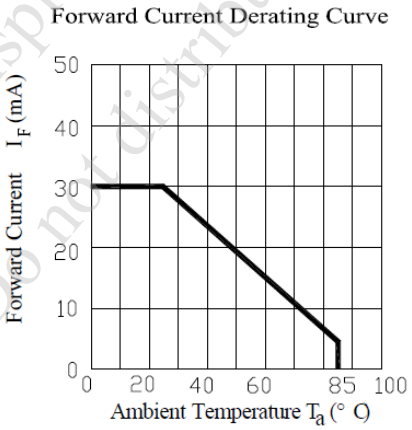
ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
POWER SUPPLY VOLTAGE	VDD-VSS	—	3.15	3.30	3.45	V	
POWER SUPPLY CURRENT	IDD	VDD-VSS=3.3V	—	90	135		NOTE (1)
LOGIC LOW INPUT VOLTAGE	VIL	IOVCC=1.8V±5%	0	—	0.57	V	
LOGIC HIGH INPUT VOLTAGE	VIH		1.2	—	IOVCC	V	
POWER SUPPLY VOLTAGE FOR LED BACKLIGHT	VLED-VLSS	ILED = 92mA	13.25	15	16.75	V	NOTE (2)
LED LIFE TIME	—	IF =23mA (PER LED)	30K	—	—	HRS	NOTE (4) NOTE (5)

NOTE (1)：THE DISPLAY PATTEN IS ALL “BLACK”.

NOTE (2)：INTERNAL CIRCUIT DIAGRAM OF BACKLIGHT



NOTE (3)：AMBIENT TEMP. VS. ALLOWABLE FORWARD CURRENT.(PER LED)



NOTE (4)：CONDITIONS; Ta=25 °C, CONTINUOUS LIGHTING.

NOTE (5)：DEFINITIONS OF LIFE TIME：

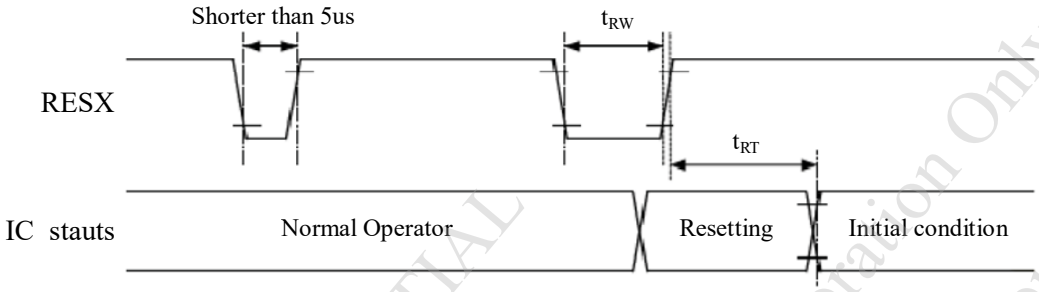
LCM LUMINANCE BECOMES HALF OF THE INITIAL VALUE.

5. TIMING CHARACTERISTICS

5.1 FOR TFT MODULE

5.1.1 AC CHARACTERISTICS

DBI TYPE C INTERFACE CHARACTERISTICS



RESET INPUT TIMINGS

ITEM	SYMBOL	RELATED PINS	MIN.	MAX.	UNIT
RESET PULSE WIDTH(2)	t_{RW}	RESX	10	—	μs
RESET COMPLETE TIME(3)	t_{RT}	—	—	5 NOTE (5)	ms
		—	—	120 NOTE (6), (7)	ms

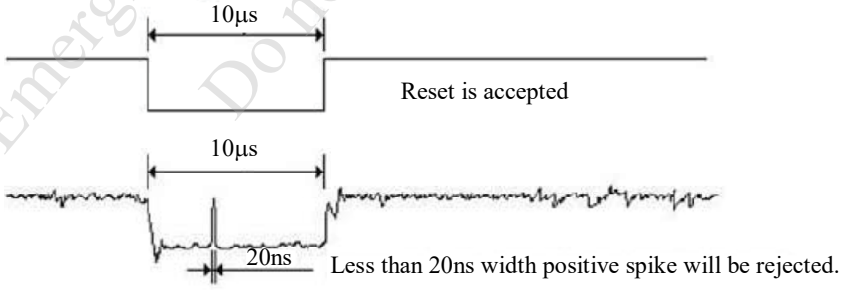
NOTE (1)：THE RESET COMPLETE TIME ALSO REQUIRED TIME FOR LOADING ID BYTES FROM OTP TO REGISTERS. THIS LOADING IS DONE EVERY TIME WHEN THERE IS HW RESET CANCEL TIME (t_{RT}) WITH IN 5 ms AFTER A RISING EDGE OF RESX.

NOTE (2)：SPIKE DUE TO AN ELECTROSTATIC DISCHARGE ON RESX LINE DOES NOT CAUSE IRREGULAR SYSTEM RESET ACCORDING TO THE TABLE BELOW.

RESX PULSE	ACTION
SHORTER THAN 5 μs	RESET REJECTED
LONGER THAN 10 μs	RESET
BETWEEN 5 μs AND 10 μs	RESET START

NOTE (3)：DURING THE RESETTING PERIOD, THE DISPLAY WILL BE BLANKED (THE DISPLAY IS ENTERING BLANKING SEQUENCE, WHICH MAXIMUM TIME IS 120 ms, WHEN RESET STARTS IN SLEEP OUT-MODE. THE DISPLAY REMAINS THE BLANK STATE IN SLEEP IN-MODE) AND THEN RETURNS TO DEFAULT CONDITION FOR H/W RESET.

NOTE (4)：SPIKE REJECTION ALSO APPLIES DURING A VALID RESET PULSE AS SHOWN BELOW.

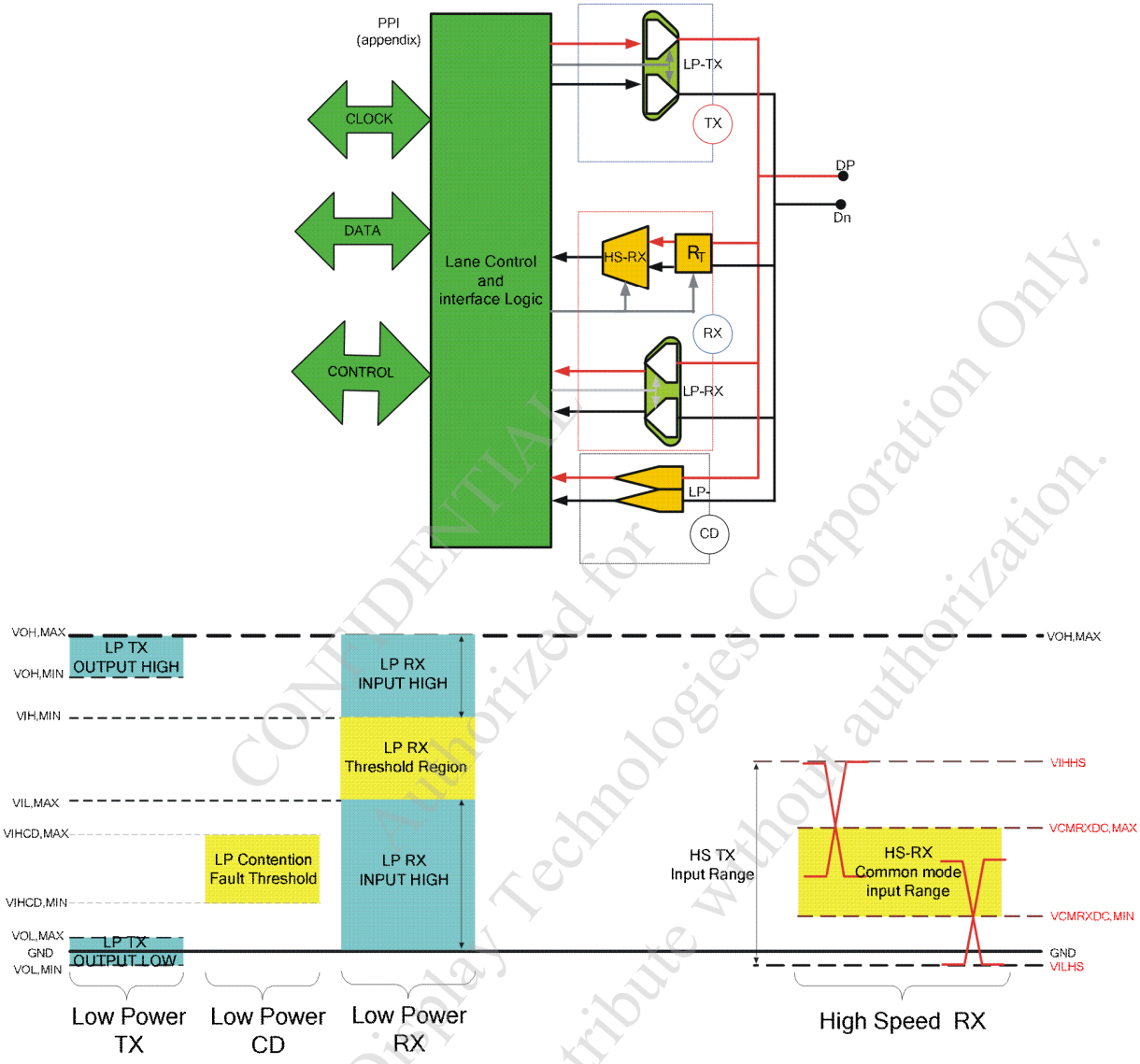


NOTE (5)：WHEN RESET IS APPLIED DURING SLEEP IN MODE.

NOTE (6)：WHEN RESET IS APPLIED DURING SLEEP OUT MODE.

NOTE (7)：IT IS NECESSARY TO WAIT 5msec AFTER RELEASING RESX BEFORE SENDING COMMANDS. ALSO SLEEP OUT COMMAND CANNOT BE SENT FOR 120msec.

DSI D-PHY ELECTRONIC CHARACTERISTICS



HS AND LP SIGNAL LEVELS

THE ELECTRONIC CHARACTERISTICS OF LOW-POWER TRANSMITTER (TX) THE LOW-POWER TX SHALL BE A SLEW-RATE CONTROLLED PUSH-PULL DRIVER. IT IS USED FOR DRIVING THE LINES IN ALL LOW-POWER MODES. HENCE, IT IS IMPORTANT TO KEEP STATIC POWER CONSUMPTION OF A LP TX BE AS LOW AS POSSIBLE. UNDER TABLES LIST DC AND AC CHARACTERISTIC FOR LOW POWER TRANSMITTER

LP-TX DC SPECIFICATIONS

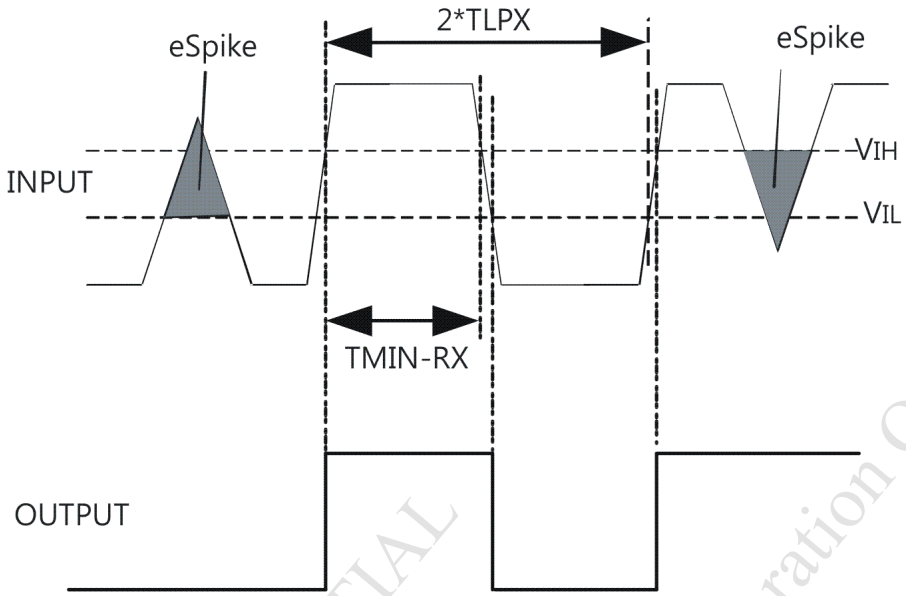
NO.	DESCRIPTION	MIN.	TYP.	MAX.	UNIT	NOTE
V_{OH}	THEVENIN OUTPUT HIGH LEVEL	1.1	1.2	1.3	V	—
V_{OL}	THEVENIN OUTPUT LOW LEVEL	-50	—	50	mV	
Z_{OLP}	OUTPUT IMPEDANCE OF LP-TX	10	—	—	Ω	(1)

NOTE (1): THOUGH NO MAXIMUM VALUE FOR Z_{OLP} IS SPECIFIED, THE LP TRANSMITTER OUTPUT IMPEDANCE SHALL ENSURE THE TRLP/TFLP SPECIFICATION IS MET.

LP-TX AC SPECIFICATIONS

NO.	DESCRIPTION	MIN.	TYP.	MAX.	UNIT	NOTE
t_{RLP}/t_{FLP}	15%-85% RISE TIME AND FALL TIME	—	—	25	ns	(1)
$T_{LP\text{-}PER\text{-}TX}$	PERIOD OF THE LP EXCLUSIVE-OR CLOCK	90	—	—	ns	
$\delta V/\delta t_{SR}$	SLEW RATE @ CLOAD=0pF	30	—	500	mV/ns	(1),(3), (5),(6)
	SLEW RATE @ CLOAD=5pF		—	300	mV/ns	
	SLEW RATE @ CLOAD=20pF	—	—	250	mV/ns	
	SLEW RATE @ CLOAD=70pF	—	—	150	mV/ns	
	SLEW RATE @ CLOAD=0 to 70pF (RISING EDGE ONLY)	30	—	—	mV/ns	(1),(3), (7)
	SLEW RATE @CLOAD=0 to 70pF (RISING EDGE ONLY)	30-0.075* (VO,INST - 700)	—	—	mV/ns	(1),(8), (9)
	SLEW RATE @ CLOAD=0 to 70pF (FALLING EDGE ONLY)	30	—	—	mV/ns	(1),(2), (3)
C_{LOAD}	LOAD CAPACITANCE	—	—	70	pF	

NOTE (1): C_{LOAD} INCLUDES THE LOW-FREQUENCY EQUIVALENT TRANSMISSION LINE CAPACITANCE. THE CAPACITANCE OF TX AND RX ARE ASSUMED TO ALWAYS BE <10pF. THE DISTRIBUTED LINE CAPACITANCE CAN BE UP TO 50pF FOR A TRANSMISSION LINE WITH 2ns DELAY.
NOTE (2): WHEN THE OUTPUT VOLTAGE IS BETWEEN 400 mV AND 930 mV.
NOTE (3): MEASURED AS AVERAGE ACROSS ANY 50 mV SEGMENT OF THE OUTPUT SIGNAL TRANSITION.
NOTE (4): THIS PARAMETER VALUE CAN BE LOWER THAN TLPX DUE TO DIFFERENCES IN RISE VS. FALL SIGNAL SLOPES AND TRIP LEVELS AND MISMATCHES BETWEEN DP AND DN LP TRANSMITTERS.
NOTE (5): THIS VALUE REPRESENTS A CORNER POINT IN A PIECEWISE LINEAR CURVE.
NOTE (6): WHEN THE OUTPUT VOLTAGE IS IN THE RANGE SPECIFIED BY VPIN(ABSMAX).
NOTE (7): WHEN THE OUTPUT VOLTAGE IS BETWEEN 400 MV AND 700 mV .
NOTE (8): WHERE VO, INST IS THE INSTANTANEOUS OUTPUT VOLTAGE, VDP OR VDN, IN MILLIVOLTS.
NOTE (9): WHEN THE OUTPUT VOLTAGE IS BETWEEN 700 mV AND 930 mV.



INPUT GLITCH REJECTIONS OF LOW-POWER RECEIVERS

LP-RX DC SPECIFICATIONS

NO.	DESCRIPTION	MIN.	TYP.	MAX.	UNIT	NOTE
V_{IH}	LOGIC 1 INPUT THRESHOLD	880	—	—	mV	—
V_{IL}	LOGIC 0 INPUT THRESHOLD, NOT IN ULP STATE	—	—	550	mV	—

LP-RX AC SPECIFICATIONS

NO.	DESCRIPTION	MIN.	TYP.	MAX.	UNIT	NOTE
e_{SPIKE}	INPUT PULSE REJECTION	—	—	300	V.ps	(1) , (2) , (3)
T_{MIN}	MINIMUM PULSE WIDTH RESPONSE	20	—	—	ns	(4)
V_{INT}	PEAK-TO-PEAK INTERFERENCE VOLTAGE	—	—	200	mV	—
f_{INT}	INTERFERENCE FREQUENCY	450	—	—	MHz	—

NOTE (1): TIME-VOLTAGE INTEGRATION OF A SPIKE ABOVE V_{IL} WHEN BEING IN LP-0 STATE OR BELOW V_{IH} WHEN BEING IN LP-1 STATE
NOTE (2): AN IMPULSE LESS THAN THIS WILL NOT CHANGE THE RECEIVER STATE.
NOTE (3): IN ADDITION TO THE REQUIRED GLITCH REJECTION, IMPLEMENTERS SHALL ENSURE REJECTION OF KNOWN RF-INTERFERERS.
NOTE (4): AN INPUT PULSE GREATER THAN THIS SHALL TOGGLE THE OUTPUT.

CONTENTION DETECTOR DC SPECIFICATIONS

NO.	DESCRIPTION	MIN.	TYP.	MAX.	UNIT	NOTE
V_{IHCD}	LOGIC 1 CONTENTION THRESHOLD	450	—	—	mV	—
V_{ILCD}	LOGIC 0 CONTENTION THRESHOLD	—	—	200	mV	—

HIGH-SPEED RECEIVER (RX)

THE HS RECEIVER IS A DIFFERENTIAL LINE RECEIVER. IT CONTAINS A SWITCH-ABLE PARALLEL INPUT TERMINATION, Z_{ID}, BETWEEN THE POSITIVE INPUT PIN DP AND THE NEGATIVE INPUT PIN DN. UNDER TABLES LIST DC AND AC CHARACTERISTIC FOR HS-RX.

HS RECEIVER DC SPECIFICATIONS

NO.	DESCRIPTION	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CMRXDC}	COMMON-MODE VOLTAGE HS RECEIVE MODE	70	—	330	mV	(1), (2)
V_{IDTH}	DIFFERENTIAL INPUT HIGH THRESHOLD	—	—	70	mV	—
V_{IDTL}	DIFFERENTIAL INPUT LOW THRESHOLD	-70	—	—	mV	—
V_{IHHS}	SINGLE-ENDED INPUT HIGH VOLTAGE	—	—	460	mV	(1)
V_{ILHS}	SINGLE-ENDED INPUT LOW VOLTAGE	-40	—	—	mV	(1)
Z_{ID}	DIFFERENTIAL INPUT IMPEDANCE	80	—	125	Ω	—

NOTE (1): EXCLUDING POSSIBLE ADDITIONAL RF INTERFERENCE OF 100 mV PEAK SINE WAVE BEYOND 450MHZ.

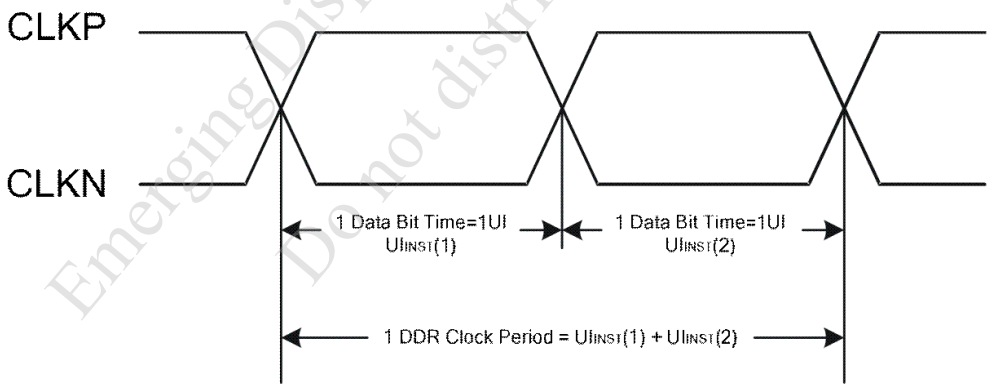
NOTE (2): THIS TABLE VALUE INCLUDES A GROUND DIFFERENCE OF 50mV BETWEEN THE TRANSMITTER AND THE RECEIVER, THE STATIC COMMON-MODE LEVEL TOLERANCE AND VARIATIONS BELOW 450MHZ

HS RECEIVER AC SPECIFICATIONS

NO.	DESCRIPTION	MIN.	TYP.	MAX.	UNIT	NOTE
$\Delta V_{CMRX(HF)}$	COMMON MODE INTERFERENCE BEYOND 450 MHZ	—	—	100	mV_{PP}	(1)
C_{CM}	COMMON MODE TERMINATION	—	—	60	pF	(2)

NOTE (1): $\Delta V_{CMRX(HF)}$ IS THE PEAK AMPLITUDE OF A SINE WAVE SUPERIMPOSED ON THE RECEIVER INPUTS.

NOTE (2): FOR HIGHER BIT RATES A 14pF CAPACITOR WILL BE NEEDED TO MEET THE COMMON-MODE RETURN LOSS SPECIFICATION.

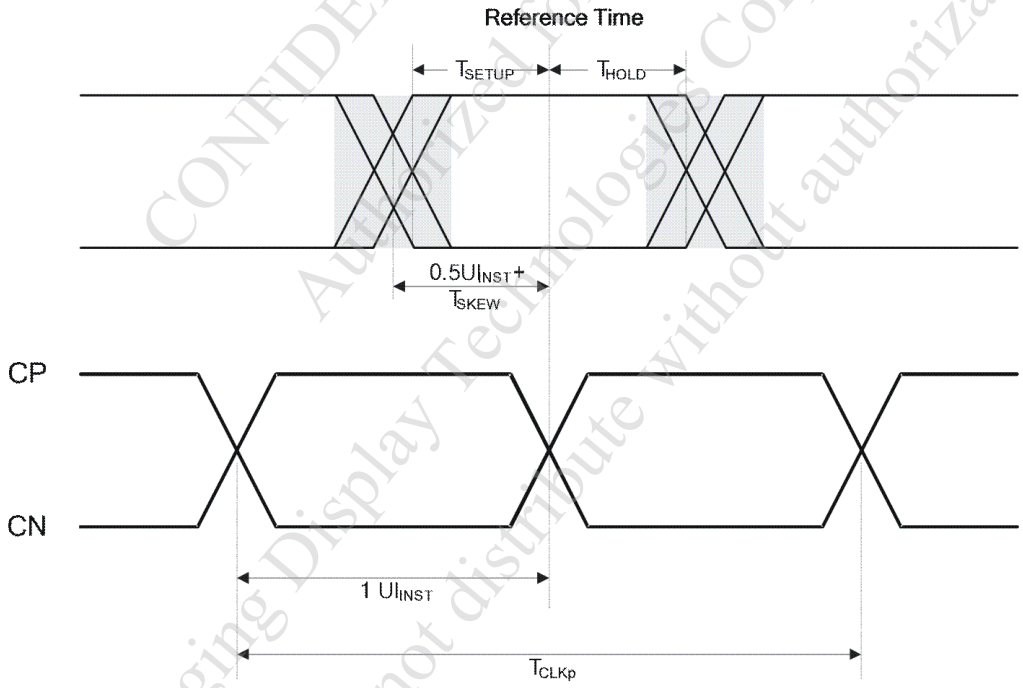


DDR CLOCK DEFINITION

REVERSE HS DATA TRANSMISSION TIMING PARAMETERS

NO.	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
UI INSTANTANEOUS	UI_{INST}	—	—	12.5	ns	(1) , (2) (3) , (4) (5) , (5)

NOTE (1): THIS VALUE CORRESPONDS TO A MINIMUM 80 MBPS DATA RATE.
NOTE (2): THE MINIMUM UI SHALL NOT BE VIOLATED FOR ANY SINGLE BIT PERIOD, I.E., ANY DDR HALF CYCLE WITHIN A DATA BURST.
NOTE (3): MAXIMUM TOTAL BIT RATE IS 850Mbps OF 1 DATA LANE 24-bit DATA FORMAT/ 630MBPS OF 1 DATA LANE 18-bit DATA FORMAT/ 560 Mbps OF 1 DATA LANE 16-bit DATA FORMAT.
NOTE (4): MAXIMUM TOTAL BIT RATE IS 1.7Gbps OF 2 DATA LANES 24-BIT DATA FORMAT/ 1.27GBPS OF 2 DATA LANE 18-bit DATA FORMAT/ 1.13Gbps OF 2 DATA LANE 16-bit DATA FORMAT.
NOTE (5): MAXIMUM TOTAL BIT RATE IS 2Gbps OF 3 DATA LANES 24-bit DATA FORMAT/ 1.5Gbps OF 3 DATA LANE 18-bit DATA FORMAT/1.33Gbps OF 3 DATA LANE 16-bit DATA FORMAT.
NOTE (6): MAXIMUM TOTAL BIT RATE IS 2Gbps OF 4 DATA LANES 24-bit DATA FORMAT/ 1.5Gbps OF 4 DATA LANE 18-BIT DATA FORMAT/ 1.33Gbps OF 4 DATA LANE 16-bit DATA FORMAT.

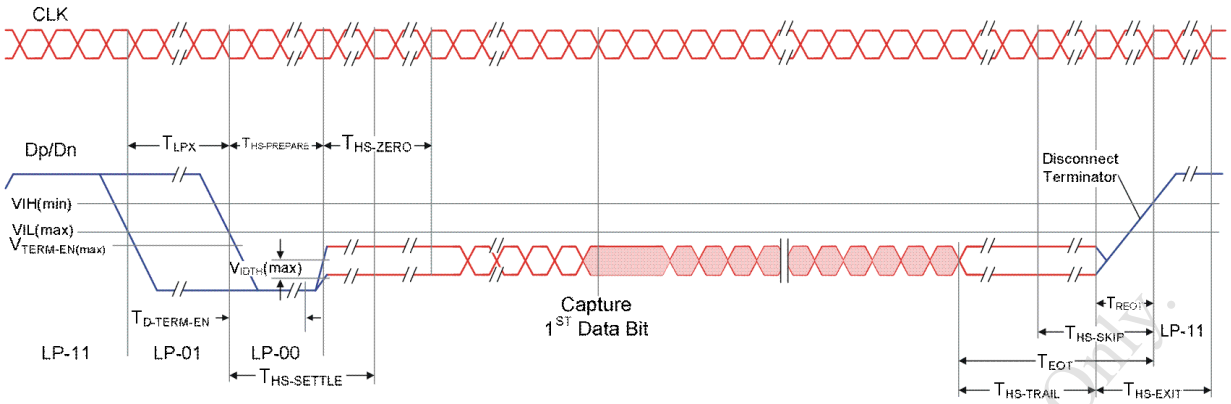


DATA TO CLOCK TIMING DEFINITIONS

DATA TO CLOCK TIMING SPECIFICATIONS

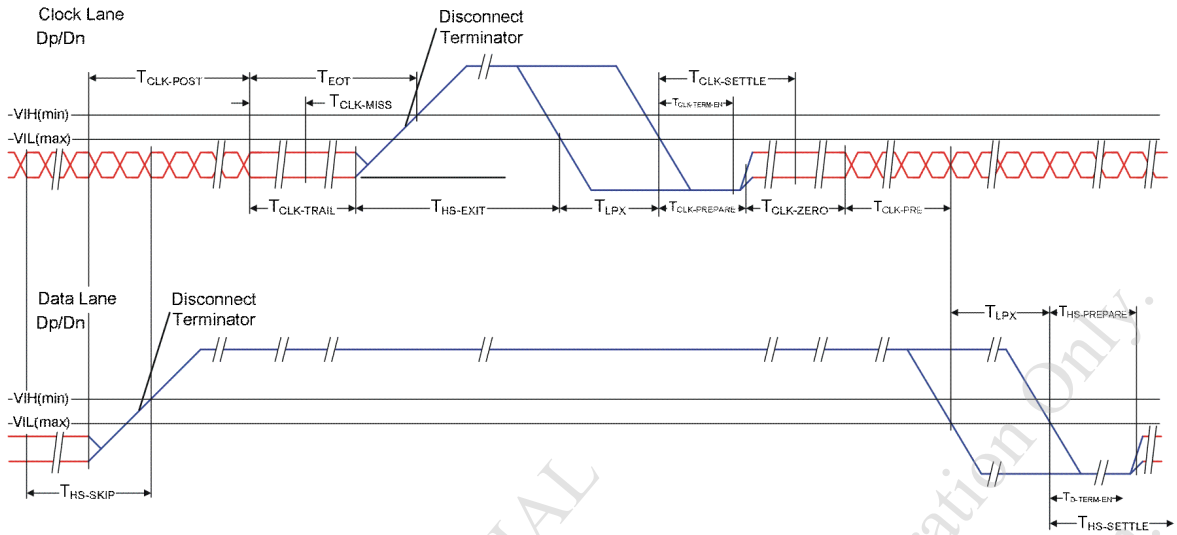
NO.	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
DATA TO CLOCK SETUP TIME [RX]	$T_{SETUP[RX]}$	0.15	—	—	UIINST	(1)
CLOCK TO DATA HOLD TIME [RX]	$T_{HOLD[RX]}$	0.15	—	—	UIINST	(1)

NOTE (1): TOTAL SETUP AND HOLD WINDOW FOR RECEIVER OF 0.3*UIINST.



HIGH-SPEED DATA TRANSMISSION IN BURSTS

NO.	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
T_{LPX}	TRANSMITTED LENGTH OF ANY LOW-POWER STATE PERIOD	50	—	—	ns
$T_{HS-PREPARE}$	TIME THAT THE TRANSMITTER DRIVES THE DATA LANE LP-00 LINE STATE IMMEDIATELY BEFORE THE HS-0 LINE STATE STARTING THE HS TRANSMISSION	40+4*UI	—	85+6*UI	ns
$T_{HS-PREPARE}$ +$T_{HS-ZERO}$	$T_{HS-PREPARE}$ +TIME THAT THE TRANSMITTER DRIVES THE HS-0 STATE PRIOR TO TRANSMITTING THE SYNC SEQUENCE.	145+10*UI	—	—	ns
$T_{D-TERM-EN}$	TIME FOR THE DATA LANE RECEIVER TO ENABLE THE HS LINE TERMINATION.	—	—	35+4*UI	ns
$T_{HS-SETTLE}$	TIME INTERVAL DURING WHICH THE HS RECEIVER SHALL IGNORE ANY DATA LANE HS TRANSITIONS.	85+6*UI	—	145+10*UI	ns
$T_{HS-TRAIL}$	TIME THAT THE TRANSMITTER DRIVES THE FLIPPED DIFFERENTIAL STATE AFTER LAST PAYLOAD DATA BIT OF A HS TRANSMISSION BURST	MAX(n*8UI, 60+n*4*UI)	—	—	ns
$T_{HS-EXIT}$	TIME THAT THE TRANSMITTER DRIVES LP-11 FOLLOWING A HS BURST.	100	—	—	ns

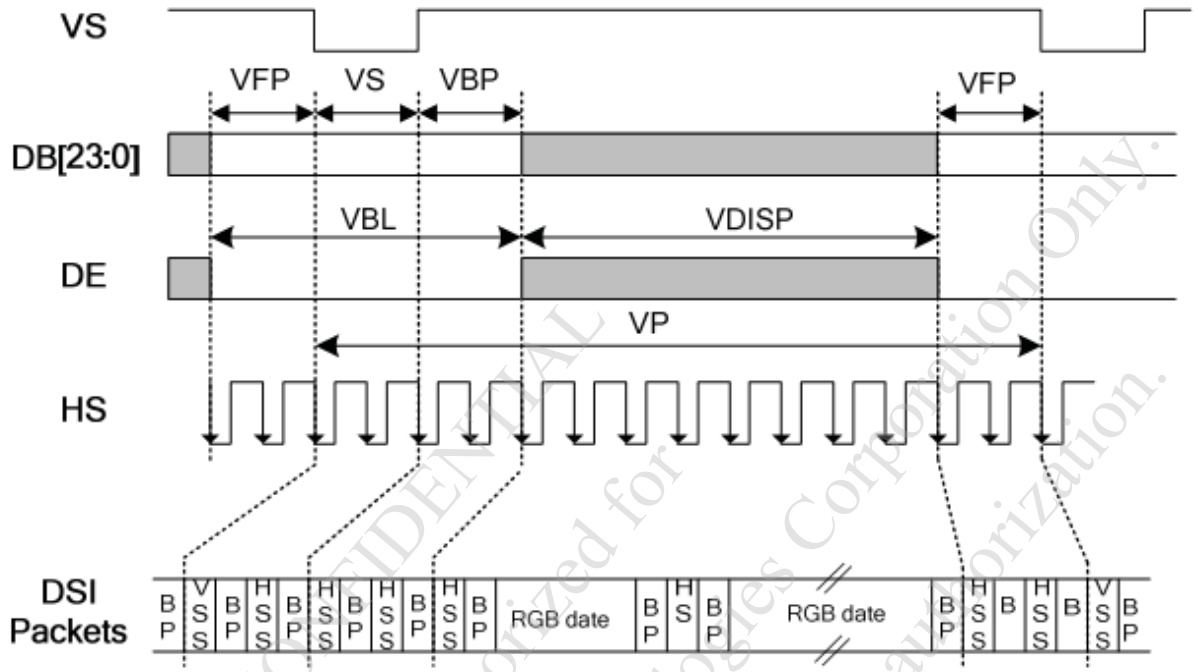


SWITCHING THE CLOCK LANE BETWEEN CLOCK TRANSMISSION AND LOW-POWER MODE

NO.	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
$T_{CLK-POST}$	TIME THAT THE TRANSMITTER CONTINUES TO SEND HS CLOCK AFTER THE LAST ASSOCIATED DATA LANE HAS TRANSITIONED TO LP MODE.	60+52*UI	—	—	ns
$T_{CLK-PRE}$	TIME THAT THE HS CLOCK SHALL BE DRIVEN BY THE TRANSMITTER PRIOR TO ANY ASSOCIATED DATA LANE BEGINNING THE TRANSITION FROM LP TO HS MODE.	8*UI	—	—	ns
$T_{CLK-PREPARE}$	TIME THAT THE TRANSMITTER DRIVES THE CLOCK LANE LP-00 LINE STATE IMMEDIATELY BEFORE THE HS-0 LINE STATE STARTING THE HS TRANSMISSION.	38	—	95	ns
$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	$T_{CLK-PREPARE}$+TIME THAT THE TRANSMITTER DRIVES THE HS-0 STATE PRIOR TO STARTING THE CLOCK.	300	—	—	ns
$T_{CLK-TERM-EN}$	TIME FOR THE CLOCK LANE RECEIVER TO ENABLE THE HS LINE TERMINATION.	—	—	38	ns
$T_{CLK-TRAIL}$	TIME THAT THE TRANSMITTER DRIVES THE HS-0 STATE AFTER THE LAST PAYLOAD CLOCK BIT OF A HS TRANSMISSION BURST.	60	—	—	ns
$T_{HS-EXIT}$	TIME THAT THE TRANSMITTER DRIVES LP-11 FOLLOWING A HS BURST.	100	—	—	ns

5.2.1 TIMINGS FOR DSI VIDEO MODE

5.2.1.1 VERTICAL TIMINGS



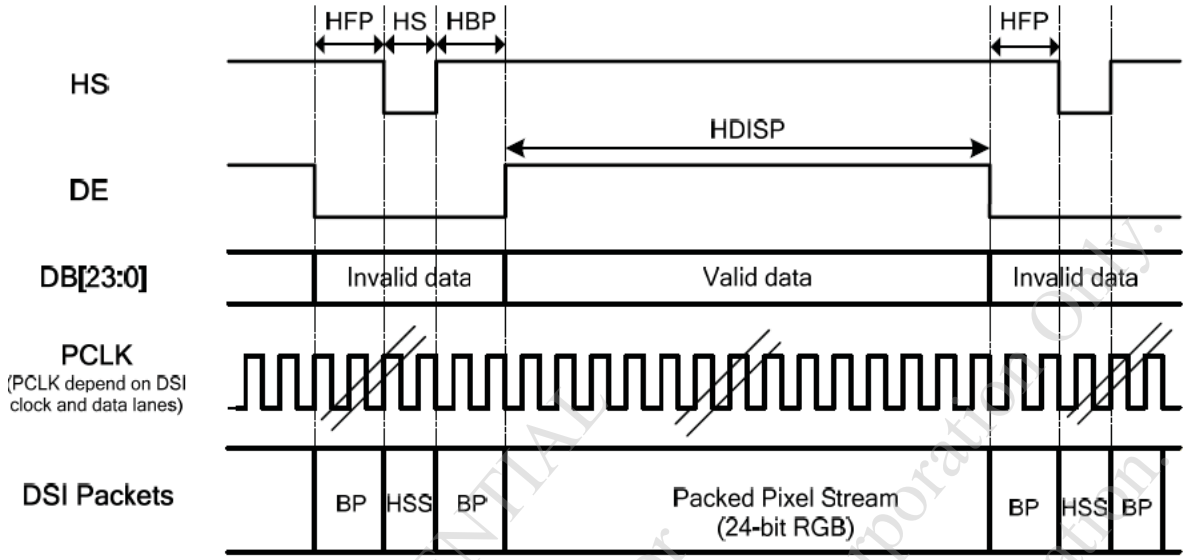
VERTICAL TIMINGS FOR DPI I/F

RESOLUTION=800*1280(T_A=25°C, VDDIO=1.8V, VCIP=3.3V, VDD=3.3V)

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
VERTICAL LOW PULSE WIDTH	VS	—	2	4	200 NOTE (1)	Line
VERTICAL FRONT PORCH	VFP	—	4	20	200	Line
VERTICAL BACK PORCH	VBP	—	2	10	200 NOTE (1)	Line
VERTICAL BLANKING PERIOD	VBK	VS+VBP+VFP	8	34	250	Line
VERTICAL ACTIVE AREA	—	VDISP	—	1280	—	Line
VERTICAL REFRESH RATE	VRR	—	—	60	—	Hz

NOTE (1)：THE VS AND VBP PULSE WIDTH ARE RELATED TO GIP START PULSE AND GIP CLOCK PULSE TIMING. THE GIP START PULSE AND GIP CLOCK PULSE MUST BE SET AT CORRESPONDING POSITION FOR LCD NORMAL DISPLAY.

5.2.1.2 HORIZONTAL TIMINGS



HORIZONTAL TIMING FOR DSI VIDEO MODE I/F

RESOLUTION=800*1280(T_A=25°C, VDDIO=1.8V, VCIP=VDD=VCCH=3.3V)

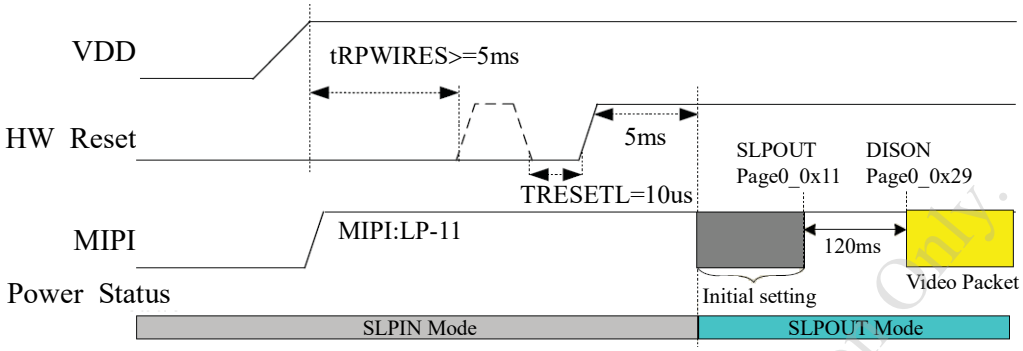
ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
HS LOW PULSE WIDTH	HS	—	6	18	78	DCK
HORIZONTAL BACK PORCH	HBP	—	5	18	78	DCK
HORIZONTAL FRONT PORCH	HFP	—	5	18	78	DCK
HORIZONTAL BLANKING PERIOD	HBLK	HS+HBP+HFP	16	54 NOTE (1)	88	DCK
HORIZONTAL ACTIVE AREA	HDISP	—	—	800	—	DCK
PIXEL CLOCK	PCLK	—	63.06 NOTE (2)	67.33 NOTE (2)	81.51 NOTE (2)	MHz

NOTE (1)：HS+HBP > 0.5us.

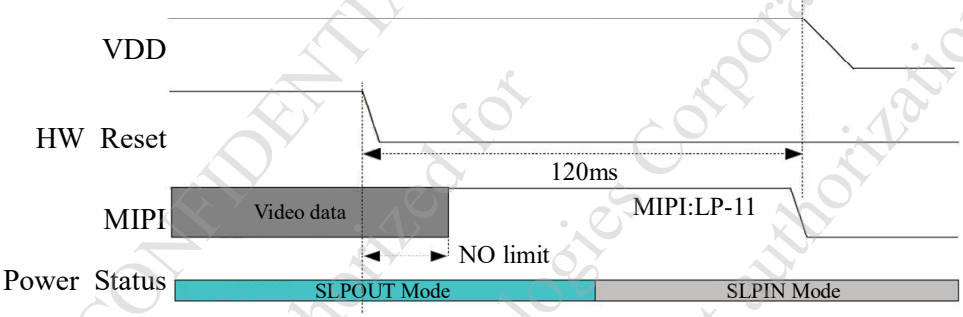
NOTE (2)：PIXEL CLOCK = (HBLK+HDISP) * (VBK+VDISP) * FRAME RATE, FRAME RATE=60Hz.

5.2.2 POWER-ON/OFF SEQUENCE FOR MIPI INTERFACE

POWER ON：



POWER OFF：



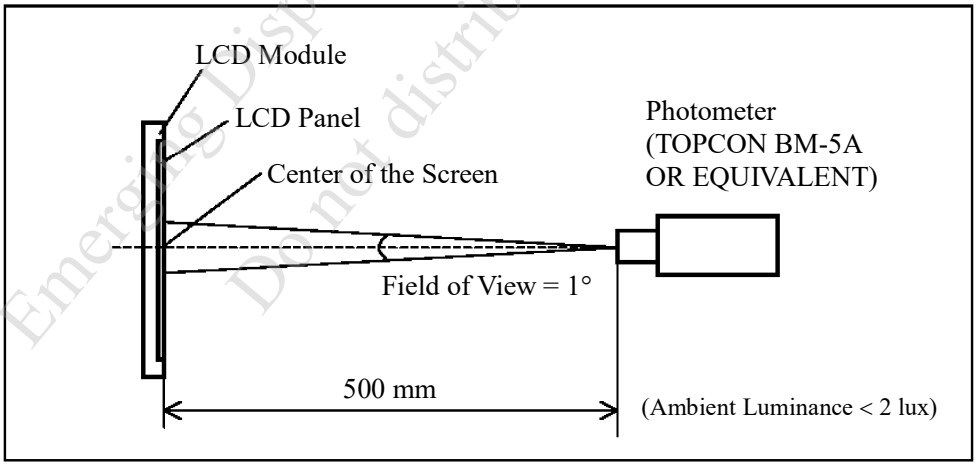
6. OPTICAL CHARACTERISTICS

6.1 OPTICAL CHARACTERISTICS

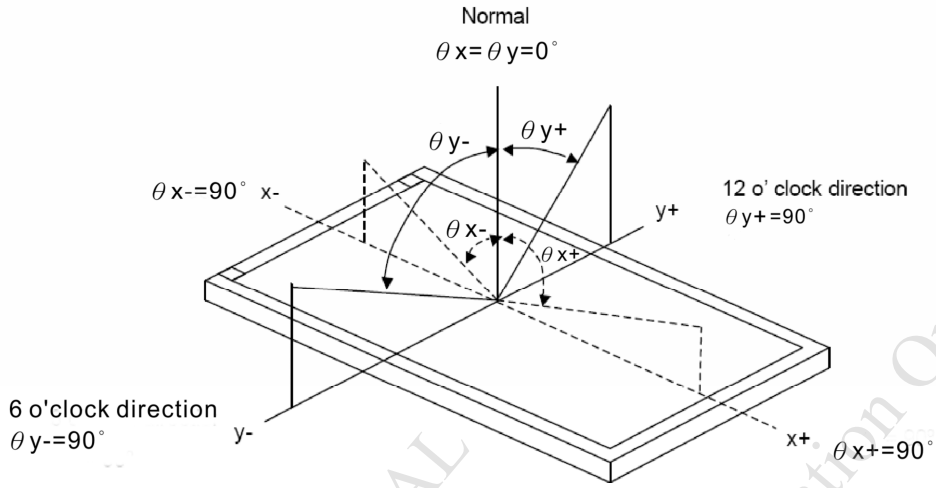
Ta = 25 ± 2 °C

ITEM		SYMBOL	CONDITION		MIN.	TYP.	MAX.	UNIT	REMARK
VIEWING ANGLE		θ_{y+}	CR ≥ 10	θ_x=0°	80	89	—	deg.	NOTE (2) NOTE (3)
		θ_{y-}			80	89	—		
		θ_{x+}		θ_y=0°	80	89	—		
		θ_{x-}			80	89	—		
CONTRAST RATIO (CENTER)		CR	θx=0° , θy=0°		700	850	—	—	NOTE (3)
RESPONSE TIME		$T_{R+}T_F$	θx=0° , θy=0°		—	30	35	ms	NOTE (4)
COLOR CHROMATICITY (CENTER)	WHITE	Wx	θx=0° , θy=0° VDD-VSS=3.3V ILED=92mA (NTSC : 50 %)		0.24	0.29	0.34	—	NOTE (5)
		Wy			0.25	0.30	0.35		
	RED	Rx			0.55	0.60	0.65	—	
		RY			0.30	0.35	0.40		
	GREEN	Gx			0.28	0.33	0.38	—	
		Gy			0.51	0.56	0.61		
	BLUE	Bx			0.10	0.15	0.20	—	
		By			0.05	0.10	0.15		
THE BRIGHTNESS OF MODULE(CENTER)		B			480	530	—	cd/m^2	NOTE (6)
THE UNIFORMITY OF MODULE		—			70	—	—	%	NOTE (7)

NOTE (1)：TEST CONDITION：
AFTER STABILIZING AND LEAVING THE PANEL ALONE AT A GIVEN TEMPERATURE FOR 30 MINUTES. MEASUREMENT SHOULD BE EXECUTED IN A STABLE, WINDLESS, AND DARK ROOM.



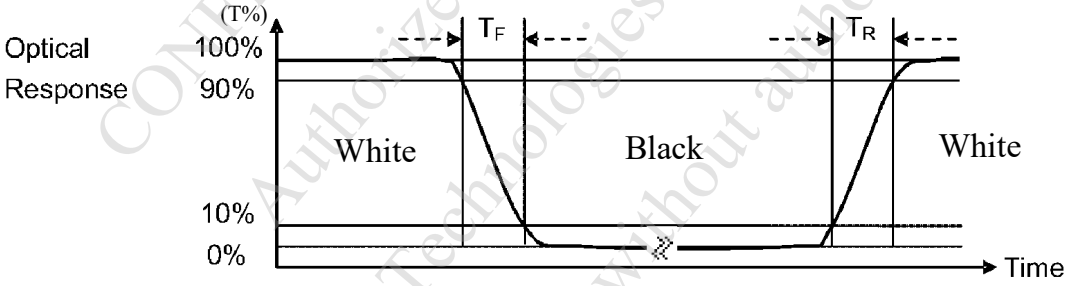
NOTE (2)：DEFINITION OF VIEWING ANGLE :



NOTE (3)：DEFINITION OF CONTRAST RATIO (CR) :
MEASURED AT THE CENTER POINT OF MODULE

$$\text{CONTRAST RATIO(CR)} = \frac{\text{BRIGHTNESS MEASURED WHEN LCD IS AT "WHITE STATE"}}{\text{BRIGHTNESS MEASURED WHEN LCD IS AT "BLACK STATE"}}$$

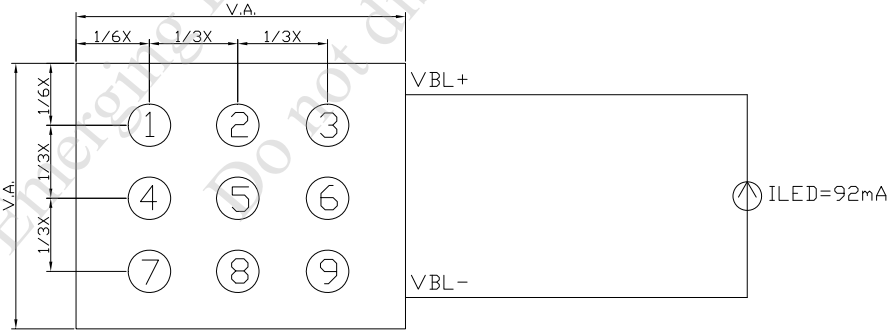
NOTE (4)：DEFINITION OF RESPONSE TIME : T_R AND T_F
THE FIGURE BELOW IS THE OUTPUT SIGNAL OF THE PHOTO DETECTOR.



NOTE (5)：DEFINITION OF COLOR CHROMATICITY
(a)100% RGB PIXEL DATA TRANSMISSION WHEN ALL THE INPUT TERMINALS OF MODULE ARE ELECTRICALLY POWERED ON.
(b)MEASURED AT THE CENTER POINT OF MODULE

NOTE (6)：MEASURED THE BRIGHTNESS OF WHITE STATE AT CENTER POINT.

NOTE (7)：(a)DEFINITION OF BRIGHTNESS UNIFORMITY

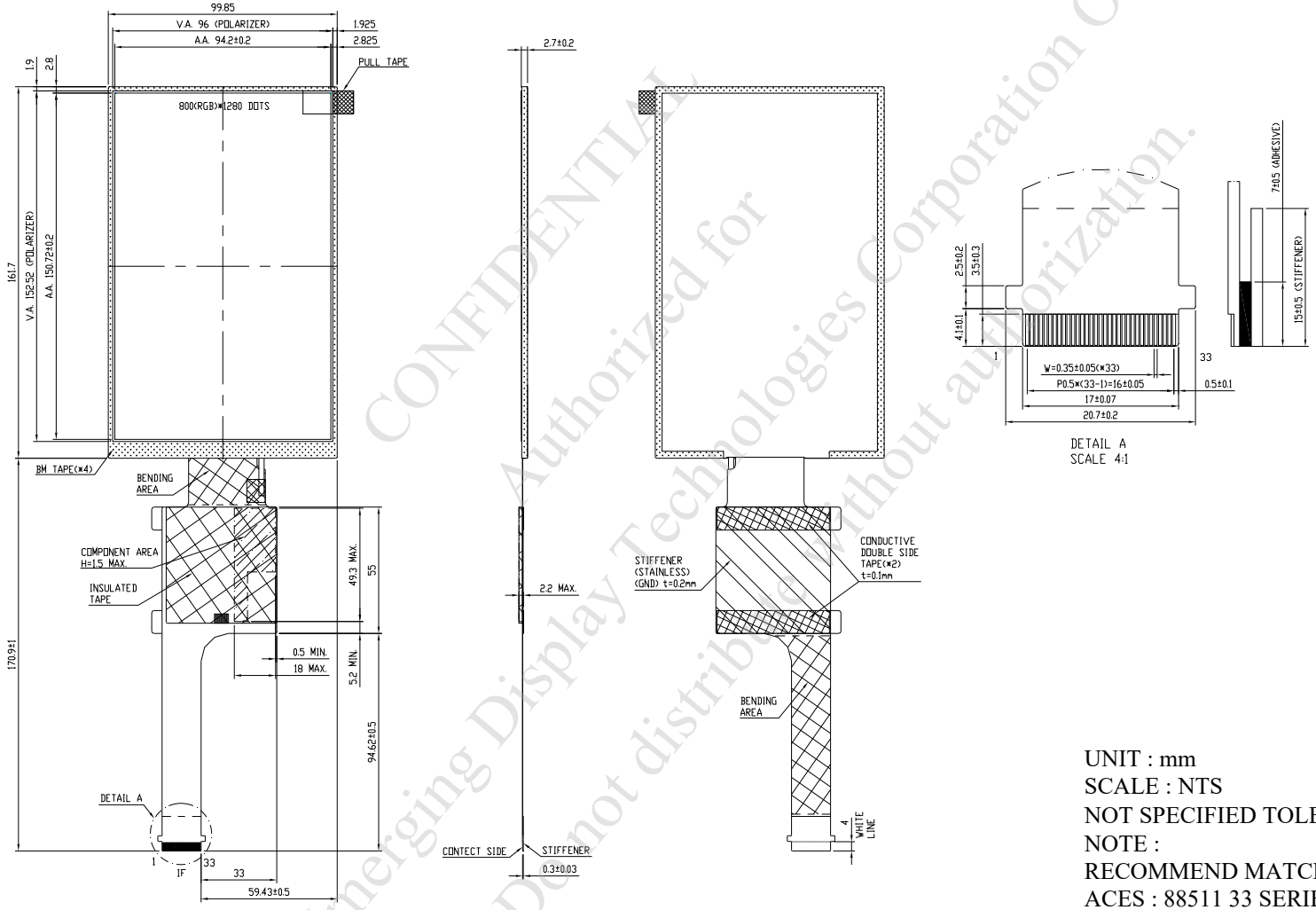


UNIT：mm

(b)THE BRIGHTNESS UNIFORMITY CALCULATING METHOD

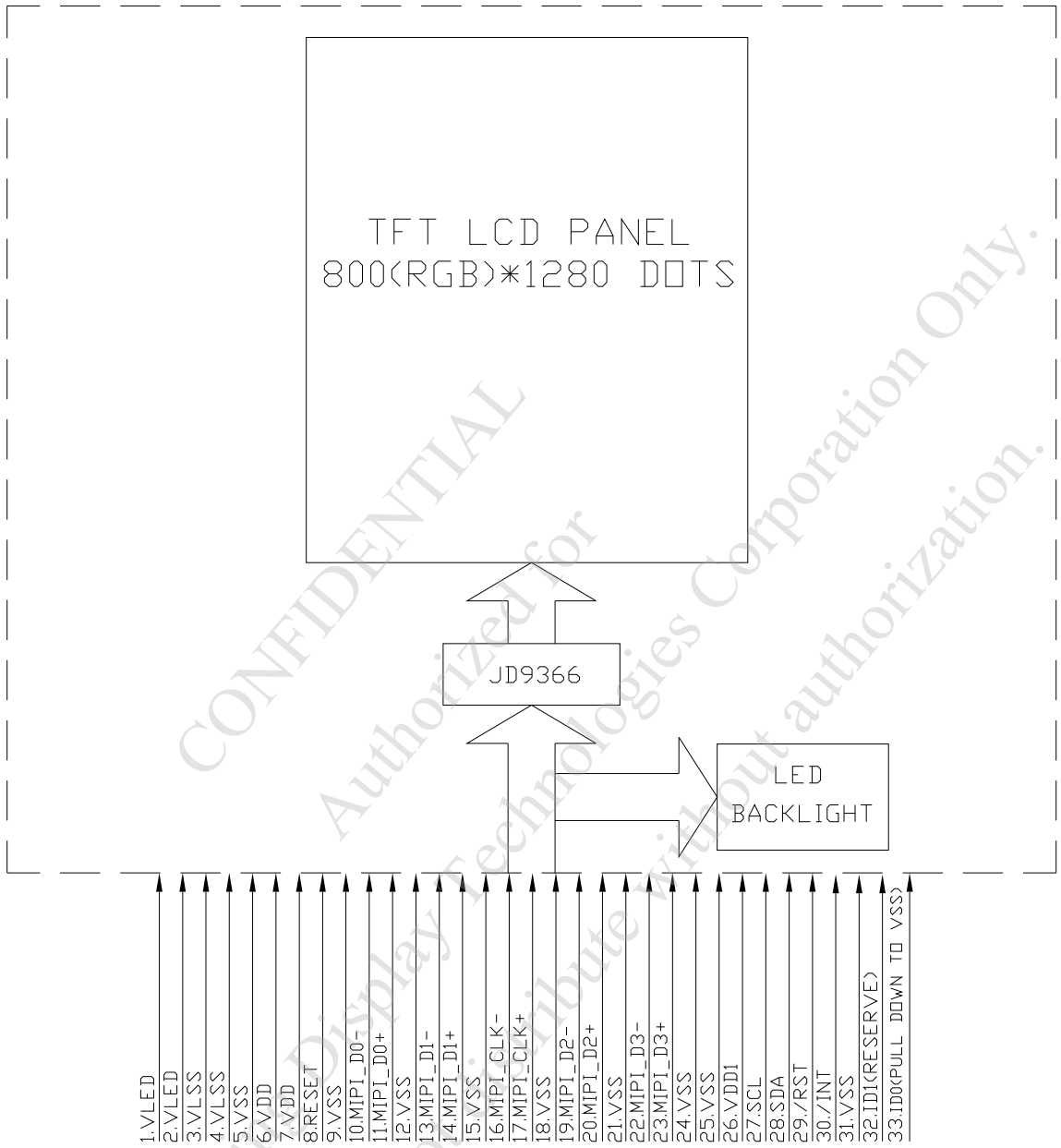
$$\text{UNIFORMITY}：\frac{\text{MINIMUM BRIGHTNESS}}{\text{MAXIMUM BRIGHTNESS}} * 100\%$$

7. OUTLINE DIMENSIONS



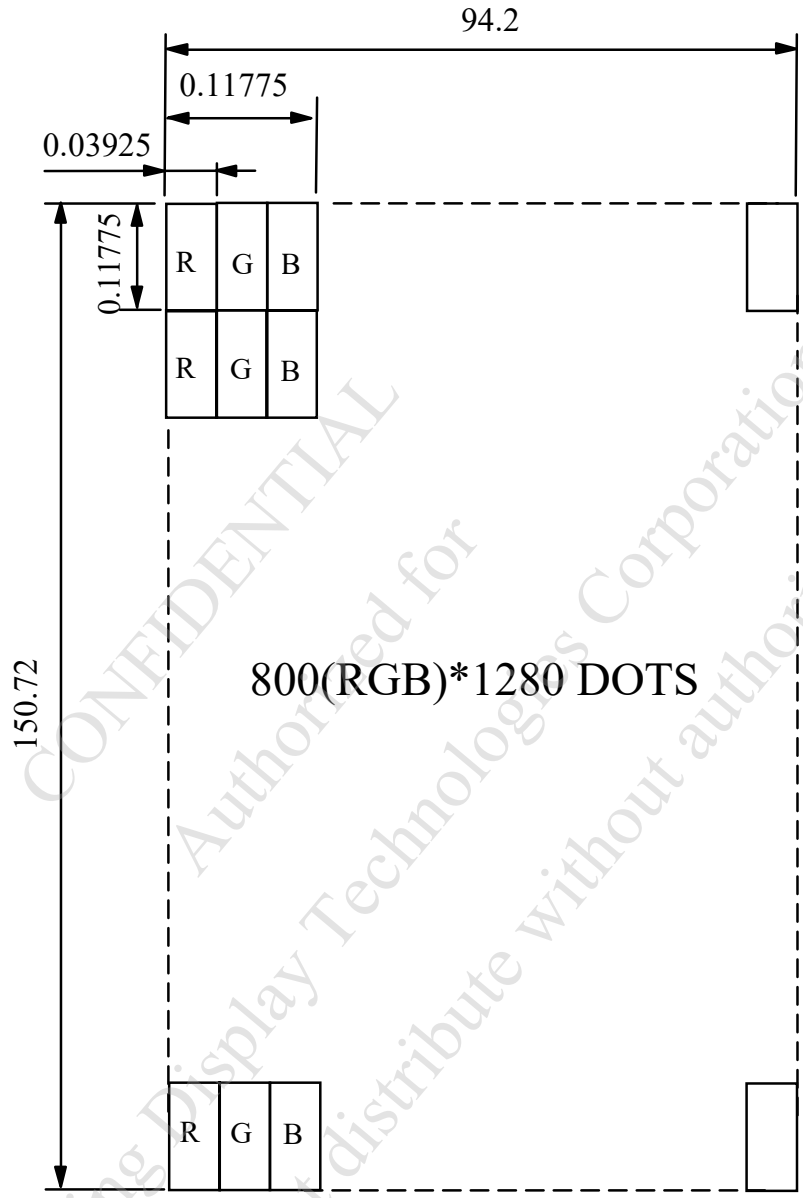
UNIT : mm
SCALE : NTS
NOT SPECIFIED TOLERANCE IS ± 0.5
NOTE :
RECOMMEND MATCH CONNECTOR
ACES : 88511 33 SERIES

8. BLOCK DIAGRAM



NOTE：PULL LOW RESISTOR：10KΩ

9. DETAIL DRAWING OF DOT MATRIX



UNIT : mm
SCALE : NTS
NOT SPECIFIED TOLERANCE IS ± 0.1
DOTS MATRIX TOLERANCE IS ± 0.01

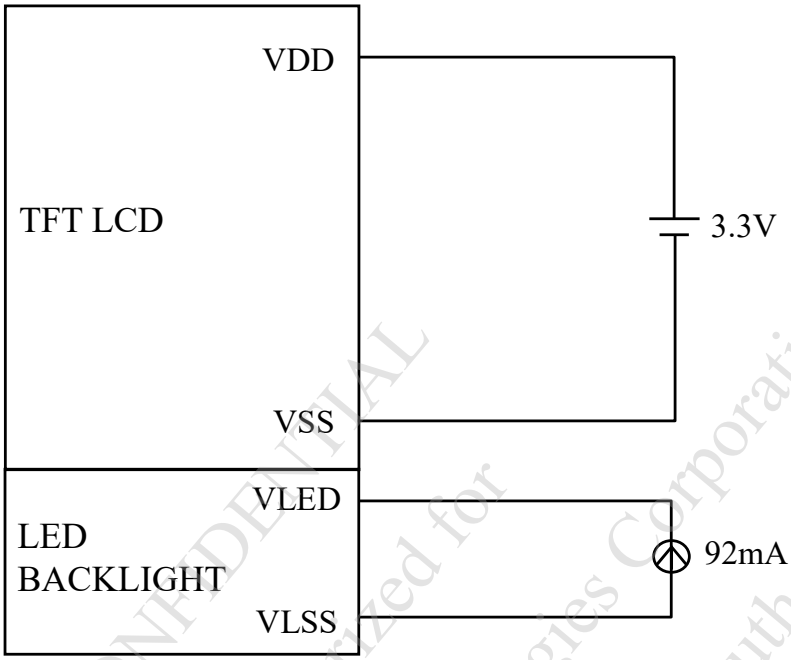
10. INTERFACE SIGNALS

10.1 TFT MODULE INTERFACE

NO.	SYMBOL	FUNCTION
1	VLED	LED BACKLIGHT ANODE
2	VLED	LED BACKLIGHT ANODE
3	VLSS	LED BACKLIGHT CATHODE
4	VLSS	LED BACKLIGHT CATHODE
5	VSS	TFT POWER GROUND
6	VDD	POWER SUPPLY VOLTAGE FOR LCD
7	VDD	POWER SUPPLY VOLTAGE FOR LCD
8	RESET	RESET LOW IS ACTIVE. NORMALLY PULLED HIGH.
9	VSS	TFT POWER GROUND
10	MIPI_D0-	MIPI DATA LANE0 INPUT (NEGATIVE)
11	MIPI_D0+	MIPI DATA LANE0 INPUT (POSITIVE)
12	VSS	TFT POWER GROUND
13	MIPI_D1-	MIPI DATA LANE1 INPUT (NEGATIVE)
14	MIPI_D1+	MIPI DATA LANE1 INPUT (POSITIVE)
15	VSS	TFT POWER GROUND
16	MIPI_CLK-	MIPI CLK INPUT (NEGATIVE)
17	MIPI_CLK+	MIPI CLK INPUT (POSITIVE)
18	VSS	TFT POWER GROUND
19	MIPI_D2-	MIPI DATA LANE2 INPUT (NEGATIVE)
20	MIPI_D2+	MIPI DATA LANE2 INPUT (POSITIVE)
21	VSS	TFT POWER GROUND
22	MIPI_D3-	MIPI DATA LANE3 INPUT (NEGATIVE)
23	MIPI_D3+	MIPI DATA LANE3 INPUT (POSITIVE)
24	VSS	TFT POWER GROUND
25	NC	NO CONNECTION
26	NC	NO CONNECTION
27	NC	NO CONNECTION
28	NC	NO CONNECTION
29	NC	NO CONNECTION
30	NC	NO CONNECTION
31	NC	NO CONNECTION
32	NC	NO CONNECTION
33	NC	NO CONNECTION

11. POWER SUPPLY

11.1 POWER SUPPLY FOR LCM



12. INSPECTION CRITERIA

12.1 APPLICATION

THIS INSPECTION STANDARD IS TO BE APPLIED TO THE LCD MODULE DELIVERED FROM EMERGING DISPLAY TECHNOLOGIES CORP.(E.D.T) TO CUSTOMERS

12.2 INSPECTION CONDITIONS

12.2.1 (1)OBSERVATION DISTANCE：45±5cm

(2)VIEWING ANGLE：±45°

±45° (FOR SECTION WITHIN VIEWING AREA), REFER TO FIG.A

90° (FOR SECTION OUTSIDE OF VIEWING AREA), REF TO FIG.B

PERPENDICULAR TO MODULE SURFACE

VIEWING ANGLE SHOULD BE SMALLER THAN 45°

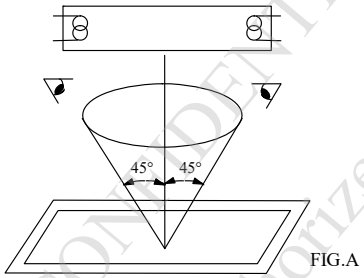


FIG.A

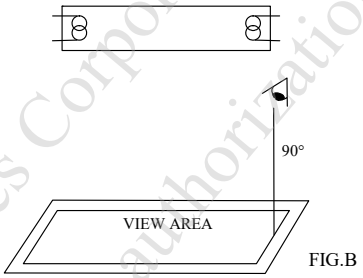


FIG.B

THE INSPECTION CRITERIA IS ACCORDING TO LINE OF SIGHT. INSPECTION SHALL BE MADE WITHIN THE HALF SECTION OF THE VIEWING CONE GENERATED BY LINE SEGMENT OF 45° WITH RESPECT TO THE VERTICAL AXIS FROM CENTER VERTEX OF LCD, THE FLUORESCENT LAMP AND THE CONE AXIS MUST BE PERPENDICULAR TO THE LCD SURFACE.

IF THE DEFECTS ARE OUTSIDE OF VIEWING AREA, IT SHALL BE INSPECTED BY 90° WITH RESPECT TO THE VERTICAL AXIS FROM EDGE OF VIEWING AREA.

12.2.2 ENVIRONMENT CONDITIONS：

AMBIENT TEMPERATURE		25±5°C
AMBIENT HUMIDITY		65 ± 20%RH
AMBIENT ILLUMINATION	COSMETIC INSPECTION	600~800 lux
	FUNCTIONAL INSPECTION	300~500 lux
INSPECTION TIME		15 secs

12.2.3 INSPECTION LOT

QUANTITY PER DELIVERY LOT FOR EACH MODEL

12.2.4 A SAMPLING INSPECTION SHALL BE MADE ACCORDING TO THE FOLLOWING PROVISIONS TO JUDGE THE ACCEPTABILITY

(a)APPLICABLE STANDARD：

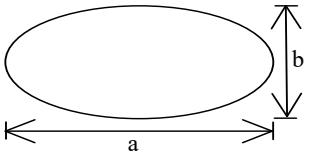
ANSI/ ASQ Z1.4 NORMAL INSPECTION LEVEL II

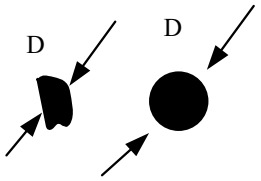
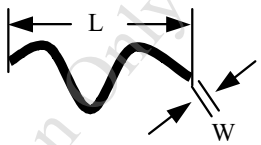
(b)AQL：MAJOR DEFECT：AQL 0.65

MINOR DEFECT：AQL 1.0

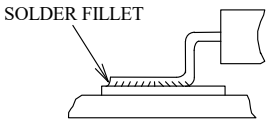
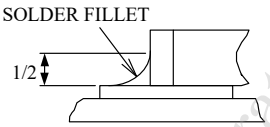
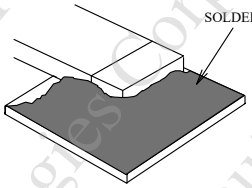
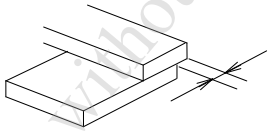
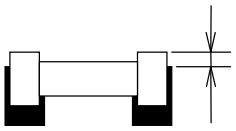
12.3 DEFECTS CLASSIFICATION

TYPE OF DEFECT	INSPECTION ITEM	DEFECT FEATURE	AQL
MAJOR DEFECT	1.DISPLAY ON	• DEFECT TO MISS SPECIFIED DISPLAY FUNCTION, FOR ALL AND SPECIFIED DOTS EX: DISCONNECTION, SHORT CIRCUIT ETC	0.65
	2.BACKLIGHT	• NO LIGHT • FLICKERING AND OTHER ABNORMAL ILLUMINATION	
	3.DIMENSIONS	• SUBJECT TO INDIVIDUAL ACCEPTANCE SPECIFICATIONS	
MINOR DEFECT	1.DISPLAY ZONE (VIEWING AREA)	• BLACK/WHITE SPOT / CIRCULAR TYPE • BUBBLES ON POLARIZER • NEWTON RING • BLACK/WHITE LINE / LINEAR TYPE • SCRATCH • CONTAMINATION • UNEVEN COLOR SPREAD	1.0
	2.BEZEL ZONE	• STAINS • SCRATCHES • FOREIGN MATTER	
	3.SOLDERING	• INSUFFICIENT SOLDER • SOLDERED IN INCORRECT POSITION • CONVEX SOLDERING SPOT • SOLDER BALLS • SOLDER SCRAPS	
	4.DISPLAY ON (ALL ON)	• LIGHT LINE	

<table>
<tr><th>NO.</th><th>ITEM</th><th>CRITERIA</th></tr>
<tr><td>1</td><td>DISPLAY ON INSPECTION</td><td>1. INCORRECT PATTERN
2. MISSING SEGMENT
3. DIM SEGMENT
4. OPERATING VOLTAGE BEYOND SPEC</td></tr>
<tr><td>2</td><td>OVERALL DIMENSIONS</td><td>1. OVERALL DIMENSION BEYOND SPEC</td></tr>
<tr><td>3</td><td>DOT DEFECT</td><td>1. INSPECTION PATTERN: FULL WHITE, FULL BLACK, RED, GREEN AND BLUE SCREENS.
2.
<table>
<tr><th>ITEMS</th><th>ACCEPTABLE COUNT</th></tr>
<tr><td>BRIGHT DOT</td><td>N ≤ 3</td></tr>
<tr><td>DARK DOT</td><td>N ≤ 5</td></tr>
<tr><td>TOTAL BRIGHT AND DARK DOTS</td><td>N ≤ 5</td></tr>
</table>
NOTE：
1. THE DEFINITION OF DOT：
THE SIZE OF A DEFECTIVE DOT OVER 1/2 OF WHOLE DOT IS REGARDED AS ONE DEFECTIVE DOT.
2. BRIGHT DOT：
DOTS APPEAR BRIGHT AND UNCHANGED IN SIZE IN WHICH LCD PANEL IS DISPLAYING UNDER BLACK PATTERN.
THE BRIGHT DOT DEFECT MUST BE VISIBLE THROUGH 5% ND FILTER.
3. DARK DOT：
DOTS APPEAR DARK AND UNCHANGED IN SIZE IN WHICH LCD PANEL IS DISPLAYING UNDER PURE RED, GREEN, BLUE PICTURE.</td></tr>
<tr><td>4</td><td>BUBBLES ON POLARIZER /SURFACE STAINS /DIRT/CF FAIL/SPOT</td><td>
<table>
<tr><th></th><th>AVERAGE DIAMETER (mm)：D</th><th>NUMBER OF PIECES PERMITTED</th></tr>
<tr><td rowspan="3">BUBBLE ON THE POLARIZER</td><td>D ≤ 0.25</td><td>LGNORE</td></tr>
<tr><td>0.25 < D ≤ 0.5</td><td>N ≤ 5</td></tr>
<tr><td>0.5 < D</td><td>NONE</td></tr>
<tr><td rowspan="3">SURFACE STAINS</td><td>D < 0.1</td><td>IGNORE</td></tr>
<tr><td>0.1 < D ≤ 0.3</td><td>N ≤ 3</td></tr>
<tr><td>0.3 < D</td><td>NONE</td></tr>
<tr><td rowspan="3">CF FAIL / SPOT</td><td>D < 0.1</td><td>IGNORE</td></tr>
<tr><td>0.1 < D ≤ 0.3</td><td>N ≤ 3</td></tr>
<tr><td>0.3 < D</td><td>NONE</td></tr>
</table>
NOTE : (1)POLARIZER BUBBLE IS DEFINED AS THE BUBBLE APPEARS ON ACTIVE DISPLAY AREA. THE DEFECT OF POLARIZER BUBBLE SHALL BE IGNORED IF THE POLARIZER BUBBLE APPEARS ON THE OUTSIDE OF ACTIVE DISPLAY AREA.
(2)THE EXTRANEOUS SUBSTANCE IS DEFINED AS IT CAN BE OBSERVED WHEN THE MODULE IS POWER ON.
(3)THE DEFINITION OF AVERAGE DIAMETER, D IS DEFINED AS FOLLOWING.
AVERAGE DIAMETER (D)=(a+b)/2
 
</td></tr>
</table>

<table>
<tr><th>NO.</th><th>ITEM</th><th>CRITERIA</th></tr>
<tr><td>5</td><td>BLACK/WHITE SPOT CIRCULAR TYPE</td><td>THE FOLLOWING BLACK/WHITE SPOT ARE WITHIN THE VIEWING AREA. AVERAGE DIAMETER：D (mm)
<table>
<tr><th>SIZE D</th><th>PERMISSIBLE NO.</th></tr>
<tr><td>D≤0.1</td><td>IGNORE</td></tr>
<tr><td>0.1<D≤0.5</td><td>6</td></tr>
<tr><td>D>0.5</td><td>0</td></tr>
</table>
NOTE (1)：THE DISTANCE BETWEEN DEFECTS SHOULD BE MORE THAN 10mm APART.

</td></tr>
<tr><td>6</td><td>SCRATCH</td><td>THE FOLLOWING SCRATCH IS WITHIN THE VIEWING AREA. WIDTH：W (mm) , LENGTH : L (mm)
<table>
<tr><th>SIZE W & L</th><th>PERMISSIBLE NO.</th></tr>
<tr><td>W≤0.05</td><td>IGNORE</td></tr>
<tr><td>0.05<W≤0.1, L≤8</td><td>5</td></tr>
<tr><td>W>0.1 OR L>8</td><td>0</td></tr>
</table>
NOTE (1)：THE DISTANCE BETWEEN DEFECTS SHOULD BE MORE THAN 10mm APART.

</td></tr>
<tr><td>7</td><td>BLACK / WHITE LINE LINEAR TYPE / FOREIGN FIBER</td><td>THE FOLLOWING BLACK LINE, WHITE LINE IS WITHIN THE VIEWING AREA. WIDTH：W (mm) , LENGTH : L (mm)
<table>
<tr><th>SIZE W & L</th><th>PERMISSIBLE NO.</th></tr>
<tr><td>W≤0.05</td><td>IGNORE</td></tr>
<tr><td>0.05<W≤0.1, L≤8</td><td>5</td></tr>
<tr><td>W>0.1 OR L>8</td><td>0</td></tr>
</table>
NOTE (1)：THE DISTANCE BETWEEN DEFECTS SHOULD BE MORE THAN 10mm APART.

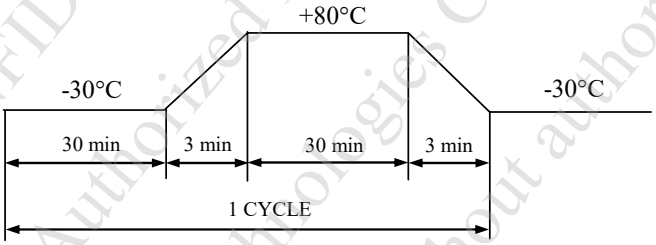
</td></tr>
<tr><td>8</td><td>CRACKED GLASS</td><td>NOT ACCEPTABLE</td></tr>
<tr><td>9</td><td>LINE DEFECT ON DISPLAY</td><td>OBVIOUS VERTICAL OR HORIZONTAL LINE DEFECT IS NOT ALLOWED</td></tr>
<tr><td>10</td><td>MURA ON DISPLAY</td><td>IT’S OK IF MURA IS SLIGHT VISIBLE THROUGH 2% ND FILTER</td></tr>
<tr><td>11</td><td>UNEVEN COLOR SPREAD, COLORATION</td><td>TO BE DETERMINED BASED UPON THE LIMITED SAMPLE.</td></tr>
<tr><td>12</td><td>BEZEL APPEARANCE</td><td>1. BEZEL MAY NOT HAVE RUST, BE DEFORMED OR HAVE FINGER PRINTS STAINS OF OTHER CONTAMINATION.
2. BEZEL MUST COMPLY WITH JOB SPECIFICATIONS.</td></tr>
<tr><td>13</td><td>PCB</td><td>1. THERE MAY NOT BE MORE THAN 2mm OF SEALANT OUTSIDE THE SEAL AREA ON THE PCB, AND THERE SHOULD BE NO MORE THAN THREE PLACES.
2. NO OXIDATION OR CONTAMINATION PCB TERMINALS.
3. PARTS ON PCB MUST BE THE SAME AS ON THE PRODUCTION CHARACTERISTIC CHART.
THERE SHOULD BE NO WRONG PARTS, MISSING PARTS OR EXCESS PARTS.
4. THE JUMPER ON THE PCB SHOULD CONFORM TO THE PRODUCT CHARACTERISTIC CHART.
5. IF SOLDER GETS ON BEZEL TAB PADS, LED PAD, ZEBRA PAD OR SCREW HOLD PAD; MAKE SURE IT IS SMOOTHED DOWN.</td></tr>
</table>

NO.	ITEM	CRITERIA
14	SOLDERING	1. NO SOLDERING FOUND ON THE SPECIFIED PLACE 2. INSUFFICIENT SOLDER (a)LSI, IC A POOR WETTING OF SOLDER IS BETWEEN LOWER BEND OR "HEEL" OF LEAD AND PAD  (b)CHIP COMPONENT · SOLDER IS LESS THAN 50% OF SIDES AND FRONT FACE WETTING  · SOLDER WETS 3 SIDES OF TERMINAL, BUT LESS THAN 25% OF SIDES AND FRONT SURFACE AREA ARE COVERED  3. PARTS ALIGNMENT (a)LSI, IC LEAD WIDTH IS MORE THAN 50% BEYOND PAD OUTLINE  (b)CHIP COMPONENT COMPONENT IS OFF CENTER, AND MORE THAN 50% OF THE LEADS IS OFF THE PAD OUTLINE  4. NO UNMELTED SOLDER PASTE MAY BE PRESENT ON THE PCB. 5. NO COLD SOLDER JOINTS, MISSING SOLDER CONNECTIONS, OXIDATION OR ICICLE. 6. NO RESIDUE OR SOLDER BALLS ON PCB. 7. NO SHORT CIRCUITS IN COMPONENTS ON PCB.

NO.	ITEM	CRITERIA
15	BACKLIGHT	1. NO LIGHT 2. FLICKERING AND OTHER ABNORMAL ILLUMINATION 3. SPOTS OR SCRATCHES THAT APPEAR WHEN LIT MUST BE JUDGED USING LCD SPOT, LINES AND CONTAMINATION STANDARDS. 4. BACKLIGHT DOESN'T LIGHT OR COLOR IS WRONG.
16	GENERAL APPEARANCE	1. NO OXIDATION, CONTAMINATION, CURVES OR, BENDS ON INTERFACE PIN (OLB) OF TCP. 2. NO CRACKS ON INTERFACE PIN (OLB) OF TCP. 3. NO CONTAMINATION, SOLDER RESIDUE OR SOLDER BALLS ON PRODUCT. 4. THE IC ON THE TCP MAY NOT BE DAMAGED, CIRCUITS. 5. THE UPPERMOST EDGE OF THE PROTECTIVE STRIP ON THE INTERFACE PIN MUST BE PRESENT OR LOOK AS IF IT CAUSE THE INTERFACE PIN TO SEVER. 6. THE RESIDUAL ROSIN OR TIN OIL OF SOLDERING (COMPONENT OR CHIP COMPONENT) IS NOT BURNED INTO BROWN OR BLACK COLOR. 7. SEALANT ON TOP OF THE ITO CIRCUIT HAS NOT HARDENED. 8. PIN TYPE MUST MATCH TYPE IN SPECIFICATION SHEET. 9. LCD PIN LOOSE OR MISSING PINS. 10. PRODUCT PACKAGING MUST BE THE SAME AS SPECIFIED ON PACKAGING SPECIFICATION SHEET. 11. PRODUCT DIMENSION AND STRUCTURE MUST CONFORM TO PRODUCT SPECIFICATION SHEET. 12. THE APPEARANCE OF HEAT SEAL SHOULD NOT ADMIT ANY DIRT AND BREAK.

13. RELIABILITY TEST

13.1 STANDARD SPECIFICATIONS FOR RELIABILITY OF LCD MODULE

NO.	ITEM	DESCRIPTION
1	HIGH TEMPERATURE OPERATION	THE SAMPLE SHOULD BE ALLOWED TO STAND AT +70°C FOR 240 HRS
2	LOW TEMPERATURE OPERATION	THE SAMPLE SHOULD BE ALLOWED TO STAND AT -20°C FOR 240 HRS
3	HIGH TEMPERATURE STORAGE	THE SAMPLE SHOULD BE ALLOWED TO STAND AT +80°C FOR 240 HRS
4	LOW TEMPERATURE STORAGE	THE SAMPLE SHOULD BE ALLOWED TO STAND AT -30°C FOR 240 HRS
5	HIGH TEMPERATURE / HUMIDITY TEST STORAGE	THE SAMPLE SHOULD BE ALLOWED TO STAND AT 60°C, 90% RH 240 HRS
6	THERMAL SHOCK (NOT OPERATED)	THE SAMPLE SHOULD BE ALLOWED TO STAND THE FOLLOWING 10 CYCLES OF OPERATION: 
7	ESD (ELECTROSTATIC DISCHARGE) (NOT OPERATED)	AIR DISCHARGE ± 12KV CONTACT DISCHARGE ± 8KV ACCORDING TO IEC-61000-4-2

NOTE (1) : THE TEST SAMPLES HAVE RECOVERY TIME FOR 2 HOURS AT ROOM TEMPERATURE BEFORE THE FUNCTION CHECK. IN THE STANDARD CONDITIONS, THERE IS NO DISPLAY FUNCTION NG ISSUE OCCURRED.

13.2 TESTING CONDITIONS AND INSPECTION CRITERIA

FOR THE FINAL TEST THE TESTING SAMPLE MUST BE STORED AT ROOM TEMPERATURE FOR 24 HOURS, AFTER THE TESTS LISTED IN TABLE 15.1, STANDARD SPECIFICATIONS FOR RELIABILITY HAVE BEEN EXECUTED IN ORDER TO ENSURE STABILITY.

NO.	ITEM	TEST MODEL	INSPECTION CRITERIA
1	CURRENT CONSUMPTION	REFER TO SPECIFICATION	THE CURRENT CONSUMPTION SHOULD CONFORM TO THE PRODUCT SPECIFICATION.
2	CONTRAST	REFER TO SPECIFICATION	AFTER THE TESTS HAVE BEEN EXECUTED, THE CONTRAST MUST BE LARGER THAN HALF OF ITS INITIAL VALUE PRIOR TO THE TESTS.
3	APPEARANCE	VISUAL INSPECTION	DEFECT FREE

14. CAUTION

14.1 OPERATION

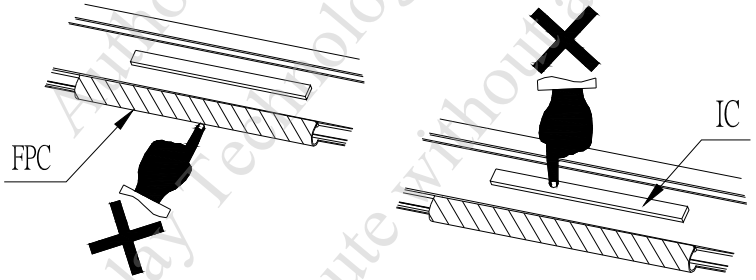
14.1.1 DO NOT CONNECT OR DISCONNECT MODULES TO OR FROM THE MAIN SYSTEM WHILE POWER IS BEING SUPPLIED .

14.1.2 USE THE MODULE WITHIN SPECIFIED TEMPERATURE ; LOWER TEMPERATURE CAUSES THE RETARDATION OF BLINKING SPEED OF THE DISPLAY ; HIGHER TEMPERATURE MAKES OVERALL DISPLAY DISCOLOR . WHEN THE TEMPERATURE RETURNS TO NORMALITY, THE DISPLAY WILL OPERATE NORMALLY.

14.1.3 ADJUST THE LC DRIVING VOLTAGE TO OBTAIN THE OPTIMUM CONTRAST .

14.1.4 POWER ON SEQUENCE INPUT SIGNALS SHOULD NOT BE SUPPLIED TO LCD MODULE BEFORE POWER SUPPLY VOLTAGE IS APPLIED AND REACHES THE SPECIFIED VALUE.
IF ABOVE SEQUENCE IS NOT FOLLOWED , CMOS LSIS OF LCD MODULES MAY BE DAMAGED DUE TO LATCH - UP PROBLEM.

14.1.5 NOT ALLOWED TO INFLICT ANY EXTERNAL STRESS AND TO CAUSE ANY MECHANICAL INTERFERENCE ON THE BENDING AREA OF FPC DURING THE TAIL BENDING BACKWARDS!
DO NOT STRESS FPC AND IC ON THE MODULE!



14.2 NOTICE

14.2.1 USE A GROUNDED SOLDERING IRON WHEN SOLDERING CONNECTOR I/O TERMINALS . FOR SOLDERING OR REPAIRING, TAKE PRECAUTION AGAINST THE TEMPERATURE OF THE SOLDERING IRON AND THE SOLDERING TIME TO PREVENT PEELING OFF THE THROUGH-HOLE-PAD .

14.2.2 DO NOT DISASSEMBLE . EDT SHALL NOT BE HELD RESPONSIBLE IF THE MODULE IS DISASSEMBLED AND UPON THE REASSEMBLY THE MODULE FAILED.

14.2.3 DO NOT CHARGE STATIC ELECTRICITY, AS THE CIRCUIT OF THIS MODULE CONTAINS CMOS LSIS. A WORKMAN'S BODY SHOULD ALWAYS BE STATIC-PROTECTED BY USE OF AN ESD STRAP. WORKING CLOTHES FOR SUCH PERSONNEL SHOULD BE OF STATIC-PROTECTED MATERIAL.

14.2.4 ALWAYS GROUND THE ELECTRICALLY-POWERED DRIVER BEFORE USING IT TO INSTALL THE LCD MODULE. WHILE CLEANING THE WORK STATION BY VACUUM CLEANER, DO NOT BRING THE SUCKING MOUTH NEAR THE MODULE ; STATIC ELECTRICITY OF THE ELECTRICALLY-POWERED DRIVER OR THE VACUUM CLEANER MAY DESTROY THE MODULE.

14.2.5 DON’T GIVE EXTERNAL SHOCK.

14.2.6 DON’T APPLY EXCESSIVE FORCE ON THE SURFACE.

14.2.7 LIQUID IN LCD IS HAZARDOUS SUBSTANCE. MUST NOT LICK AND SWALLOW.
WHEN THE LIQUID IS ATTACH TO YOUR, SKIN, CLOTH ETC. WASH IT OUT THOROUGHLY AND IMMEDIATELY.

14.2.8 DON’T OPERATE IT ABOVE THE ABSOLUTE MAXIMUM RATING.

14.2.9 STORAGE IN A CLEAN ENVIRONMENT, FREE FROM DUST, ACTIVE GAS, AND SOLVENT.

14.2.10 STORE WITHOUT ANY PHYSICAL LOAD.

14.2.11 REWIRING: NO MORE THAN 3 TIMES.