



# 12.48 inch E-paper Display Series



**GDEW1248Z95**

Dalian Good Display Co., Ltd.

## Revision History

<b>Rev.</b>	<b>Issued Date</b>	<b>Revised Contents</b>
1.0	Apr.02.2018	1. Preliminary
1.1	Aug.22.2018	1. In part 7-4): Modify Reference Circuit.
1.2	Aug.07.2020	1. In part 7-4): Modify Reference Circuit.

## ***TECHNICAL SPECIFICATION***

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## 1. Over View

The display is a TFT active matrix electrophoretic display, with interface and a reference system design. The 12.48” active area contains 984×1304 pixels, and has 1-bit white/black and 1-bit red full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM, and border are supplied with each panel.

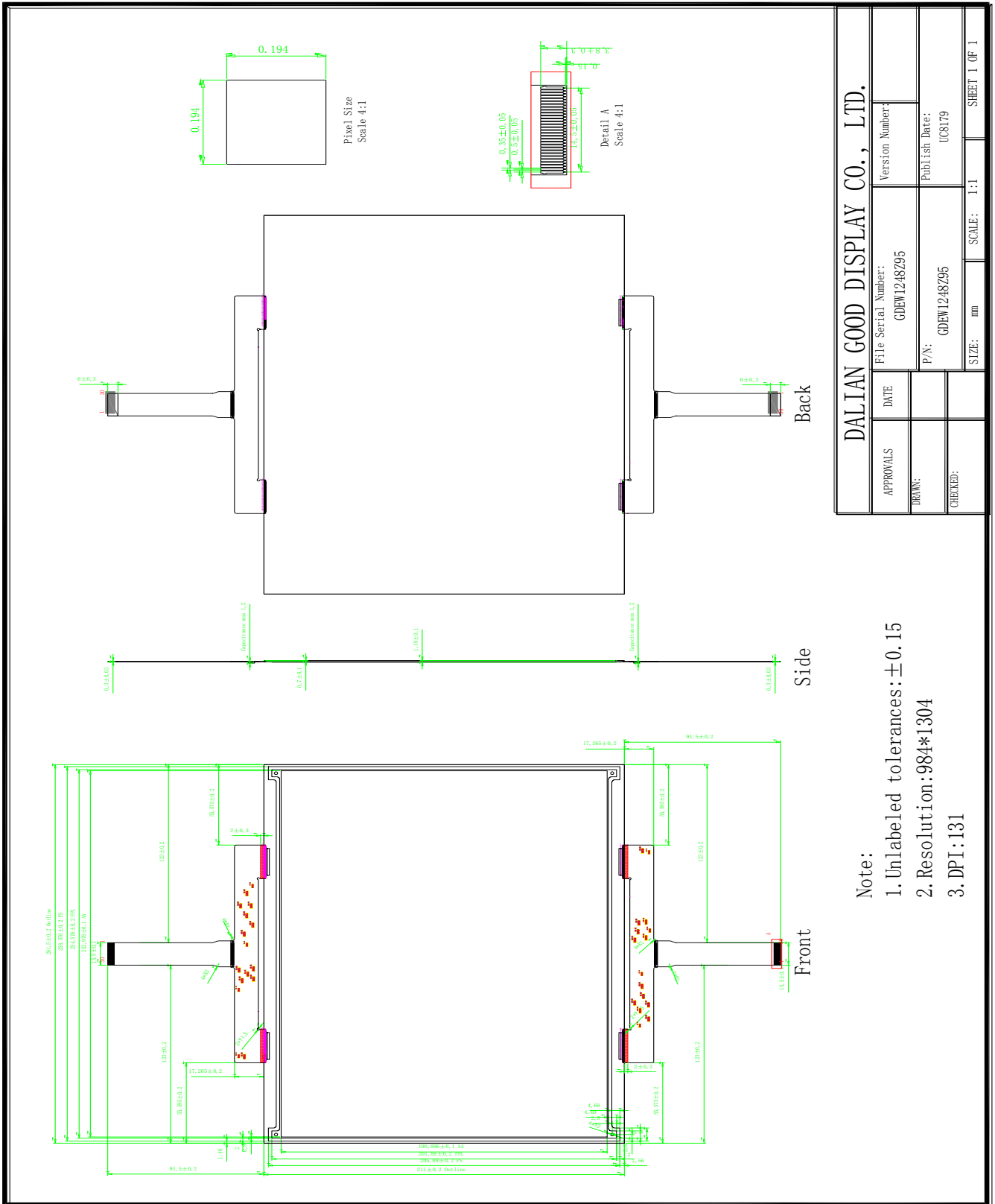
## 2. Features

- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- Landscape, portrait mode
- Antiglare hard-coated front-surface
- Low current deep sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and source driving voltage
- I<sup>2</sup>C Signal Master Interface to read external temperature sensor
- Available in COG package IC thickness 300um

## 3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	12.48	Inch	
Display Resolution	1304(H)×984(V)	Pixel	Dpi: 131
Active Area	252.976(H)×190.896(V)	mm	
Pixel Pitch	0.194×0.194	mm	
Pixel Configuration	Square		
Outline Dimension	261.5(H)×211(V) ×1.18(D)	mm	
Weight	132	g	

4. Mechanical Drawing of EPD module



DALIAN GOOD DISPLAY CO., LTD.

APPROVALS	DATE	File Serial Number: GDEW1248Z95	Version Number:
DRAWN:		P/N: GDEW1248Z95	Publish Date: 10/8/19
CHECKED:		SIZE: mm	SCALE: 1:1
			SHEET 1 OF 1

Note:  
 1. Unlabeled tolerances: ±0.15  
 2. Resolution: 984\*1304  
 3. DPI: 131

## 5. Input/Output Terminals

### 5-1) Pin out List

FPC-1 pin out list

Pin #	Type	Single	Description	Remark
1	I	CSB_M1	Serial communication chip select	Note 5-1
2	O	GDR_M1	This pin is N-MOS gate control	
3	P	RESE_M1	Current sense input for control loop	
4	P	VSHR_M1	Positive source voltage for Red	
5	O	TSCL	I <sup>2</sup> C clock for external temperature sensor	
6	I/O	TSDA	I <sup>2</sup> C data for external temperature sensor	
7	I	BS	Input interface setting. Select 3 wire/4 wire SPI interface	Note 5-5
8	O	BUSY_M1	This pin indicates the driver status	Note 5-4
9	I	RST	Global reset pin. Low reset	Note 5-3
10	I	DC	Serial communication Command/Data input	Note 5-2
11	I	CSB_S1	Serial communication chip select	Note 5-1
12	I	SCL	Serial communication clock input	
13	I/O	SDA	Serial communication data input	
14	I/O	LSYNC_M1	2+2 cascade sync signal	
15	I/O	M1M2_SYNC_M1	2+2 cascade sync signal	
16	I/O	M2M1_SYNC_M1	2+2 cascade sync signal	
17	P	VDDIO_M1	IO voltage supply	
18	P	VDD_M1	Digital/Analog power	
19	P	VSS_M1	Digital ground	
20	P	VDD_18V_M1	1.8V voltage input & output	
21	P	VOTP_M1	OTP program power (7.5V)	
22	P	VSH_M1	Positive source voltage	
23	P	VGH_M1	Positive gate voltage	
24	P	VSL_M1	Negative source voltage	
25	P	VGL_M1	Negative gate voltage	
26	O	VCOM_M1	VCOM output	
27	O	BUSY_S1	This pin indicates the driver status	Note 5-4
28	P	VSHR_S1	Positive source voltage for Red	
29	P	VSH_S1	Positive source voltage	
30	P	VSL_S1	Positive gate voltage	

## FPC-2 pin out list

Pin #	Type	Single	Description	Remark
1	I	CSB_S2	Serial communication chip select	Note 5-1
2	O	GDR_M2	This pin is N-MOS gate control	
3	P	RESE_M2	Current sense input for control loop	
4	P	VSHR_M2	Positive source voltage for Red	
5	O	TSCL	I <sup>2</sup> C clock for external temperature sensor	
6	I/O	TSDA	I <sup>2</sup> C data for external temperature sensor	
7	I	BS	Input interface setting. Select 3 wire/4 wire SPI interface	Note 5-5
8	O	BUSY_M2	This pin indicates the driver status	Note 5-4
9	I	RST	Global reset pin. Low reset	Note 5-3
10	I	DC	Serial communication Command/Data input	Note 5-2
11	I	CSB_M2	Serial communication chip select	Note 5-1
12	I	SCL	Serial communication clock input	
13	I/O	SDA	Serial communication data input	
14	I/O	LSYNC_M2	2+2 cascade sync signal	
15	I/O	M1M2_SYNC_M2	2+2 cascade sync signal	
16	I/O	M2M1_SYNC_M2	2+2 cascade sync signal	
17	P	VDDIO_M2	IO voltage supply	
18	P	VDD_M2	Digital/Analog power	
19	P	VSS_M2	Digital ground	
20	P	VDD_18V_M2	1.8V voltage input & output	
21	P	VOTP_M2	OTP program power (7.5V)	
22	P	VSH_M2	Positive source voltage	
23	P	VGH_M2	Positive gate voltage	
24	P	VSL_M2	Negative source voltage	
25	P	VGL_M2	Negative gate voltage	
26	O	VCOM_M2	VCOM output	
27	O	BUSY_S2	This pin indicates the driver status	Note 5-4
28	P	VSHR_S2	Positive source voltage for Red	
29	P	VSH_S2	Positive source voltage	
30	P	VSL_S2	Positive gate voltage	

Note 5-1: This pin (CSB) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled Low.

Note 5-2: This pin (DC) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled Low, the data will be interpreted as command.

Note 5-3: This pin (RST\_N) is reset signal input. The Reset is active Low.

Note 5-4: This pin (BUSY\_N) is BUSY\_N state output pin. When BUSY\_N is low, the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put BUSY\_N pin low when the driver IC is working such as:

- Outputting display waveform; or
- Programming with OTP
- Communicating with digital temperature sensor

Note 5-5: This pin (BS) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

Table: Bus interface selection

BS	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) – 9 bits SPI



**6. Command Table**

W/R: 0: Write cycle 1: Read cycle C/D: 0: Command 1: Data D7~D0: -: Don't care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default	
1	Panel Setting(PSR)	0	0	0	0	0	0	0	0	0	0		00h	
		0	1	--	--	#	#	#	#	#	#	#	REG, KW/R, UD, SHL, SHD_N, RST_N	0Fh
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01h	
		0	1	--	--	--	#	--	#	#	#	#	BD_EN, VSR_EN, VS_EN, VG_EN	07h
		0	1	#	--	--	#	--	#	#	#	#	VPP_EN, VCOM_SLEW, VG_LVL[2:0]	17h
		0	1	--	--	#	#	#	#	#	#	#	VDH_LVL[5:0]	3ah
		0	1	--	--	#	#	#	#	#	#	#	VDL_LVL[5:0]	3ah
		0	1	--	--	#	#	#	#	#	#	#	VDHR_LVL[5:0]	03h
3	Power OFF(POF)	0	0	0	0	0	0	0	0	1	0		02h	
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1		03h	
		0	1	--	--	#	#	--	--	--	--	--	T_VDS_OFF[1:0]	00h
5	Power ON(PON)	0	0	0	0	0	0	0	1	0	0		04h	
6	Power ON Measure (PMES)	0	0	0	0	0	0	0	1	0	1		05h	
7	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06h	
		0	1	#	#	#	#	#	#	#	#	#	BT_PHA[7:0]	17h
		0	1	#	#	#	#	#	#	#	#	#	BT_PHB[7:0]	17h
		0	1	--	--	#	#	#	#	#	#	#	BT_PHC1[5:0]	17h
		0	1	#	--	#	#	#	#	#	#	#	PHC2_EN, BT_PHC2[5:0]	17h
8	Deep Sleep(DSLP)	0	0	0	0	0	0	0	1	1	1		07h	
		0	1	1	0	1	0	0	1	0	1	1	Check code	A5h
9	Display Start Transmission 1 (DTM1, White/Black Data) (x-byte command)	0	0	0	0	0	1	0	0	0	0	K/W or OLD Pixel Data (800x600):	10h	
		0	1	#	#	#	#	#	#	#	#	#	KPXL[1:8]	-
		0	1	:	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	#	KPXL[n-7:n]	-

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default	
10	Data Stop (DSP)	0	0	0	0	0	1	0	0	0	1		11h	
		1	1	#	--	--	--	--	--	--	--	--	Data_flag	00h
11	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12h	
12	Display Start transmission 2 (DTM2, Red Data) (x-byte command)	0	0	0	0	0	1	0	0	1	1	Red or NEW Pixel Data (800x600):	13h	
		0	1	#	#	#	#	#	#	#	#	#	RPXL[1:8]	-
		0	1	:	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	#	RPXL[n-7:n]	-
13	Dual SPI	0	0	0	0	0	1	0	1	0	1		15h	
		1	1	--	--	#	#	--	--	--	--	--	MM_EN, DUSPI_EN	00h
14	Auto Sequence (AUTO)	0	0	0	0	0	1	0	1	1	1		17h	
		0	1	1	0	1	0	0	1	0	1		Check code	A5h
15	LUT option (LUTOPT)	0	0	0	0	1	0	1	0	1	0		2Ah	
		0	1	#	#	--	--	--	--	--	--	--	STATE_XON[9:8]	00h
		0	1	#	#	#	#	#	#	#	#	#	STATE_XON[7:0]	00h
16	KW LUT option (KWOPT)	0	0	0	0	1	0	1	0	1	1		2Bh	
		0	1	--	--	--	--	--	--	--	#	#	ATRED, NORED	00h
		0	1	#	#	--	--	--	--	--	--	--	KWE[9:8]	00h
		0	1	#	#	#	#	#	#	#	#	#	KWE[7:0]	00h
17	PLL control (PLL)	0	0	0	0	1	1	0	0	0	0		30h	
		0	1	--	--	--	--	#	#	#	#	#	FRS[3:0]	06h
18	Temperature Sensor Calibration (TSC)	0	0	0	1	0	0	0	0	0	0		40h	
		1	1	#	#	#	#	#	#	#	#	#	D[10:3] / TS[7:0]	00h
		1	1	#	#	#	--	--	--	--	--	--	D[2:0] / -	00h
19	Temperature Sensor Selection (TSE)	0	0	0	1	0	0	0	0	0	1		41h	
		0	1	#	--	--	--	#	#	#	#	#	TSE,TO[3:0]	00h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default	
20	Temperature Sensor Write (TSW)	0	0	0	1	0	0	0	0	1	0		42h	
		0	1	#	#	#	#	#	#	#	#	#	WATTR[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	#	WMSB[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	#	WLSB[7:0]	00h
21	Temperature Sensor Read (TSR)	0	0	0	1	0	0	0	0	1	1		43h	
		1	1	#	#	#	#	#	#	#	#	#	RMSB[7:0]	00h
		1	1	#	#	#	#	#	#	#	#	#	RLSB[7:0]	00h
22	Panel Break Check (PBC)	0	0	0	1	0	0	0	1	0	0		44h	
		1	1	--	--	--	--	--	--	--	--	#	PSTA	00h
23	VCOM and data interval setting (CDI)	0	0	0	1	0	1	0	0	0	0		50h	
		0	1	#	--	#	#	--	--	#	#	#	BDZ, BDV[1:0], DDX[1:0]	31h
		0	1	--	--	--	--	#	#	#	#	#	CDI[3:0]	07h
24	Lower Power Detection (LPD)	0	0	0	1	0	1	0	0	0	1		51h	
		1	1	--	--	--	--	--	--	--	--	#	LPD	01h
25	End Voltage Setting (EVS)	0	0	0	1	0	1	0	0	0	1		52h	
		0	1	--	--	--	--	#	--	#	#	#	VCEND, BDEND[1:0]	02h
26	TCON Setting (TCON)	0	0	0	1	1	0	0	0	0	0		60h	
		0	1	#	#	#	#	#	#	#	#	#	S2G[3:0], G2S[3:0]	22h
27	Resolution setting (TRES)	0	0	0	1	1	0	0	0	0	1		61h	
		0	1	--	--	--	--	--	--	#	#	#	HRES[9:8]	03h
		0	1	#	#	#	#	#	0	0	0	0	HRES[7:3]	20h
		0	1	--	--	--	--	--	--	#	#	#	VRES[9:0]	02h
		0	1	#	#	#	#	#	#	#	#	#		58h
28	Gate/Source Start setting (GSST)	0	0	0	1	1	0	0	1	0	1		65h	
		0	1	--	--	--	--	--	--	#	#	#	HST[9:8]	00h
		0	1	#	#	#	#	#	0	0	0	0	HST[7:3]	00h
		0	1	--	--	--	--	--	--	#	#	#	VST[9:0]	00h
		0	1	#	#	#	#	#	#	#	#	#		00h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
29	Revision (REV)	0	0	0	1	1	1	0	0	0	0		70h
		1	1	#	#	#	#	#	#	#	#	PROD_REV[23:16]	FFh
		1	1	#	#	#	#	#	#	#	#	PROD_REV[15:8]	FFh
		1	1	#	#	#	#	#	#	#	#	PROD_REV[7:0]	FFh
		1	1	#	#	#	#	#	#	#	#	LUT_REV[23:16]	FFh
		1	1	#	#	#	#	#	#	#	#	LUT_REV[15:8]	FFh
		1	1	#	#	#	#	#	#	#	#	LUT_REV[7:0]	FFh
		1	1	#	#	#	#	#	#	#	#	CHIP_REV[7:0]	0Ch
30	Status register (FLG)	0	0	0	1	1	1	0	0	0	1		71h
		1	1	--	#	#	#	#	#	#	#	PTL_FLAG ,I2 C_ERR, I2 C_BUSYN, DATA_FLAG, PON, POF, BUSY_N	13h
31	Auto Measurement VCOM (AMV)	0	0	1	0	0	0	0	0	0	0		80h
		1	1	--	--	#	#	#	#	#	#	AMV[1:0],XON,AMVS,AMV, AMVE	10h
32	Read VCOM Value (VV)	0	0	1	0	0	0	0	0	0	1		81h
		1	1	--	--	#	#	#	#	#	#	VV[6:0]	00h
33	VCM_DC Setting register (VDCS)	0	0	1	0	0	0	0	0	1	0		82h
		0	1	--	#	#	#	#	#	#	#	VDCS[6:0]	00h
34	Partial Window (PTL)	0	0	1	0	0	1	0	0	0	0		90h
		0	1	--	--	--	--	--	--	#	#	HRST[9:8]	00h
		0	1	#	#	#	#	#	0	0	0	HRST[7:3]	00h
		0	1	--	--	--	--	--	--	#	#	HRED[9:8]	03h
		0	1	#	#	#	#	#	1	1	1	HRED[7:3]	1Fh
		0	1	--	--	--	--	--	--	#	#	VRST[9:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	--	--	--	--	--	--	#	#	VRED[8:0]	02h
		0	1	#	#	#	#	#	#	#	#		57h
		0	1	--	--	--	--	--	--	#	#	PT_SCAN	01h
35	Partial In (PTIN)	0	0	1	0	0	1	0	0	0	1		91h
36	Partial Out (PTOUT)	0	0	1	0	0	1	0	0	1	0		92h
37	Program Mode(PGM)	0	0	1	0	1	0	0	0	0	0		A0h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default	
38	Active Program(APG)	0	0	1	0	1	0	0	0	0	1		A1h	
39	Read OTP Data(ROTP)	0	0	1	0	1	0	0	0	1	0		A2h	
		1	1	#	#	#	#	#	#	#	#	Data of Address = 000h	N/A	
		1	1	:	:	:	:	:	:	:	:	:	:	N/A
		1	1	#	#	#	#	#	#	#	#	#	Data of Address = n	N/A
40	Cascade Setting (CCSET)	0	0	1	1	1	0	0	0	0	0		E0h	
		0	1	--	--	--	--	--	--	#	#	TSFIX, CCEN	00h	
41	Power Saving (PWS)	0	0	1	1	1	0	0	0	1	1		E3h	
		0	1	#	#	#	#	#	#	#	#	VCOM_W[3:0], SD_W[3:0]	00h	
42	LVD Voltage Select (LVSEL)	0	0	1	1	1	0	0	1	0	0		E4h	
		0	1	--	--	--	--	--	--	#	#	LVD_SEL[1:0]	03h	
43	Force Temperature (TSSET)	0	0	1	1	1	0	0	1	0	1		E5h	
		0	1	#	#	#	#	#	#	#	#	TS_SET[7:0]	00h	
44	Temperature Boundary Phase-C2 (TSBDRY)	0	0	1	1	1	0	0	1	1	1		E7h	
		0	1	#	#	#	#	#	#	#	#	TSBDRY_PHC2[7:0]	00h	

(1) Panel Setting (PSR) (Register: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting the panel	0	0	0	0	0	0	0	0	0	0
	0	1	-	-	REG	KW/R	UD	SHL	SHD_N	RST_N

REG: LUT selection

- 0: LUT from OTP. (Default)
- 1: LUT from register.

KW/R: Black / White / Red

- 0: Pixel with Black/White/Red, KWR mode. (Default)
- 1: Pixel with Black/White, KW mode.

UD: Gate Scan Direction

- 0: Scan down. First line to Last line: Gn-1 → Gn-2 → Gn-3 → ... → G0
- 1: Scan up. (Default) First line to Last line: G0 → G1 → G2 → ... → Gn-1

SHL: Source Shift Direction

- 0: Shift left. First data to Last data: Sn-1 → Sn-2 → Sn-3 → ... → S0
- 1: Shift right. (Default) First data to Last data: S0 → S1 → S2 → ... → Sn-1

SHD\_N: Booster Switch

- 0: Booster OFF
- 1: Booster ON (Default)

When SHD\_N becomes LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF. And Source/Gate/Border/VCOM will be released to floating.

RST\_N: Soft Reset

- 0: No effect. (default)
- 1: Booster OFF, Register data are set to their default values, and SEG/BG/VCOM: floating.

When RST\_N become low, driver will reset. All register will reset to default value. Driver all function will disable. SD output and VCOM will base on previous condition and keep floating.

(2) Power Setting Register (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Selecting Internal/External Power	0	0	0	0	0	0	0	0	0	1
	0	1	-	-	-	BD_EN	-	VSR_EN	VS_EN	VG_EN
	0	1	VPP_EN	-	-	VCOM_SLEW	-	VG_LVL[2:0]		
	0	1	-	-	VDH_LVL[5:0]					
	0	1	-	-	VDL_LVL[5:0]					
	0	1	-	-	VDHR_LVL[5:0]					

BD\_EN: Border LDO enable

- 0: Border LDO disable (Default)
- Border level selection: 00b: VCOM 01b: VDH 10b: VDL 11b: VDHR

1: Border LDO enable

Border level selection: 00b: VCOM 01b: VBH(VCOM-VDL) 10b: VBL(VCOM-VDH) 11b: VDHR

VSR\_EN: Source LV power selection

- 0: External source power from VDHR pins
- 1: Internal DC/DC function for generating VDHR. (Default)

VS\_EN: Source power selection

0 : External source power from VDH/VDL pins

1 : Internal DC/DC function for generating VDH/VDL. (Default)

VG\_EN: Gate power selection

0 : External gate power from VGH/VGL pins

1 : Internal DC/DC function for generating VGH/VGL. (Default)

VPP\_EN: OTP program power selection

0 : External OTP program power from VPP pin

1 : OTP program power from internal power circuit.

Internal OTP program power voltage is selected by VDHR\_LVL[5:0].

VCOM\_SLEW: VCOM slew rate selection for voltage transition

0 : Slow slew rate

1 : Fast slew rate

VG\_LVL[2:0]: VGH / VGL Voltage Level selection.

VG_LVL[2:0]	VGH/VGL Voltage Level
000	VGH=9V, VGL= -9V
001	VGH=10V, VGL= -10V
010	VGH=11V, VGL= -11V
011	VGH=12V, VGL= -12V
100	VGH=17V, VGL= -17V
101	VGH=18V, VGL= -18V
110	VGH=19V, VGL= -19V
111 (Default)	VGH=20V, VGL= -20V

VDH\_LVL[5:0]: Internal VDH power selection for K/W pixel. (Default value: 111010b)

VDH_LVL	Voltage	VDH_LVL	Voltage	VDH_LVL	Voltage	VDH_LVL	Voltage
000000	2.4 V	010001	5.8 V	100010	9.2 V	110011	12.6V
000001	2.6 V	010010	6.0 V	100011	9.4 V	110100	12.8V
000010	2.8 V	010011	6.2 V	100100	9.6 V	110101	13.0V
000011	3.0 V	100101	6.4 V	100101	9.8 V	110110	13.2V
000100	3.2 V	010101	6.6 V	100110	10.0 V	110110	13.4V
000101	3.4 V	010110	6.8 V	100111	10.2 V	111000	13.6V
000110	3.6 V	010111	7.0 V	101000	10.4 V	111001	13.8V
000111	3.8 V	011000	7.2 V	101001	10.6 V	111001	14.0V
001000	4.0 V	011001	7.4 V	101010	10.8 V	111011	14.2V
001001	4.2 V	011010	7.6 V	101011	11.0 V	111100	14.4V
001010	4.4 V	011011	7.8 V	101100	11.2 V	111101	14.6V
001011	4.6 V	011100	8.0 V	101101	11.4 V	111110	14.8V
001100	4.8 V	011101	8.2 V	101110	11.6 V	111111	15.0V
001101	5.0 V	011110	8.4 V	101111	11.8 V		
001110	5.2 V	011111	8.6 V	110000	12.0 V		
001111	5.4 V	100000	8.8 V	110001	12.2 V		
010000	5.6 V	100001	9.0 V	110010	12.4 V		

VDL\_LVL[5:0]: Internal VDL power selection for K/W pixel. (Default value: 111010b)

VDL_LVL	Voltage	VDL_LVL	Voltage	VDL_LVL	Voltage	VDL_LVL	Voltage
000000	- 2.4 V	010001	- 5.8 V	100010	- 9.2 V	110011	- 12.6V
000001	- 2.6 V	010010	- 6.0 V	100011	- 9.4 V	110100	- 12.8V
000010	- 2.8 V	010011	- 6.2 V	100100	- 9.6 V	110101	- 13.0V
000011	- 3.0 V	100101	- 6.4 V	100101	- 9.8 V	110110	- 13.2V
000100	- 3.2 V	010101	- 6.6 V	100110	- 10.0 V	110110	- 13.4V
000101	- 3.4 V	010110	- 6.8 V	100111	- 10.2 V	111000	- 13.6V
000110	- 3.6 V	010111	- 7.0 V	101000	- 10.4 V	111001	- 13.8V
000111	- 3.8 V	011000	- 7.2 V	101001	- 10.6 V	111001	- 14.0V
001000	- 4.0 V	011001	- 7.4 V	101010	- 10.8 V	111011	- 14.2V
001001	- 4.2 V	011010	- 7.6 V	101011	- 11.0 V	111100	- 14.4V
001010	- 4.4 V	011011	- 7.8 V	101100	- 11.2 V	111101	- 14.6V
001011	- 4.6 V	011100	- 8.0 V	101101	- 11.4 V	111110	- 14.8V
001100	- 4.8 V	011101	- 8.2 V	101110	- 11.6 V	111111	- 15.0V
001101	- 5.0 V	011110	- 8.4 V	101111	- 11.8 V		
001110	- 5.2 V	011111	- 8.6 V	110000	- 12.0 V		
001111	- 5.4 V	100000	- 8.8 V	110001	- 12.2 V		
010000	- 5.6 V	100001	- 9.0 V	110010			

VDHR\_LVL[5:0]: Internal VDHR power selection for Red pixel. (Default value: 000011b)

VDHR_LVL	Voltage	VDHR_LVL	Voltage	VDHR_LVL	Voltage	VDHR_LVL	Voltage
000000	2.4 V	010001	5.8 V	100010	9.2 V	110011	12.6V
000001	2.6 V	010010	6.0 V	100011	9.4 V	110100	12.8V
000010	2.8 V	010011	6.2 V	100100	9.6 V	110101	13.0V
000011	3.0 V	100101	6.4 V	100101	9.8 V	110110	13.2V
000100	3.2 V	010101	6.6 V	100110	10.0 V	110110	13.4V
000101	3.4 V	010110	6.8 V	100111	10.2 V	111000	13.6V
000110	3.6 V	010111	7.0 V	101000	10.4 V	111001	13.8V
000111	3.8 V	011000	7.2 V	101001	10.6 V	111001	14.0V
001000	4.0 V	011001	7.4 V	101010	10.8 V	111011	14.2V
001001	4.2 V	011010	7.6 V	101011	11.0 V	111100	14.4V
001010	4.4 V	011011	7.8 V	101100	11.2 V	111101	14.6V
001011	4.6 V	011100	8.0 V	101101	11.4 V	111110	14.8V
001100	4.8 V	011101	8.2 V	101110	11.6 V	111111	15.0V
001101	5.0 V	011110	8.4 V	101111	11.8 V		
001110	5.2 V	011111	8.6 V	110000	12.0 V		
001111	5.4 V	100000	8.8 V	110001	12.2 V		
010000	5.6 V	100001	9.0 V	110010	12.4 V		

(3) Power OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning OFF the power	0	0	0	0	0	0	0	0	1	0

After the Power OFF command, the driver will be powered OFF. Refer to the POWER MANAGEMENT section for the sequence.



This command will turn off booster, controller, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD turned OFF or Deep Sleep Mode. Source/Gate/Border/VCOM will be released to floating.

(4) Power OFF Sequence Setting (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting	0	0	0	0	0	0	0	0	1	1
Power OFF Sequence	0	1	-	-	T_VDS_OFF[1:0]	-	-	-	-	-

T\_VDS\_OFF[1:0]: Source to gate power off interval time.

00b: 1 frame (Default)    01b: 2 frames    10b: 3 frames    11b: 4 frame

(5) Power ON (R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning ON the Power	0	0	0	0	0	0	0	1	0	0

After the Power ON command, the driver will be powered ON. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn on booster, controller, regulators, and temperature sensor will be activated for one-time sensing before enabling booster. When all voltages are ready, the BUSY\_N signal will return to high.

(6) Power ON Measure (PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Internal Bandgap Set	0	0	0	0	0	0	0	1	0	1

This command enables the internal bandgap, which will be cleared by the next POF.

(7) Booster Soft Start (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Booster Software Start Set	0	0	0	0	0	0	0	1	1	0
	0	1	BT_PHA[7:6]			BT_PHA[5:3]		BT_PHA[2:0]		
	0	1	BT_PHB[7:6]			BT_PHB[5:3]		BT_PHB[2:0]		
	0	1	-	-	BT_PHC1[5:3]		BT_PHC1[2:0]			
	0	1	PHC2EN		-	BT_PHC2[5:3]		BT_PHC2[2:0]		

BT\_PHA[7:6]: Soft start period of phase A.

00b: 10mS    01b: 20mS    10b: 30mS    11b: 40mS

BT\_PHA[5:3]: Driving strength of phase A

000b: strength 1    001b: strength 2    010b: strength 3    011b: strength 4  
 100b: strength 5    101b: strength 6    110b: strength 7    111b: strength 8 (strongest)

BT\_PHA[2:0]: Minimum OFF time setting of GDR in phase A

000b: 0.27uS    001b: 0.34uS    010b: 0.40uS    011b: 0.54uS  
 100b: 0.80uS    101b: 1.54uS    110b: 3.34uS    111b: 6.58uS

BT\_PHB[7:6]: Soft start period of phase B.

00b: 10mS    01b: 20mS    10b: 30mS    11b: 40mS

BT\_PHB[5:3]: Driving strength of phase B

000b: strength 1    001b: strength 2    010b: strength 3    011b: strength 4  
 100b: strength 5    101b: strength 6    110b: strength 7    111b: strength 8 (strongest)

BT\_PHB[2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS    001b: 0.34uS    010b: 0.40uS    011b: 0.54uS

100b: 0.80uS      101b: 1.54uS      110b: 3.34uS      111b: 6.58uS

BT\_PHC1[5:3]:      Driving strength of phase C1

000b: strength 1      001b: strength 2      010b: strength 3      011b: strength 4  
 100b: strength 5      101b: strength 6      110b: strength 7      111b: strength 8 (strongest)

BT\_PHC1[2:0]:      Minimum OFF time setting of GDR in phase C1

000b: 0.27uS      001b: 0.34uS      010b: 0.40uS      011b: 0.54uS  
 100b: 0.80uS      101b: 1.54uS      110b: 3.34uS      111b: 6.58uS

PHC2EN:      Booster phase-C2 enable

0:      Booster phase-C2 disable

Phase-C1 setting always is applied for booster phase-C.

1:      Booster phase-C2 enable

If temperature > temperature boundary phase-C2(RE7h[7:0]), phase-C1 setting is applied for booster phase-C.

If temperature <= temperature boundary phase-C2(RE7h[7:0]), phase-C2 setting is applied for booster phase-C.

BT\_PHC2[5:3]:      Driving strength of phase C2

000b: strength 1      001b: strength 2      010b: strength 3      011b: strength 4  
 100b: strength 5      101b: strength 6      110b: strength 7      111b: strength 8 (strongest)

BT\_PHC2[2:0]:      Minimum OFF time setting of GDR in phase C2

000b: 0.27uS      001b: 0.34uS      010b: 0.40uS      011b: 0.54uS  
 100b: 0.80uS      101b: 1.54uS      110b: 3.34uS      111b: 6.58uS

(8) Deep Sleep (DSLPL) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Deep Sleep	0	0	0	0	0	0	0	1	1	1
	0	1	1	0	1	0	0	1	0	1

After this command is transmitted, the chip will enter Deep Sleep Mode to save power. Deep Sleep Mode will return to Standby Mode by hardware reset. The only one parameter is a check code, the command will be executed if check code = 0xA5.

(9) Data Start Transmission 1 (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	0	0	0
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8
	0	1	..	..	..	..	..	..	..	..
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes “OLD” data to SRAM.

In KWR mode, this command writes “K/W” data to SRAM.

In Program mode, this command writes “OTP” data to SRAM for programming.

(10) Data stop (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Stopping data transmission	0	0	0	0	0	1	0	0	0	1
	1	1	data_flag	-	-	-	-	-	-	-

Check the completeness of data. If data is complete, start to refresh display.

Data\_flag: Data flag of receiving user data.

0: Driver didn't receive all the data.

1: Driver has already received all the one-frame data (DTM1 and DTM2).

After "Data Start" (R10h) or "Data Stop" (R11h) commands and when data\_flag=1, the refreshing of panel starts and BUSY\_N signal will become "0".

(11) Display Refresh (DRF) (R12 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Refreshing the display	0	0	0	0	0	1	0	0	1	0

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.

After Display Refresh command, BUSY\_N signal will become "0" and the refreshing of panel starts.

(12) Data Start Transmission 2(DTM2) (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	0	1	1
	0	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8
	0	1	..	..	..	..	..	..	..	..
	0	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes "NEW" data to SRAM.

In KWR mode, this command writes "RED" data to SRAM.

(13) Dual SPI Mode (DUSPI) (R15 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Stopping data transmission	0	0	0	0	0	1	0	1	0	1
	0	1	-	-	MM_EN	DUSPI_EN	-	-	-	-

This command sets dual SPI mode.

MM\_EN: MM input pin definition enable.

0: MM input pin definition disable

1: MM input pin definition enable.

DUSPI\_EN: Dual SPI mode enable.

0: Dual SPI mode disable (single SPI mode)

1: Dual SPI mode enable

(14) Auto Sequence (AUTO) (R17h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Auto	0	0	0	0	0	1	0	1	1	1
Sequence	0	1	1	0	1	0	0	1	0	1

The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP.

AUTO (0x17) + Code(0xA5) = (PON → DRF → POF)

AUTO (0x17) + Code(0xA7) = (PON → DRF → POF → DSLP)

(15) LUT Option (LUTOPT) (R2Ah)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
LUT Option	0	0	0	0	1	0	1	0	1	0
	0	1	STATE_XON[9:8]		-	-	-	-	-	-
	0	1	STATE_XON[7:0]							

This command sets XON control enable.

STATE\_XON[9:0]:

All Gate ON (Each bit controls one state, STATE\_XON [0] for state-1, STATE\_XON [1] for state-2 .....

- 00 0000 0000b: no All-Gate-ON
- 00 0000 0001b: State-1 All-Gate-ON
- 00 0000 0011b: State-1 and State2 All-Gate-ON
- : :

(16) KW LUT Option (KWOPT) (R2Bh)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
KW LUT Option	0	0	0	0	1	0	1	0	1	1
	0	1	-	-	-	-	-	-	ATRED	NORED
	0	1	KWE[9:8]		-	-	-	-	-	-
	0	1	KWE[7:0]							

This command sets KW LUT mechanism option in KWR mode’s LUT and only valid in K/W/R mode.

{ATRED, NORED}: KW LUT or KWR LUT selection control

ATRED	NORED	Description
0	0	KWR LUT always
0	1	KW LUT only
1	0	Auto detect by red data
1	1	KW LUT only

KWE[9:0]:

KW LUT enable control bits. Each bit controls one state, KWE[0] for state-1, KWE[1] for state-2, ... .

At least 1 Enable Control bit should be set when KW LUT only is selected in KWR mode.

- 00 0000 0001b: KW LUT enable in State-1
- 00 0000 0011b: KW LUT enable in State-1 and State2
- 00 0000 1011b: KW LUT enable in State-1, State2 and State-4

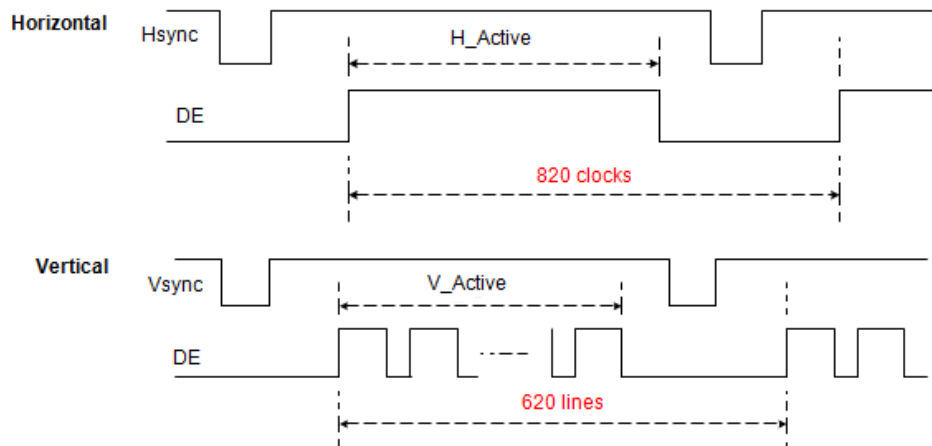
(17) PLL Control (PLL) (R30h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Controlling	0	0	0	0	1	1	0	0	0	0
PLL	0	1	-	-	-	-	FRS[3:0]			

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

FMR[3:0]: Frame rate setting

FRS	Frame rate	FRS	Frame rate
0000	5Hz	1000	70Hz
0001	10Hz	1001	80Hz
0010	15Hz	1010	90Hz
0011	20Hz	1011	100Hz
0100	30Hz	1100	110Hz
0101	40Hz	1101	130Hz
<b>0110</b>	<b>50Hz</b>	1110	150Hz
0111	60Hz	1111	200Hz



(18) Temperature Sensor Calibration (TSC) (R40h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	0	0	0	1	0	0	0	0	0	0
	1	1	D10/TS7	D9/TS6	D8/TS5	D7/TS4	D6 / TS3	D5 / TS2	D4 / TS1	D3 / TS0
	1	1	D2	D1	D0	-	-	-	-	-

This command enables internal or external temperature sensor, and reads the result.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

TS[7:0]/D[10:3]	Temp. (°C)	TS[7:0]/D[10:3]	Temp. (°C)	TS[7:0]/D[10:3]	Temp. (°C)
1110_0111	-25	0000_0000	0	0001_1001	25
1110_1000	-24	0000_0001	1	0001_1010	26
1110_1001	-23	0000_0010	2	0001_1011	27
1110_1010	-22	0000_0011	3	0001_1100	28
1110_1011	-21	0000_0100	4	0001_1101	29
1110_1100	-20	0000_0101	5	0001_1110	30
1110_1101	-19	0000_0110	6	0001_1111	31
1110_1110	-18	0000_0111	7	0010_0000	32
1110_1111	-17	0000_1000	8	0010_0001	33
1111_0000	-16	0000_1001	9	0010_0010	34
1111_0001	-15	0000_1010	10	0010_0011	35
1111_0010	-14	0000_1011	11	0010_0100	36
1111_0011	-13	0000_1100	12	0010_0101	37
1111_0100	-12	0000_1101	13	0010_0110	38
1111_0101	-11	0000_1110	14	0010_0111	39
1111_0110	-10	0000_1111	15	0010_1000	40
1111_0111	-9	0001_0000	16	0010_1001	41
1111_1000	-8	0001_0001	17	0010_1010	42
1111_1001	-7	0001_0010	18	0010_1011	43
1111_1010	-6	0001_0011	19	0010_1100	44
1111_1011	-5	0001_0100	20	0010_1101	45
1111_1100	-4	0001_0101	21	0010_1110	46
1111_1101	-3	0001_0110	22	0010_1111	47
1111_1110	-2	0001_0111	23	0011_0000	48
1111_1111	-1	0001_1000	24	0011_0001	49

## (19) Temperature Sensor Enable (TSE) (R41h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Enable	0	0	0	1	0	0	0	0	0	1
Temperature Sensor /Offset	0	1	TSE	-	-	-	TO[3:0]			

This command selects Internal or External temperature sensor.

TSE:

Internal temperature sensor switch

0: Enable (default)

1: Disable; using external sensor.

TO[3:0]: Temperature offset.

TO[3:0]	Calibration	TO[3:0]	Calibration
0000 b	+0 (Default)	1000	-8
0001	+1	1001	-7
0010	+2	1010	-6
0011	+3	1011	-5
0100	+4	1100	-4
0101	+5	1101	-3
0110	+6	1110	-2
0111	+7	1111	-1

(20) Temperature Sensor Write (TSW) (R42h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Write External Temperature Sensor	0	0	0	1	0	0	0	0	1	0
	0	1	WATTR[7:0]							
	0	1	WMSB[7:0]							
	0	1	WLSB[7:0]							

This command writes the temperature sensed by the temperature sensor.

WATTR[7:6]: I2C Write Byte Number

00b : 1 byte (head byte only)

01b : 2 bytes (head byte + pointer)

10b : 3 bytes (head byte + pointer + 1st parameter)

11b : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

WATTR[5:3]: User-defined address bits (A2, A1, A0)

WATTR[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor

WLSB[7:0]: LSByte of write-data to external temperature sensor

(21) Temperature Sensor Read (TSR) (R43h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read External Temperature Sensor	0	0	0	1	0	0	0	0	1	1
	1	1	RMSB[7:0]							
	1	1	RLSB[7:0]							

This command reads the temperature sensed by the temperature sensor.

RMSB[7:0]: MSByte read data from external temperature sensor

RLSB[7:0]: LSByte read data from external temperature sensor

## (22) Panel Glass Check (PBC)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Check Panel	0	0	0	1	0	0	0	1	0	0
Glass	1	1	-	-	-	-	-	-	-	PSTA

This command is used to enable panel check, and to disable after reading result.

PSTA: 0: Panel check fail (panel broken) 1: Panel check pass

## (23) VCOM and Data interval Setting (CDI) (R50h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Interval	0	0	0	1	0	1	0	0	0	0
between VCOM	0	1	BDZ	-	BDV[1:0]		N2OCP	-	DDX[1:0]	
and Data	0	1	-	-	-	-	CDI[3:0]			

This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

BDZ: Border Hi-Z control

0: Border output Hi-Z disabled (default) 1: Border output Hi-Z enabled

BDV[1:0]: Border LUT selection

KWR mode (KW/R=0)

DDX[0]	BDV[1:0]	LUT
0	00	LUTBD
	01	LUTR
	10	LUTW
	11	LUTK
1 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	LUTBD

KW mode (KW/R=1)

DDX[0]	BDV[1:0]	LUT
0	00	LUTBD
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	LUTKK (0 → 0)
1 (Default)	00	LUTKK (0 → 0)
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	LUTBD

N2OCP: Copy frame data from NEW data to OLD data enable control after display refresh with NEW/OLD in KW mode.

0: Copy NEW data to OLD data disabled (default) 1: Copy NEW data to OLD data enabled



DDX[1:0]: Data polarity.

Under KWR mode (KW/R=0):

DDX[1] is for RED data.

DDX[0] is for K/W data,

DDX[1:0]	Data {Red, K/W}	LUT
00	00	LUTW
	01	LUTK
	10	LUTR
	11	LUTR
01 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	LUTR

DDX[1:0]	Data {Red, K/W}	LUT
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTK
11	00	LUTR
	01	LUTR
	10	LUTK
	11	LUTW

Under KW mode (KW/R=1):

DDX[1]=0 is for KW mode with NEW/OLD,

DDX[1]=1 is for KW mode without NEW/OLD.

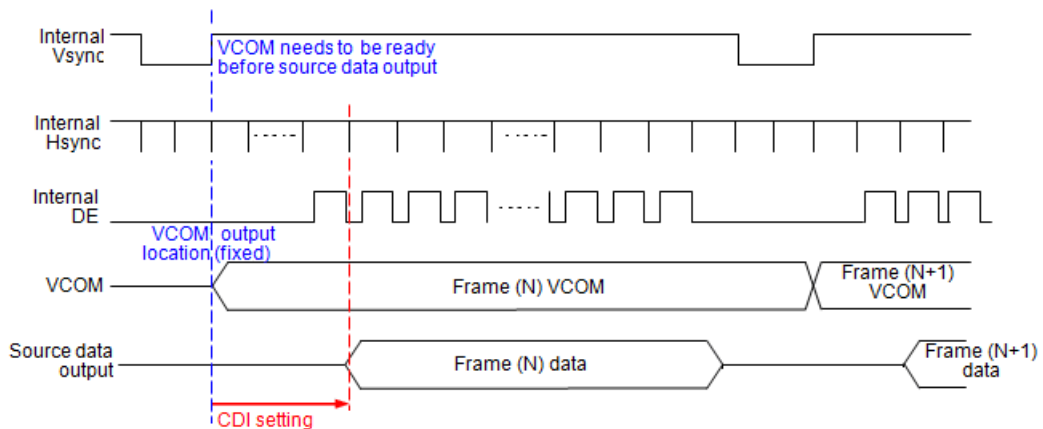
DDX[1:0]	Data {NEW, OLD}	LUT
00	00	LUTWW (0 → 0)
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	LUTKK (1 → 1)
01 (Default)	00	LUTKK (0 → 0)
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	LUTWW (1 → 1)

DDX[1:0]	Data {NEW}	LUT
10	0	LUTKW (1 → 0)
	1	LUTWK (0 → 1)
11	0	LUTWK (1 → 0)
	1	LUTKW (0 → 1)

CDI[3:0]: VCOM and data interval

CDI[3:0]	VCOM and Data Interval
0000 b	17 hsync
0001	16
0010	15
0011	14
0100	13
0101	12
0110	11
0111	10 (Default)

CDI[3:0]	VCOM and Data Interval
1000	9
1001	8
1010	7
1011	6
1100	5
1101	4
1110	3
1111	2



(24) Low Power Detection (LPD) (R51h)

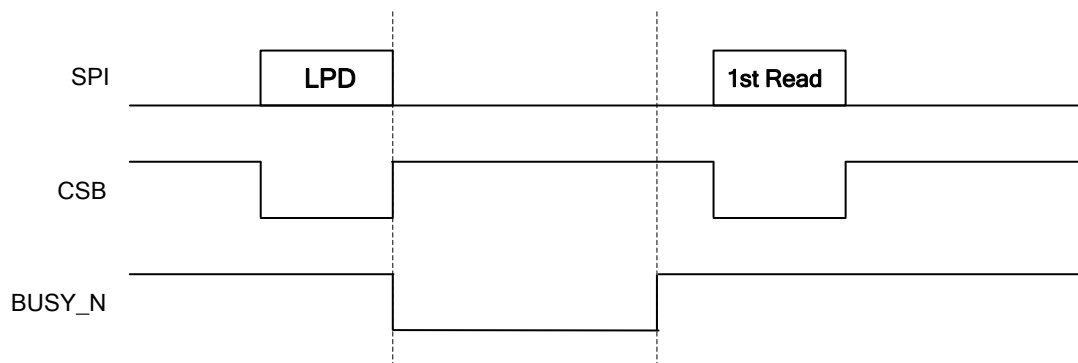
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Detect Low Power	0	0	0	1	0	1	0	0	0	1
	1	1	-	-	-	-	-	-	-	LPD

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal Low Power Detection Flag

0: Low power input ( $V_{DD} < 2.5V, 2.4V, 2.3V,$  or  $2.2V$ , selected by  $LVD\_SEL[1:0]$  in command LVSEL)

1: Normal status (default)



(25) End Voltage Setting (EVS) (R52h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
End Voltage Setting	0	0	0	1	0	1	0	0	1	0
	0	1	-	-	-	-	VCEND	-	BDEND[1:0]	

This command selects source end voltage and border end voltage after LUTs are finished.

VCEND: VCOM end voltage selection

0b: VCOM\_DC      1b: floating

BDEND[1:0]: Border end voltage selection

00b: 0V      01b: 0V      10b: VCOM\_DC      11b: floating

(26) TCON Setting (TCON) (R60h)

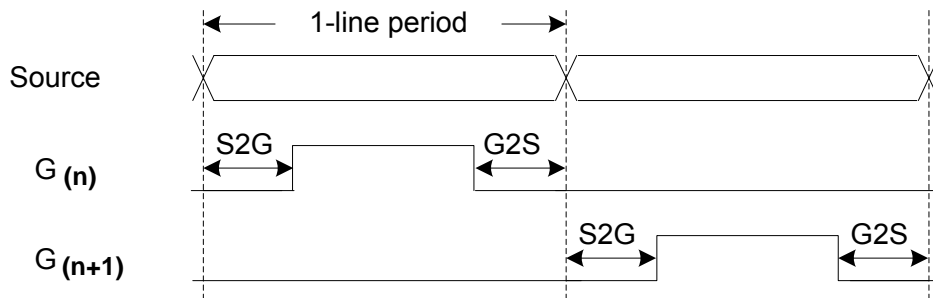
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Gate/Source Non-overlap	0	0	0	1	1	0	0	0	0	0
Period	0	1	S2G[3:0]				G2S[3:0]			

This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period	S2G[3:0] or G2S[3:0]	Period
0000 b	4	1000 b	36
0001	8	1001	40
0010	12 (Default)	1010	44
0011	16	1011	48
0100	20	1100	52
0101	24	1101	56
0110	28	1110	60
0111	32	1111	64

Period Unit = 667 nS.



(27) Resolution Setting (TRES) (R61h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Resolution	0	0	0	1	1	0	0	0	0	1
	0	1	-	-	-	-	-	-	HRES[9:8]	
	0	1	HRES[7:3]					0	0	0
	0	1	-	-	-	-	-	-	VRES[9:8]	
	0	1	VRES[7:0]							

This command defines resolution setting.

HRES[9:3]: Horizontal Display Resolution (Value range: 01h ~ 64h)

VRES[9:0]: Vertical Display Resolution (Value range: 001h ~ 258h)

Active channel calculation, assuming HST[9:0]=0, VST[9:0]=0:

Gate: First active gate = G0;

Last active gate = VRES[9:0] - 1

Source: First active source = S0;

Last active source = HRES[9:3]\*8 - 1

Example: 128 (source) x 272 (gate), assuming HST[9:0]=0, VST[9:0]=0

Gate: First active gate = G0,  
 Last active gate = G271; (VRES[9:0] = 272, 272 - 1 = 271)  
 Source: First active source = S0,  
 Last active source = S127; (HRES[9:3] = 16, 16 \* 8 - 1 = 127)

(28) Gate/Source Start Setting (GSST) (R65h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Gate/Source Start	0	0	0	1	1	0	0	1	0	1
	0	1	-	-	-	-	-	-	HST[9:8]	
	0	1	HST[7:3]					0	0	0
	0	1	-	-	-	-	-	-	VST[9:8]	
	0	1	VST[7:0]							

This command defines resolution start gate/source position.

HST[9:3]: Horizontal Display Start Position (Source). (Value range: 00h ~ 63h)

VST[9:0]: Vertical Display Start Position (Gate). (Value range: 000h ~ 257h)

Example : For 128(Source) x 240(Gate)

HST[9:3] = 4 (HST[9:0] = 4 \* 8 = 32),

VST[9:0] = 32

Gate: First active gate = G32 (VST[9:0] = 32),  
 Last active gate = G271 (VRES[9:0] = 240, VST[9:0] = 32, 240 - 1 + 32 = 271)  
 Source: First active source = S32 (HST[9:0] = 32),  
 Last active source = S239 (HRES[9:0] = 128, HST[9:0] = 32, 128 - 1 + 32 = 239)

(29) Revision (REV) (R70h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
LUT/Chip Revision	0	0	0	1	1	1	0	0	0	0
	1	1	PROD_REV[23:16]							
	1	1	PROD_REV[15:8]							
	1	1	PROD_REV[7:0]							
	1	1	LUT_REV[23:16]							
	1	1	LUT_REV[15:8]							
	1	1	LUT_REV[7:0]							
	1	1	CHIP_REV[7:0]							

The command reads the product revision, LUT revision and chip revision.

PROD\_REV[23:0]: Product Revision. PROD\_REV[23:0] is read from OTP address 0x0BDD ~ 0x0BDF or 0x17DD ~ 0x17DF.

LUT\_REV[23:0]: LUT Revision. LUT\_REV[23:0] is read from OTP address 0x0BE0 ~ 0x0BE2 or 0x17E0 ~ 0x17E2.

CHIP\_REV[7:0]: Chip Revision, fixed at 00001100b.

## (30) Get Status (FLG) (R71h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	0	1	1	1	0	0	0	1
Flags	1	1	-	PTL_Flag	I <sup>2</sup> C_ERR	I <sup>2</sup> C_BUSYN	Data_Flag	PON	POF	BUSY_N

This command reads the IC status.

PTL\_Flag: Partial display status (high: partial mode)

I<sup>2</sup>C\_ERR: I<sup>2</sup>C master error status

I<sup>2</sup>C\_BUSYN: I<sup>2</sup>C master busy status (low active)

Data\_Flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY\_N: Driver busy status (low active)

## (31) Auto Measure VCOM (AMV) (R80h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure VCOM	0	0	1	0	0	0	0	0	0	0
	0	1	-	-	AMVT[1:0]	XON	AMVS	AMV	AMVE	

This command triggers auto VCOM sensing mechanism.

AMVT[1:0]: Auto Measure VCOM Time

00b: 3s

01b: 5s (default)

10b: 8s

11b: 10s

XON: All Gate ON of AMV

0: Gate normally scan during Auto Measure VCOM period. (default)

1: All Gate ON during Auto Measure VCOM period.

AMVS: Source output of AMV

0: Source output 0V during Auto Measure VCOM period. (default)

1: Source output VDHR during Auto Measure VCOM period.

AMV: Analog signal

0: Get VCOM value with the VV command (R81h) (default)

1: Get VCOM value in analog signal. (External analog to digital converter)

AMVE: Auto Measure VCOM Enable (/Disable)

0: No effect (default)

1: Trigger auto VCOM sensing.

## (32) VCOM Value (VV) (R81h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure VCOM	0	0	1	0	0	0	0	0	0	1
	1	1	-	VV[6:0]						

This command gets the VCOM value.

VV[6:0]: VCOM Value Output

VV [6:0]	VCOM Voltage (V)	VV [6:0]	VCOM Voltage (V)	VV [6:0]	VCOM Voltage (V)
000 0000b	-0.10	001 1011b	-1.45	011 0110b	-2.80
000 0001b	-0.15	001 1100b	-1.50	011 0111b	-2.85
000 0010b	-0.20	001 1101b	-1.55	011 1000b	-2.90
000 0011b	-0.25	001 1110b	-1.60	011 1001b	-2.95
000 0100b	-0.30	001 1111b	-1.65	011 1010b	-3.00
000 0101b	-0.35	010 0000b	-1.70	011 1011b	-3.05
000 0110b	-0.40	010 0001b	-1.75	011 1100b	-3.10
000 0111b	-0.45	010 0010b	-1.80	011 1101b	-3.15
000 1000b	-0.50	010 0011b	-1.85	011 1110b	-3.20
000 1001b	-0.55	010 0100b	-1.90	011 1111b	-3.25
000 1010b	-0.60	010 0101b	-1.95	100 0000b	-3.30
000 1011b	-0.65	010 0110b	-2.00	100 0001b	-3.35
000 1100b	-0.70	010 0111b	-2.05	100 0010b	-3.40
000 1101b	-0.75	010 1000b	-2.10	100 0011b	-3.45
000 1110b	-0.80	010 1001b	-2.15	100 0100b	-3.50
000 1111b	-0.85	010 1010b	-2.20	100 0101b	-3.55
001 0000b	-0.90	010 1011b	-2.25	100 0110b	-3.60
001 0001b	-0.95	010 1100b	-2.30	100 0111b	-3.65
001 0010b	-1.00	010 1101b	-2.35	100 1000b	-3.70
001 0011b	-1.05	010 1110b	-2.40	100 1001b	-3.75
001 0100b	-1.10	010 1111b	-2.45	100 1010b	-3.80
001 0101b	-1.15	011 0000b	-2.50	100 1011b	-3.85
001 0110b	-1.20	011 0001b	-2.55	100 1100b	-3.90
001 0111b	-1.25	011 0010b	-2.60	100 1101b	-3.95
001 1000b	-1.30	011 0011b	-2.65	100 1110b	-4.00
001 1001b	-1.35	011 0100b	-2.70	100 1111b	-4.05
001 1010b	-1.40	011 0101b	-2.75		

## (33) VCOM\_DC Setting (VDCS) (R82h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set VCOM_DC	0	0	1	0	0	0	0	0	1	0
	0	1	-	VDCS[6:0]						

This command sets VCOM\_DC value

VDCS[6:0]: VCOM\_DC Setting

VDCS [6:0]	VCOM Voltage (V)	VDCS [6:0]	VCOM Voltage (V)	VDCS [6:0]	VCOM Voltage (V)
000 0000b	-0.10	001 1011b	-1.45	011 0110b	-2.80
000 0001b	-0.15	001 1100b	-1.50	011 0111b	-2.85
000 0010b	-0.20	001 1101b	-1.55	011 1000b	-2.90
000 0011b	-0.25	001 1110b	-1.60	011 1001b	-2.95
000 0100b	-0.30	001 1111b	-1.65	011 1010b	-3.00
000 0101b	-0.35	010 0000b	-1.70	011 1011b	-3.05
000 0110b	-0.40	010 0001b	-1.75	011 1100b	-3.10
000 0111b	-0.45	010 0010b	-1.80	011 1101b	-3.15
000 1000b	-0.50	010 0011b	-1.85	011 1110b	-3.20
000 1001b	-0.55	010 0100b	-1.90	011 1111b	-3.25
000 1010b	-0.60	010 0101b	-1.95	100 0000b	-3.30
000 1011b	-0.65	010 0110b	-2.00	100 0001b	-3.35
000 1100b	-0.70	010 0111b	-2.05	100 0010b	-3.40
000 1101b	-0.75	010 1000b	-2.10	100 0011b	-3.45
000 1110b	-0.80	010 1001b	-2.15	100 0100b	-3.50
000 1111b	-0.85	010 1010b	-2.20	100 0101b	-3.55
001 0000b	-0.90	010 1011b	-2.25	100 0110b	-3.60
001 0001b	-0.95	010 1100b	-2.30	100 0111b	-3.65
001 0010b	-1.00	010 1101b	-2.35	100 1000b	-3.70
001 0011b	-1.05	010 1110b	-2.40	100 1001b	-3.75
001 0100b	-1.10	010 1111b	-2.45	100 1010b	-3.80
001 0101b	-1.15	011 0000b	-2.50	100 1011b	-3.85
001 0110b	-1.20	011 0001b	-2.55	100 1100b	-3.90
001 0111b	-1.25	011 0010b	-2.60	100 1101b	-3.95
001 1000b	-1.30	011 0011b	-2.65	100 1110b	-4.00
001 1001b	-1.35	011 0100b	-2.70	100 1111b	-4.05
001 1010b	-1.40	011 0101b	-2.75		

(34) Partial Window (PTL) (R90h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Window	0	0	1	0	0	1	0	0	0	0
	0	1	-	-	-	-	-	-	HRST[9:8]	
	0	1	HRST[7:3]					0	0	0
	0	1	-	-	-	-	-	-	HRED[9:8]	
	0	1	HRED[7:3]					1	1	1
	0	1	-	-	-	-	-	-	VRST[9:8]	
	0	1	VRST[7:0]							
	0	1	-	-	-	-	-	-	VRED[9:8]	
	0	1	VRED[7:0]							
	0	1	-	-	-	-	-	-	-	PT_SCAN

This command sets partial window.

HRST[9:3]: Horizontal start channel bank. (Value range: 00h~63h)

HRED[9:3]: Horizontal end channel bank. (Value range: 00h~63h). HRED must be greater than HRST.

- VRST[9:0]: Vertical start line. (Value range: 000h~257h)
- VRED[9:0]: Vertical end line. (Value range: 000h~257h). VRED must be greater than VRST.
- PT\_SCAN: 0: Gates scan only inside of the partial window.  
 1: Gates scan both inside and outside of the partial window. (default)

(35) Partial In (PTIN) (R91h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Partial In	0	0	1	0	0	1	0	0	0	1

This command makes the display enter partial mode.

(36) Partial Out (PTOUT) (R92h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Partial Out	0	0	1	0	0	1	0	0	1	0

This command makes the display exit partial mode and enter normal mode.

(37) Program Mode (PGM) (RA0h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Enter Program Mode	0	0	1	0	1	0	0	0	0	0

After this command is issued, the chip would enter the program mode.

After the programming procedure completed, a hardware reset is necessary for leaving program mode.

(38) Active Program (APG) (RA1h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Active Program OTP	0	0	1	0	1	0	0	0	0	1

After this command is transmitted, the programming state machine would be activated.

The BUSY\_N flag would fall to 0 until the programming is completed.

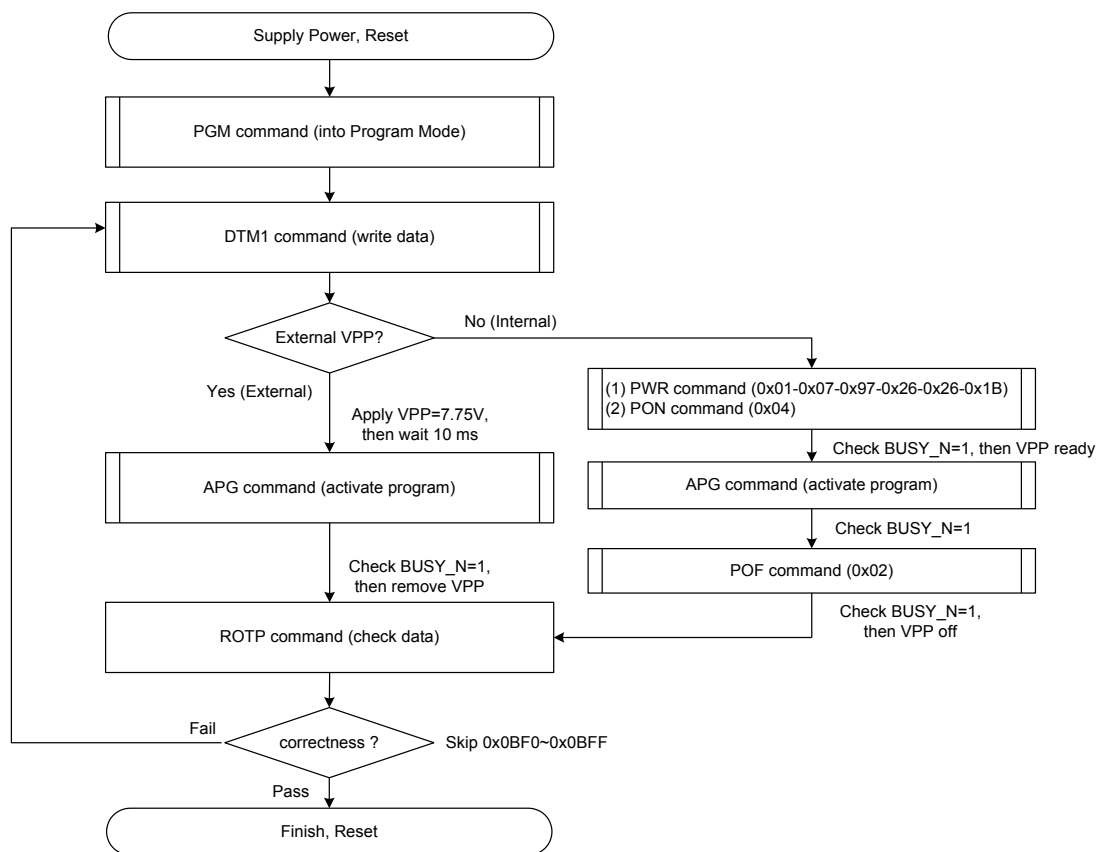
(39) Read OTP Data (ROTP) (RA2h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read OTP data for check	0	0	1	0	1	0	0	0	0	1
	1	1	The data of address 0x000 in the OTP							
	1	1	The data of address 0x001 in the OTP							
	1	1	:							
	1	1	The data of address (n-1) in the OTP							
	1	1	The data of address (n) in the OTP							

The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, the max address = 0x17FF.





The sequence of programming OTP.

(40) Cascade Setting (CCSET) (RE0h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Cascade	0	0	1	1	1	0	0	0	0	0
Option	0	1	-	-	-	-	-	-	TSFIX	CCEN

This command is used for cascade.

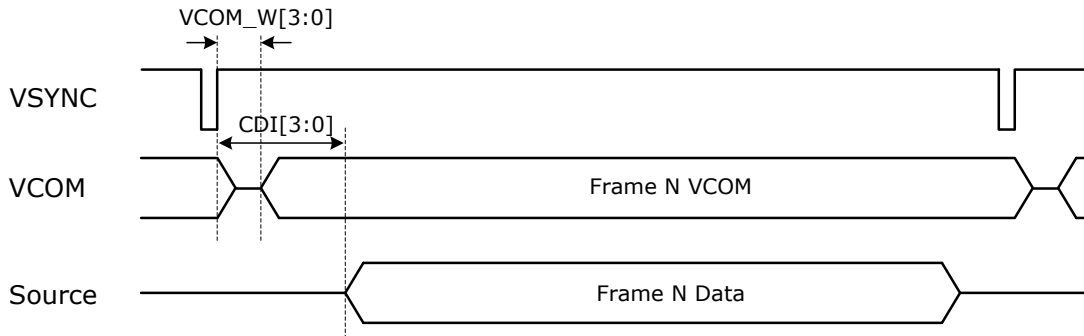
- TSFIX: Let the value of slave's temperature is same as the master's.
- 0: Temperature value is defined by internal temperature sensor / external LM75. (default)
  - 1: Temperature value is defined by TS\_SET[7:0] registers.
- CCEN: Output clock enable/disable.
- 0: Output 0V at CL pin. (default)
  - 1: Output clock at CL pin to slave chip.

(41) Power Saving (PWS) (RE3h)

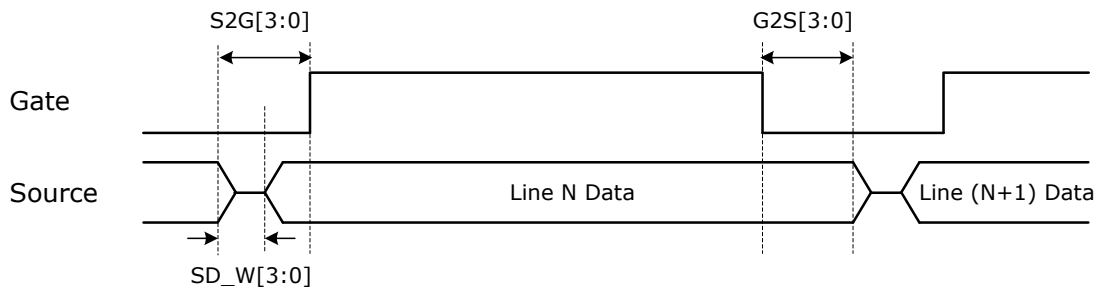
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Power Saving for VCOM & Source	0	0	1	1	1	0	0	0	1	1
	0	1	VCOM_W[3:0]			SD_W[3:0]				

This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM\_W[3:0]: VCOM power saving width (Unit: line period)



SD\_W[3:0]: Source power saving width (Unit: 660nS)



(42) LVD Voltage Select (LVSEL) (RE4h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Select LVD	0	0	1	1	1	0	0	1	0	0
Voltage	0	1	-	-	-	-	-	-	LVD_SEL[1:0]	

LVD\_SEL[1:0]: Low Power Voltage selection

LVD_SEL[1:0]	LVD value
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5 V (default)

(43) Force Temperature (TSSET) (RE5h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Force Temperature Value for Cascade	0	0	1	1	1	0	0	1	0	1
	0	1	TS_SET[7:0]							

This command is used for cascade to fix the temperature value of master and slave chip.

(44) Temperature Boundary Phase-C2 (TSBDRY) (RE7h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Temperature Boundary	0	0	1	1	1	0	0	1	1	1
Phase-C2	0	1	TSBDRY_PHC2[7:0]							

This command is used to set the temperature boundary to judge whether booster phase-C2 is applied or not.

## 7. Electrical Characteristics

### 7-1) Absolute maximum rating

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	$V_{CI}$	-0.3 to +6.0	V
Digital Input Voltage	$V_I$	-0.3 to $V_{DDIO}+0.3$	V
Operating Temp. range	$T_{OPR}$	0 to +40	°C
Storage Temp. range	$T_{STG}$	-25 to +60	°C
Humidity range	-	40~70	%RH

\*Note: Avoid direct sunlight.

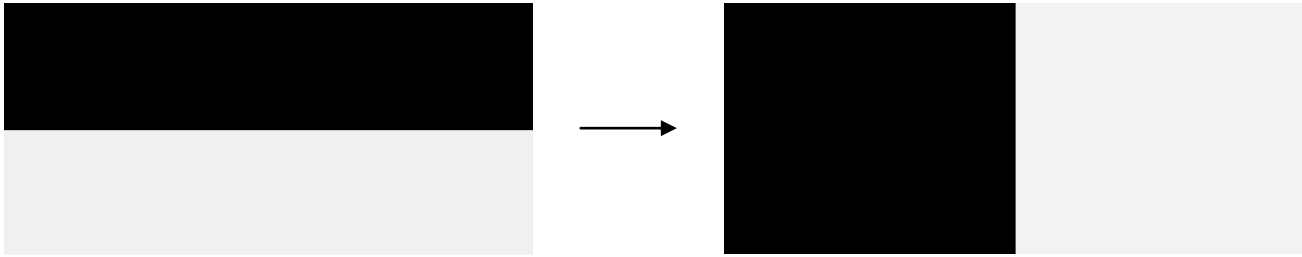
### 7-2) Panel DC Characteristics

The following specifications apply for:  $V_{SS} = 0V$ ,  $V_{CI} = 3.3V$ ,  $T_A = 25^\circ C$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Single ground	$V_{SS}$	-	-	0	-	V
IO supply Voltage	$V_{DDIO}$	-	2.5	3.3	3.6	V
Digital/Analog supply voltage	$V_{DD}$	-	2.5	3.3	3.6	V
High level input voltage	$V_{IH}$	Digital input pins	$0.7V_{IO}$	-	$V_{IO}$	V
Low level input voltage	$V_{IL}$	Digital input pins	0	-	$0.3V_{DD}$	V
High level output voltage	$V_{OH}$	Digital input pins , $I_{OH} = 400\mu A$	$V_{IO}-0.4$	-	-	V
Low level output voltage	$V_{OL}$	Digital input pins , $I_{OL} = -400\mu A$	0	-	0.4	V
Image update current	$I_{UPDATE}$	-	-	25	38	mA
Standby panel current	$I_{STDBY}$	-	-	0.215	0.225	mA
Power panel (update)	$P_{UPDATE}$	-	-	82.5	125.4	mW
Standby power panel	$P_{STBY}$	-	-	0.71	0.81	mW
Operating temperature	-	-	0	-	40	°C
Storage temperature	-	-	-25	-	60	°C
Image update Time at 25 °C	-	-	-	15	20	Sec
Deep sleep mode current	$I_{VCI}$	DC/DC off No clock No input load Ram data not retain	-	2	5	uA

- The Typical power consumption is measured with following pattern transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern.(Note 7-1)
- The standby power is the consumed power when the panel controller is in standby mode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Good Display
- $V_{com}$  is recommended to be set in the range of assigned value  $\pm 0.1V$ .

Note 7-1 The Typical power consumption



### 7-3) Panel AC Characteristics

#### 7-3-1) Oscillator frequency

The following specifications apply for: VSS = 0V, VCI = 3.3V, TA = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal Oscillator frequency	Fosc	VCI=2.3 to 3.6V	-	1.625	-	MHz

#### 7-3-2) MCU Interface

##### 7-3-2-1) MCU Interface Selection

In this module, there are 4-wire SPI and 3-wire SPI that can communicate with MCU. The MCU interface mode can be set by hardware selection on BS pins. When it is “Low”, 4-wire SPI is selected. When it is “High”, 3-wire SPI (9 bits SPI) is selected.

Pin Name	Data/Command Interface		Control Signal		
	D1	D0	CSB	DC	RST_N
Bus interface	SDA	SCL	CSB	DC	RST_N
SPI4	SDA	SCL	CSB	L	RST_N

**Table 7-1:** MCU interface assignment under different bus interface mode

Note 7-2: L is connected to VSS

Note 7-3: H is connected to VCI

**7-3-2-2) MCU Serial Interface (4-wire SPI)**

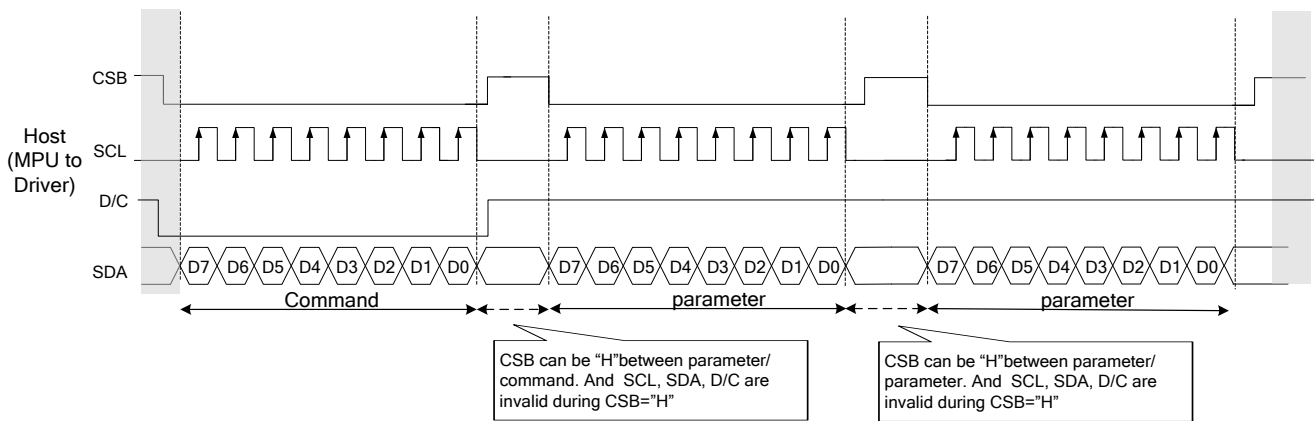
The 4-wire SPI consists of serial clock SCL, serial data SDA, DC, CSB. In SPI mode, D0 acts as SCL, D1 acts as SDA.

Function	CSB	DC	SCL
Write Command	L	L	↑
Write data	L	H	↑

**Table 7-2:** Control pins of 4-wire Serial Peripheral interface

Note 7-4: ↑stands for rising edge of signal

SDA is shifted into an 8-bit shift register in the order of D7, D6, ... D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.



**Figure 7-1:** Write procedure in 4-wire Serial Peripheral Interface mode

**7-3-2-3) MCU Serial Interface (3-wire SPI)**

The 3-wire serial interface consists of serial clock SCL, serial data SDA and CSB.

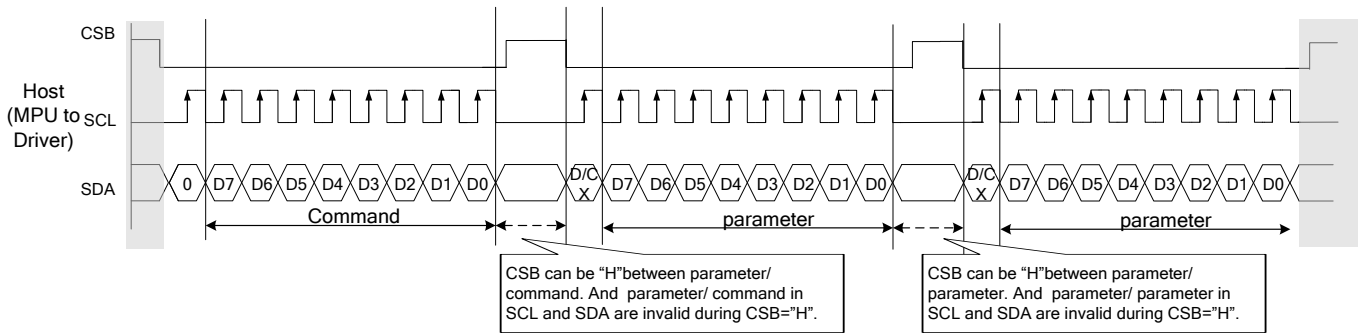
In 3-wire SPI mode, D0 acts as SCL, D1 acts as SDA, The pin DC can be connected to an external ground.

The operation is similar to 4-wire serial interface while DC pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: DC bit, D7 to D0 bit. The DC bit (first bit of the sequential data) will determine the following data byte in shift register is written to the Display Data RAM (DC bit = 1) or the command register (DC bit = 0). Under serial mode, only write operations are allowed.

Function	CSB	DC	SCL
Write Command	L	Tie LOW	↑
Write data	L	Tie LOW	↑

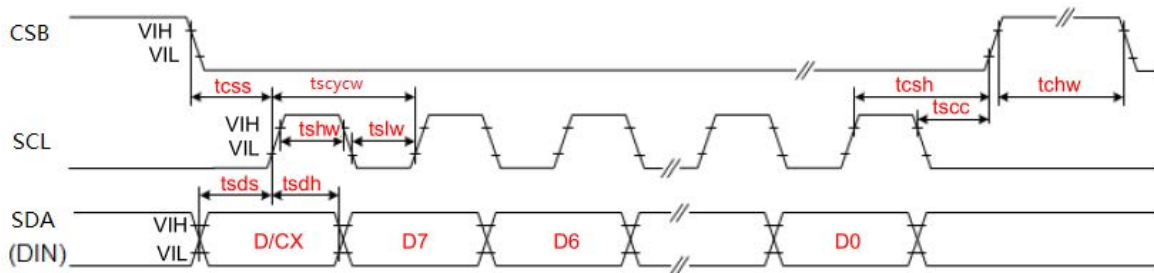
**Table 7-3:** Control pins of 3-wire Serial Peripheral Interface

Note 7-5: ↑stands for rising edge of signal

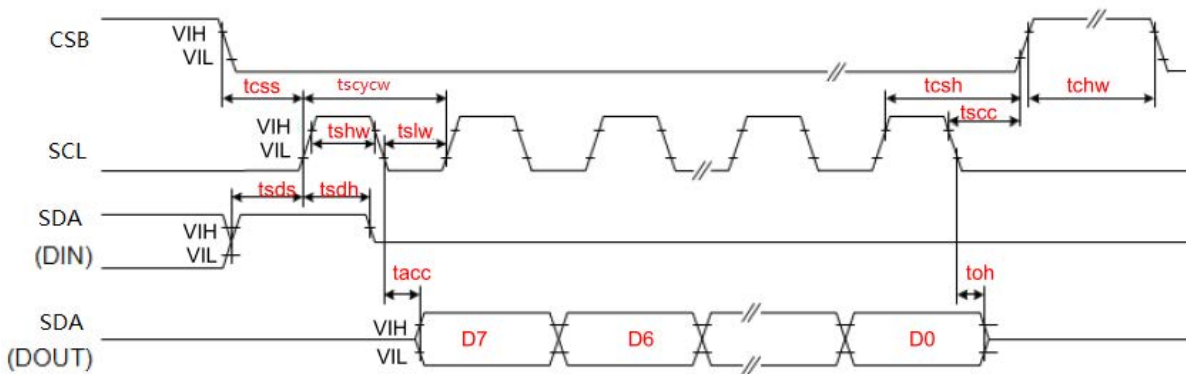


**Figure 7-2:** Write procedure in 3-wire Serial Peripheral Interface mode

7-3-3) Timing Characteristics of Series Interface



3-wire Serial Interface – Write



3-wire Serial Interface – Read

bol	Signal	Parameter	Min	Typ	Max	Unit
tcss	CSB	Chip Select Setup Time	100	-	-	ns
tsh		Chip Select Hold Time	100	-	-	ns
tsc		Chip Select Setup Time	50	-	-	ns
tch		Chip Select Setup Time	500	-	-	ns
tscycw	SCL	Serial clock cycle (write)	100	-	-	ns
tshw		SCL "H" pulse width (write)	35	-	-	ns
tslw		SCL "L" pulse width (write)	35	-	-	ns
tscycr		Serial clock cycle (Read)	200	-	-	ns
tshr		SCL "H" pulse width (Read)	85	-	-	ns
tslr		SCL "L" pulse width (Read)	85	-	-	ns
tsds	SDA (DIN)	Data setup time	30	-	-	ns
tsdh		Data hold time	30	-	-	ns
tacc	SDA (DOUT)	Access time	10	-	-	ns
toh		Output disable time	15	-	-	ns
tcds	D/C	DC setup time	20	-	-	ns
tcdh		DC hold time	20	-	-	ns

7-4) Reference Circuit

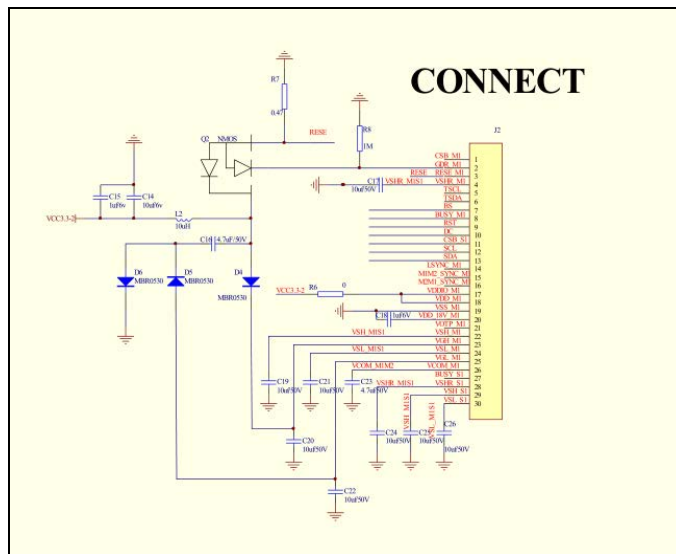


Figure . 7-4 (1)

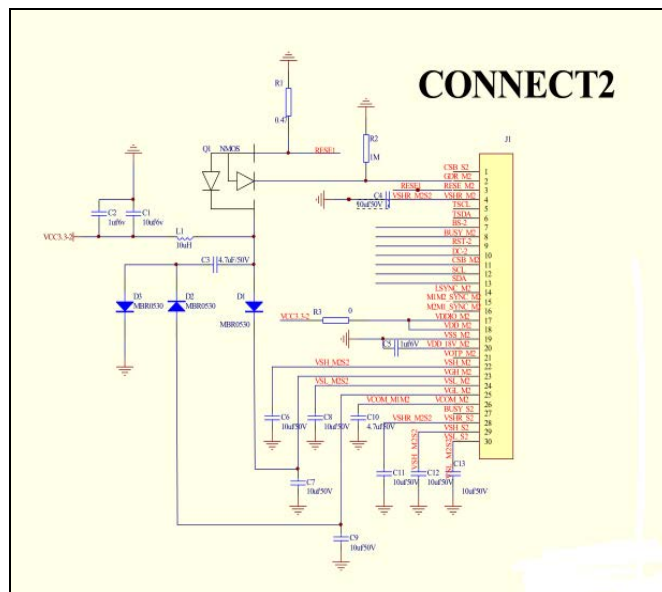


Figure . 7-4 (2)

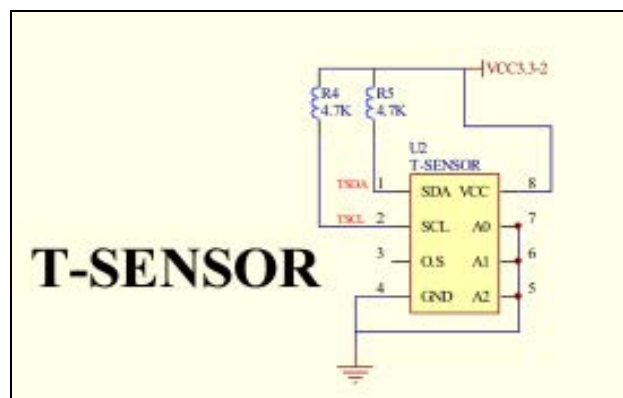


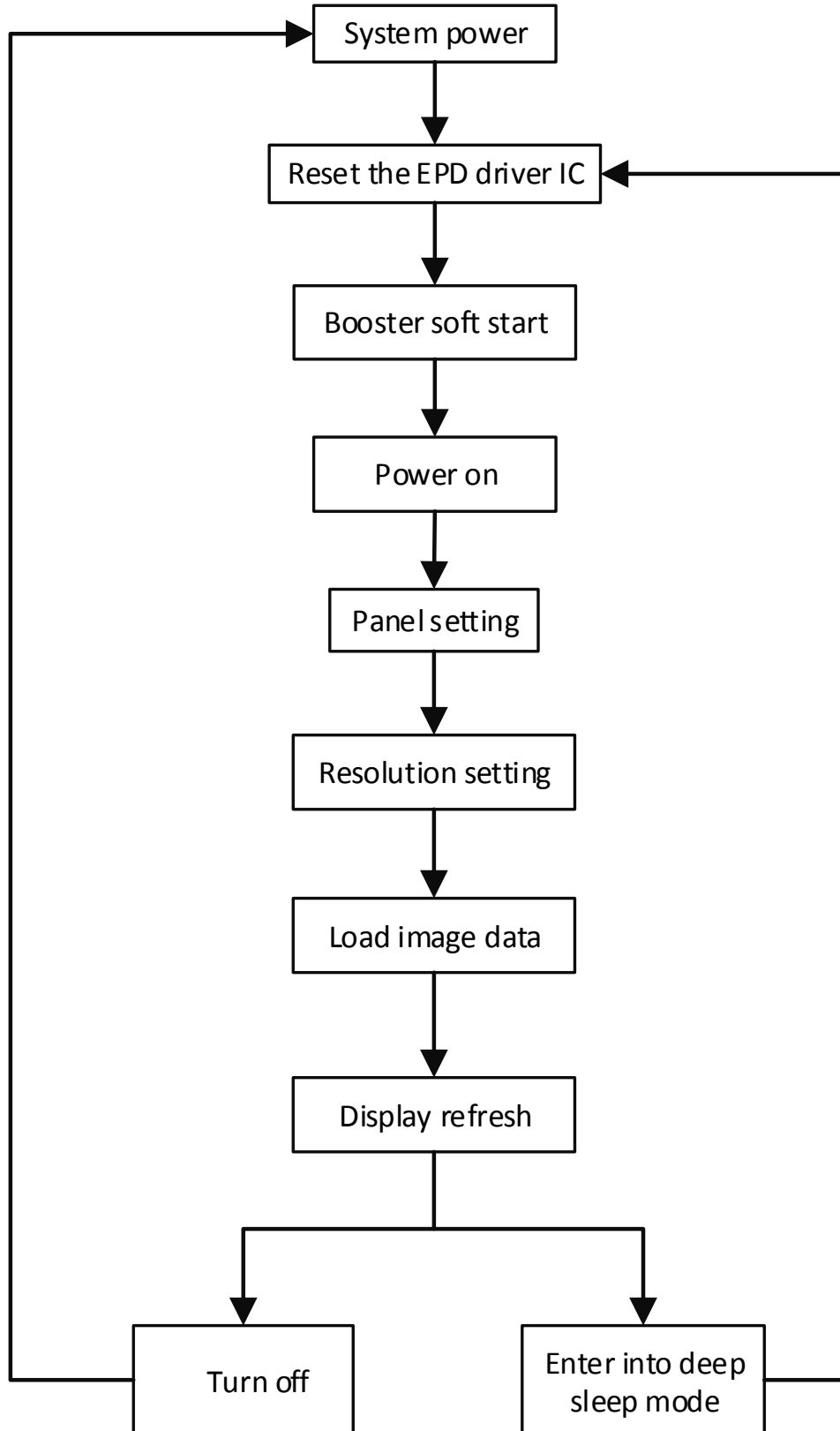
Figure . 7-4 (3)



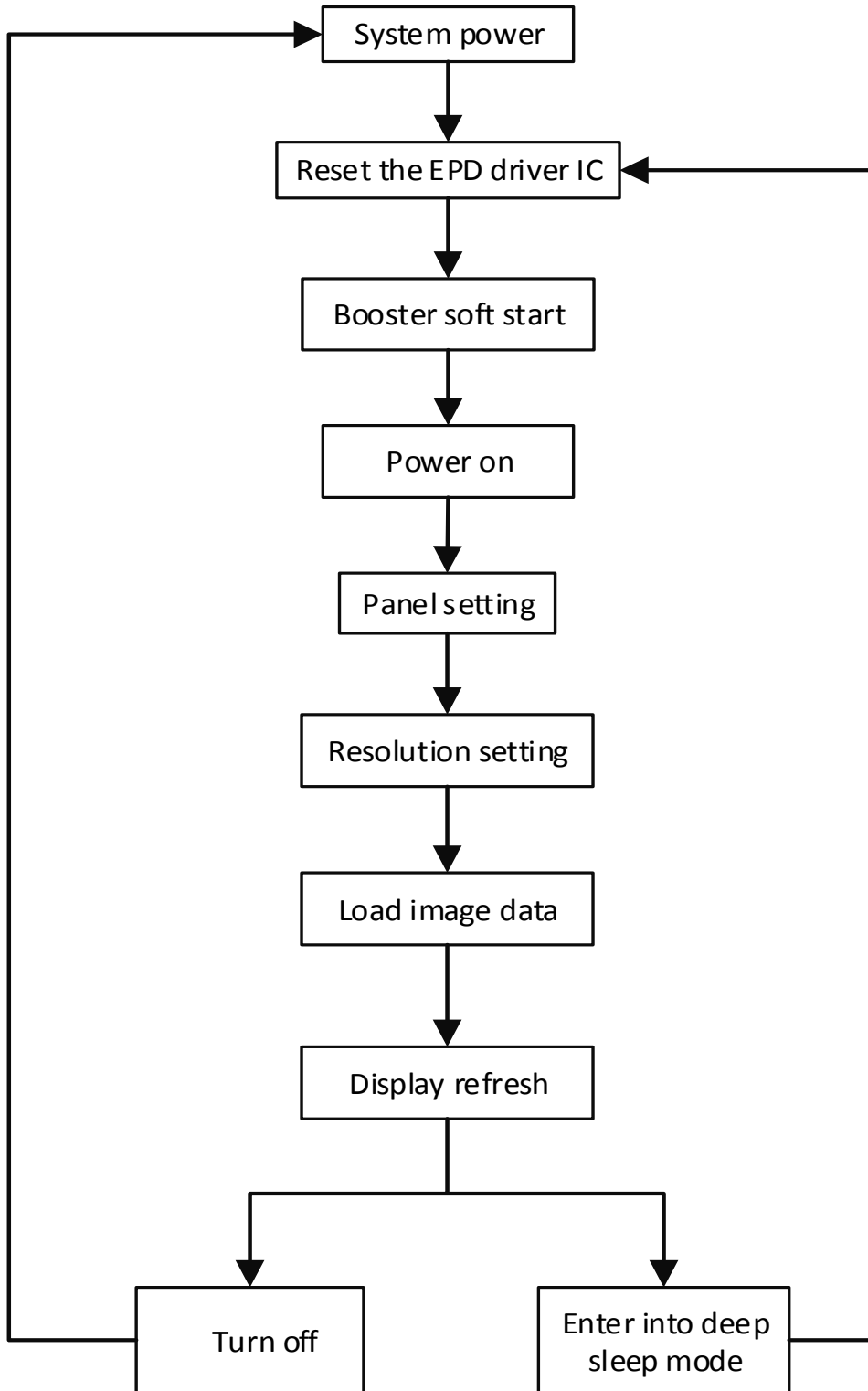
8. Typical Operating Sequence

8-1) Normal Operation Flow

1. BWR mode & LUT from Register

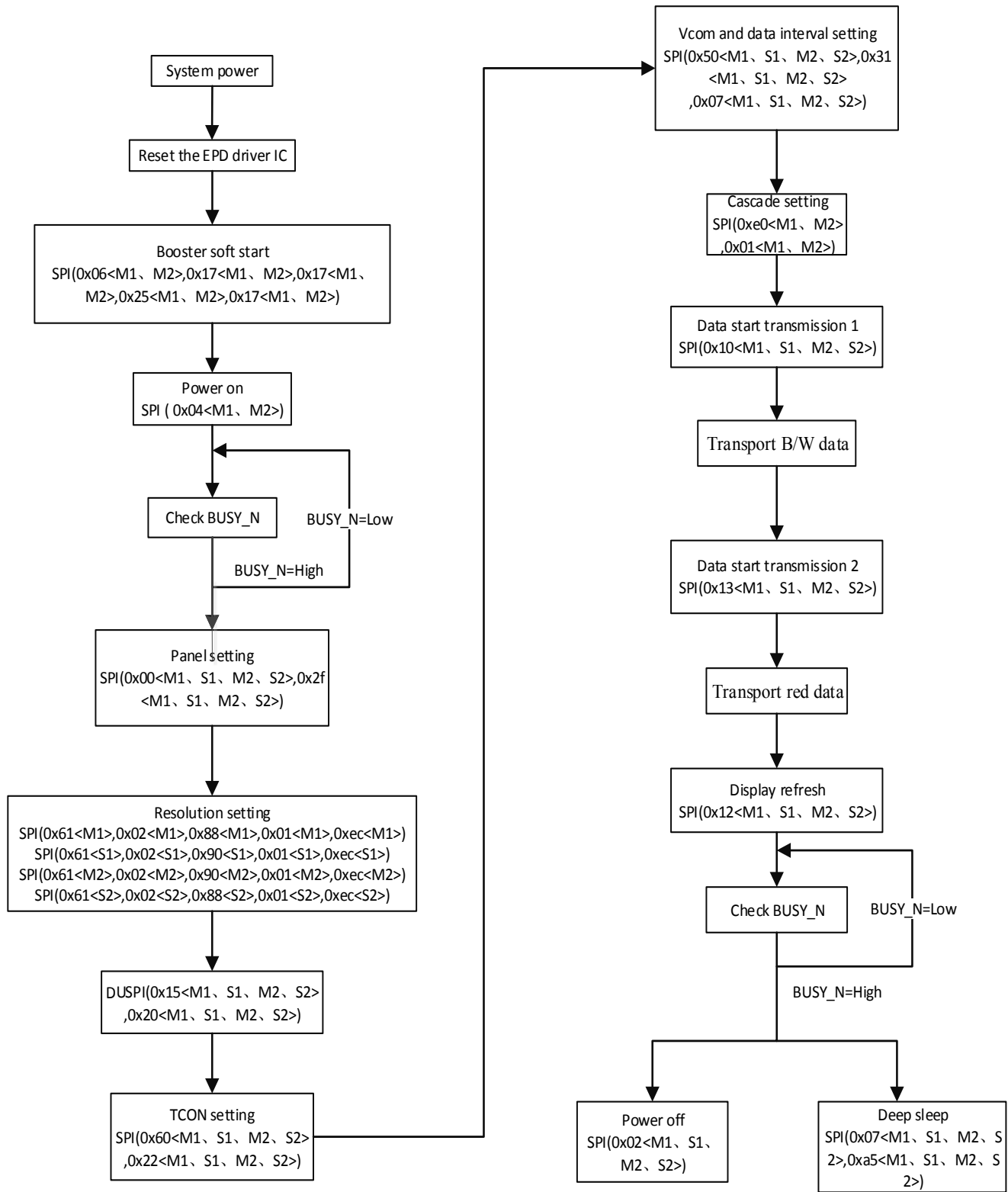


2. BWR mode & LUT from OTP



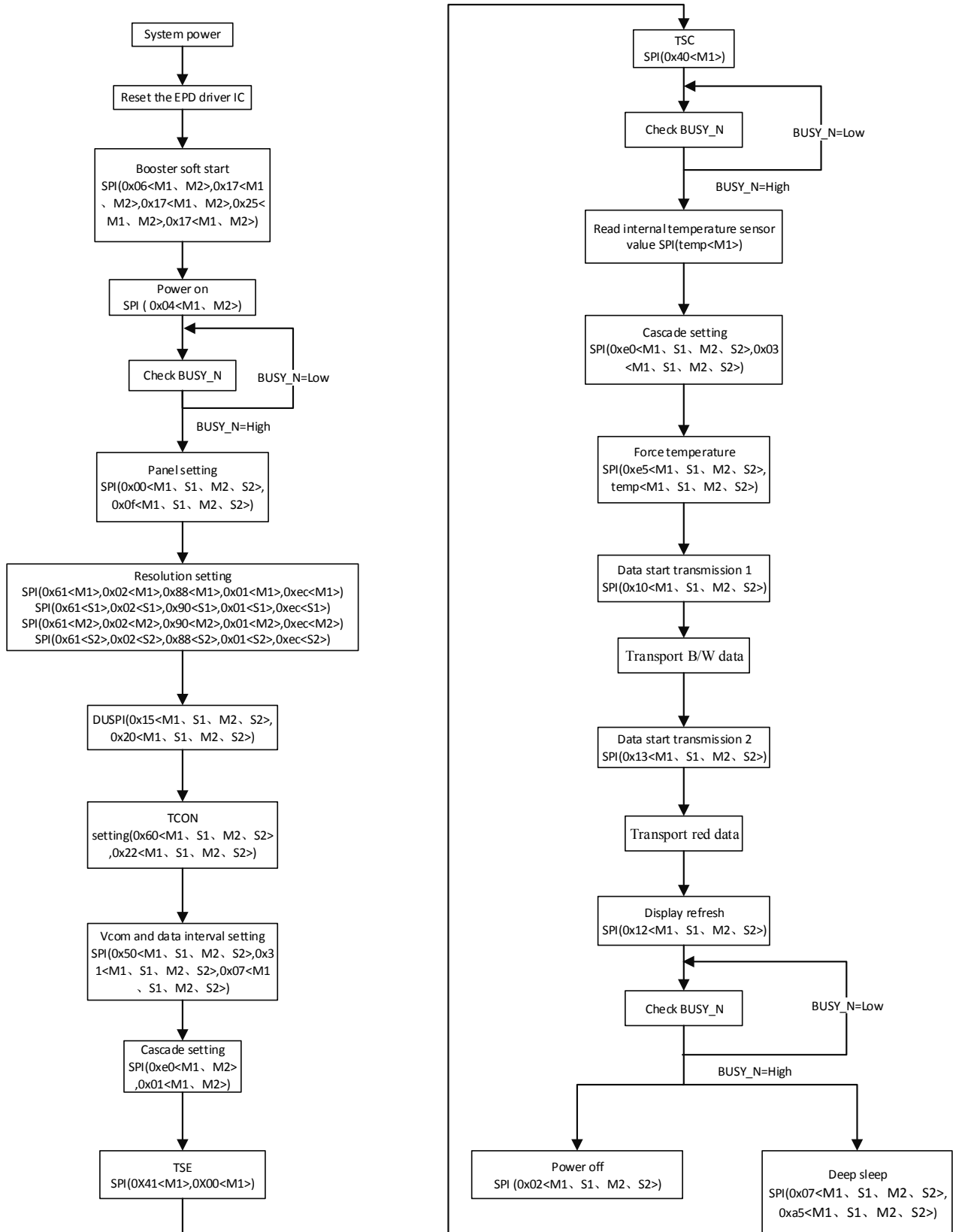
8-2) Reference Program Code

1. BWR mode & LUT from register



Note1: Set border to floating.

2. BWR mode & LUT from OTP



Note1: Set border to floating.

8. Optical characteristics

9-1) Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYPE	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 9-1
Gn	2Grey Level	-	-	$DS+(WS-DS) \times n(m-1)$	-	L*	-
CR	Contrast Ratio	indoor	8		-	-	-
Panel's life		0°C~40°C		1000000 times or 5 years			Note 9-2

WS : White state, DS : Dark state

Gray state from Dark to White : DS、WS

m : 2

Note 9-1 : Luminance meter : Eye – One Pro Spectrophotometer

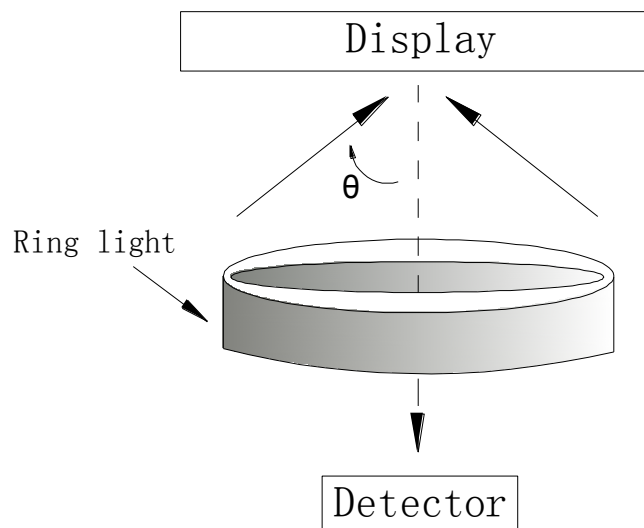
Note 9-2 : Panel life will not guaranteed when work in temperature below 0 degree or above 50 degree. Each update interval time should be minimum at 180 seconds.

9-2) Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd) :

R1: white reflectance      Rd: dark reflectance

$$CR = R1/Rd$$

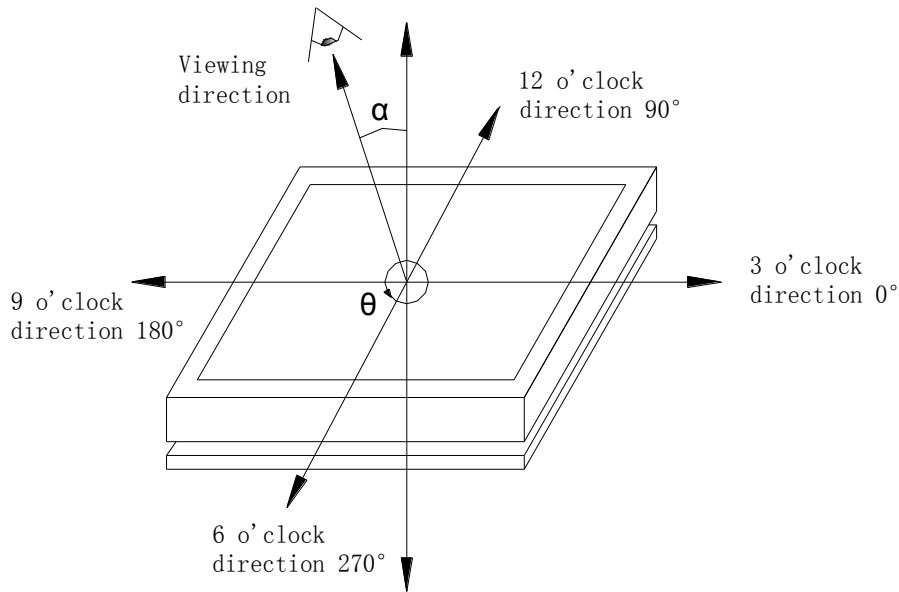


**9-3) Reflection Ratio**

The reflection ratio is expressed as :

$$R = \text{Reflectance Factor}_{\text{white board}} \times (L_{\text{center}} / L_{\text{white board}})$$

$L_{\text{center}}$  is the luminance measured at center in a white area ( $R=G=B=1$ ) .  $L_{\text{white board}}$  is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



**9-4) Bi-stability**

The Bi-stability standard as follows:

Bi-stability	Result		
		AVG	MAX
24 hours Luminance drift	White state $\Delta L^*$	-	3
	Black state $\Delta L^*$	-	3

## 9. Handling, Safety and Environmental Requirements

<b>Warning</b>
<p>The display glass may break when it is dropped or bumped on a hard surface. Handle with care.</p> <p>Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.</p>

<b>Caution</b>
<p>The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.</p> <p>Disassembling the display module can cause permanent damage and invalidate the warranty agreements.</p>

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

<b>Data sheet status</b>	
Product specification	The data sheet contains final product specifications.
<b>Limiting values</b>	
<p>Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134).</p> <p>Stress above one or more of the limiting values may cause permanent damage to the device.</p> <p>These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.</p>	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

<b>Product environmental certification</b>
RoHS

**10. Reliability test**

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = 40°C, RH=35%, for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the high temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Bp.	When experiment finished, the EPD must meet electrical and optical performance standards.
2	Low-Temperature Operation	T = 0°C for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the low temperature environmental chamber and set aside for a few minutes. As EPDs return room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Ab.	When experiment finished, the EPD must meet electrical and optical performance standards.
3	High-Temperature Storage	T = +60°C, RH= 35%, for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the high temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Bp.	When experiment finished, the EPD must meet electrical and optical performance standards.
4	Low-Temperature Storage	T = -25°C for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the low temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Ab	When experiment finished, the EPD must meet electrical and optical performance standards.
5	High Temperature, High-Humidity Operation	T=+40°C, RH=80% for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-3CA.	When experiment finished, the EPD must meet electrical and optical performance standards.
6	High Temperature, High-Humidity Storage	T=+50°C, RH=80% for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-3CA.	When experiment finished, the EPD must meet electrical performance standards.
7	Temperature Cycle	[-25°C 30mins]→ [+60°C, RH=35% 30mins], 50cycles Test in white	1. Samples are put in the Temp & Humid. Environmental Chamber. Temperature cycle starts with -25°C, storage period 30 minutes. After 30 minutes, it needs 30min to let temperature rise to 60°C. After 30min, temperature will be adjusted to 60°C, RH=35% and storage period	When experiment finished, the EPD must meet electrical and optical performance



		pattern	<p>is 30 minutes. After 30 minutes, it needs 30min to let temperature rise to -25°C. One temperature cycle (2hrs) is complete.</p> <p>2. Temperature cycle repeats 50 times.</p> <p>3. When 50 cycles finished, the samples will be taken out from experiment chamber and set aside a few minutes. As EPDs return to room temperature, tests will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-14NB.</p>	standards.
8	UV exposure Resistance	765 W/m <sup>2</sup> for 168 hrs,40°C	Standard # IEC 60 068-2-5 Sa	
9	Electrostatic discharge	Machine model: +/-250V, 0Ω ,200pF	Standard # IEC61000-4-2	
10	Package Vibration	1.04G,Frequency : 10~500Hz Direction : X,Y,Z Duration:1 hours in each direction	Full packed for shipment	
11	Package Drop Impact	Drop from height of 122 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment	

Actual EMC level to be measured on customer application.

Note: (1) The protective film must be removed before temperature test.

(2) There's temperature vs display quality limitation in our display module, we guarantee 1 pixel display quality from 0°C ~ 40°C.

(3) In order to make sure the display module can provide the best display quality, the update should be made after putting the display module in stable temperature environment for 4 hours at 25°C.

**11. Point and line standard**

Shipment Inseption Standard

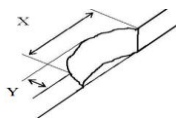
Part-A: Active area Part-B: Border area

Equipment: Electrical test fixture, Point gauge

Outline dimension:

261.5(H)×211(V)×1.18(D)

Unit: mm

Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle
	23±2℃	55±5%RH	1200~1500Lux	300 mm	35 Sec	
Name	Causes	Spot size		Part-A	Part-B	
Spot	B/W spot in glass or protection sheet, foreign mat. Pin hole	D ≤ 0.25mm		Ignore	Ignore	
		0.25mm < D ≤ 0.4mm		4		
		0.4mm < D ≤ 0.5mm		1		
		0.5mm < D		0		
Scratch or line defect	Scratch on glass or Scratch on FPL or Particle is Protection sheet.	Length	Width	Part-A	Ignore	
		L ≤ 2.0mm	W ≤ 0.2 mm	Ignore		
		2.0 mm < L ≤ 8.0mm	0.2 mm < W ≤ 0.5mm	2		
		8.0 mm < L	0.5mm < W	0		
Air bubble	Air bubble	D1, D2 ≤ 0.25 mm		Ignore	Ignore	
		0.25 mm < D1, D2 ≤ 0.4mm		4		
		0.4mm < D1, D2		0		
Side Fragment						
	X ≤ 6mm, Y ≤ 1mm & display is ok, Ignore					

Remarks: Spot define: That only can be seen under WS or DS defects.

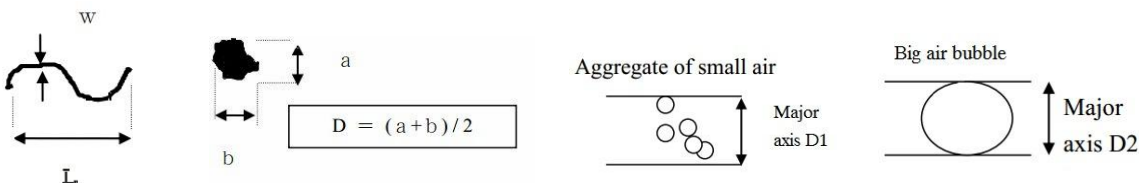
Any defect which is visible under gray pattern or transition process but invisible under black and white is disregarded.

Here is definition of the “Spot” and “Scratch or line defect”.

Spot:  $W > 1/4L$  Scratch or line defect:  $W \leq 1/4L$

Definition for L/W and D (major axis)

FPC bonding area pad doesn't allowed visual inspection.



Note: AQL = 0.4

**12. Packing**

