Specification For HINK 2.13''EPD

Model NO.: HINK-E0213A167

Product VER:A0

Customer Approval

Customer	
Approval By	
Date Of Approval	

It will be agreed by the receiver, if not sign back the Specification within 15days.

Prepared By	Checked By	Approval By
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Version	Content	Date	Producer
A0	New release	2021/02/23	Daisy Zhu

CONTENTS

1. General Description

HINK-E0213A167 is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design. The 2.13" active area contains 122×250 pixels, and has 1-bit B/W full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

2. Features

- 122×250 pixels display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C signal master interface to read external temperature sensor/built-in temperature sensor

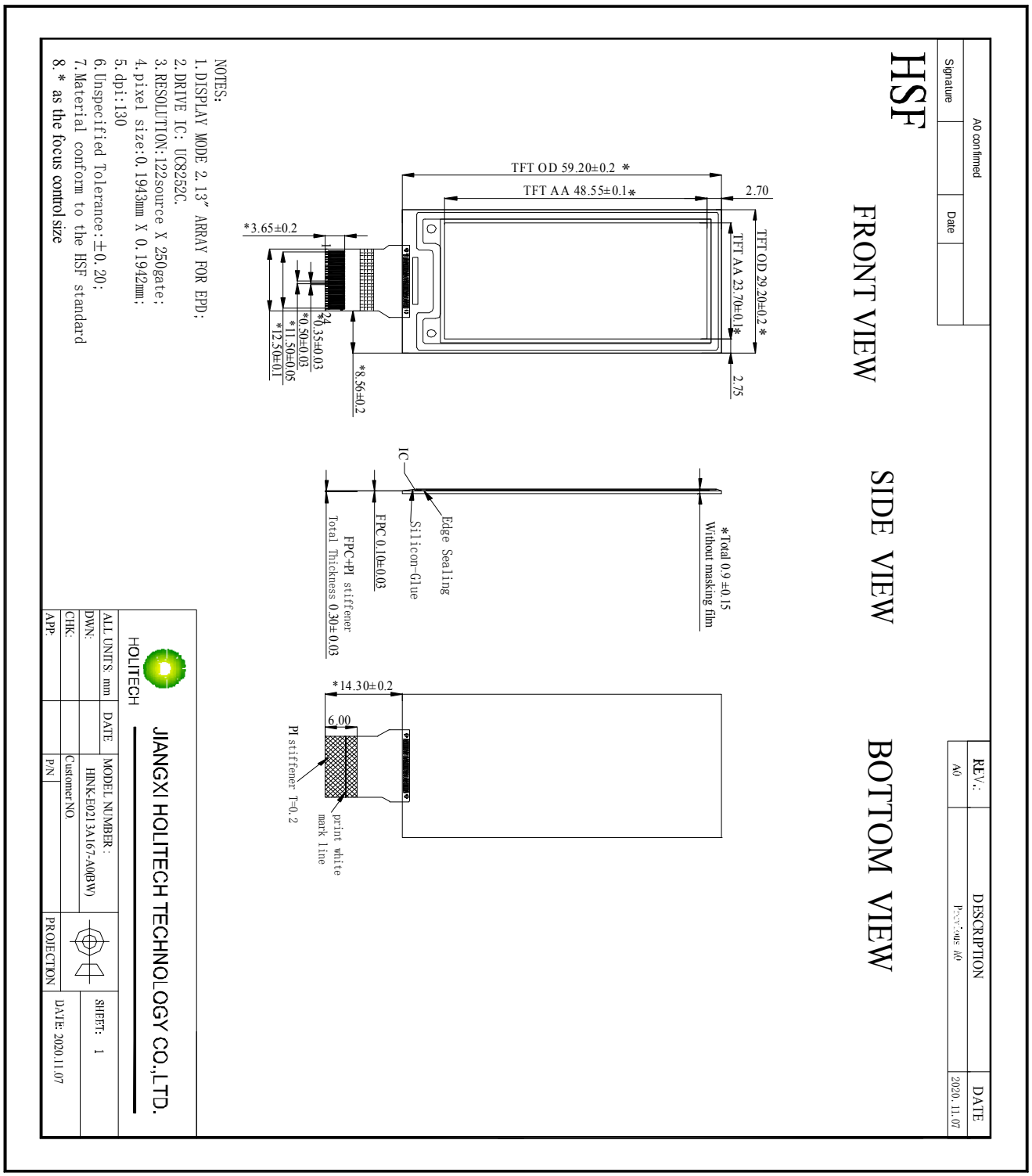
3. Application

Electronic Shelf Label System

4. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.13	Inch	
Display Resolution	122(H)×250(V)	Pixel	Dpi:111
Active Area	23.70(H)×48.55(V)	mm	
Pixel Pitch	0.194×0.194	mm	
Pixel Configuration	Rectangle		
Outline Dimension	29.2(H)×59.2 (V) ×0.9 (D)	mm	Without masking film
Weight	3±0.5	g	

5. Mechanical Drawing of EPD module



6. Input/Output Terminals

Pin #	Single	Description	Remark
1	NC	Not Connected	Keep Open
2	GDR	N-MOS gate control	
3	RESE	Current sense input for control loop	
4	NC	Not Connected	Keep Open
5	VDHR	Positive source driver voltage for Red	
6	TSCL	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I2C Interface to digital temperature sensor Data pin	
8	BS	Bus Selection	Note 6-5
9	BUSY_N	Driver busy flag	Note 6-4
10	RST_N	Global reset pin	Note 6-3
11	DC	Command/Data input	Note 6-2
12	CSB	Serial communication chip select	Note 6-1
13	SCL	Serial communication clock input	
14	SDA	Serial communication data input/output	
15	VDDIO	IO power	
16	VDD	Digital power	
17	GND	Digital Ground	
18	VDDD	Digital power input	
19	VPP	OTP program power	
20	VSH	Positive source driver Voltage	
21	VGH	Positive Gate voltage	
22	VSL	Negative source driver voltage	
23	VGL	Negative Gate voltage	
24	VCOM	VCOM output	

Note 6-1: This pin (CSB) is the chip select input connecting to the MCU. The chip is enabled for MCU communication: only when CSB is pulled LOW.
Note 6-2: This pin (DC) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Note 6-3: This pin (RST_N) is reset signal input. When RST_N become LOW, driver will reset. All register will reset to default value. Driver all function will disable

Note 6-4: This pin (BUSY_N) is Busy state output pin. When Busy_N is LOW, the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy_N pin LOW when the driver IC is working such as:

- Outputting display waveform;
- Communicating with digital temperature sensor

Note 6-5: This pin (BS) is for 3-wire SPI or 4-wire SPI selection. When it is "Low", 4-wire SPI is selected. When it is "High", 3-wire SPI (9 bits SPI) is selected.

7. MCU Interface

7.1 MCU interface selection

E0213A167 can provide 3-wire/4-wire serial interface for command and display data transferred from the MCU. The serial interface supports 8-bit mode. Data can be input/output by clocks while the EPD module is active (CSB =LOW). While input, data are written in order from MSB at the clock rising edge. When too many parameters are input, the EPD module accepts only defined parameters, and ignores undefined ones.

BS	Interface	CSB	DC	SCL	SDA
High	3-Wire SPI	Available	Fix to GND	Available	Available
Low	4-Wire SPI	Available	Available	Available	Available

7.2 MCU Serial Peripheral Interface (4-wire SPI)

Data / Command is recognized with DC pin. Data are transferred in the unit of 8 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 8 bits. (The serial counter is reset at the rising edge of the CSB signal.)

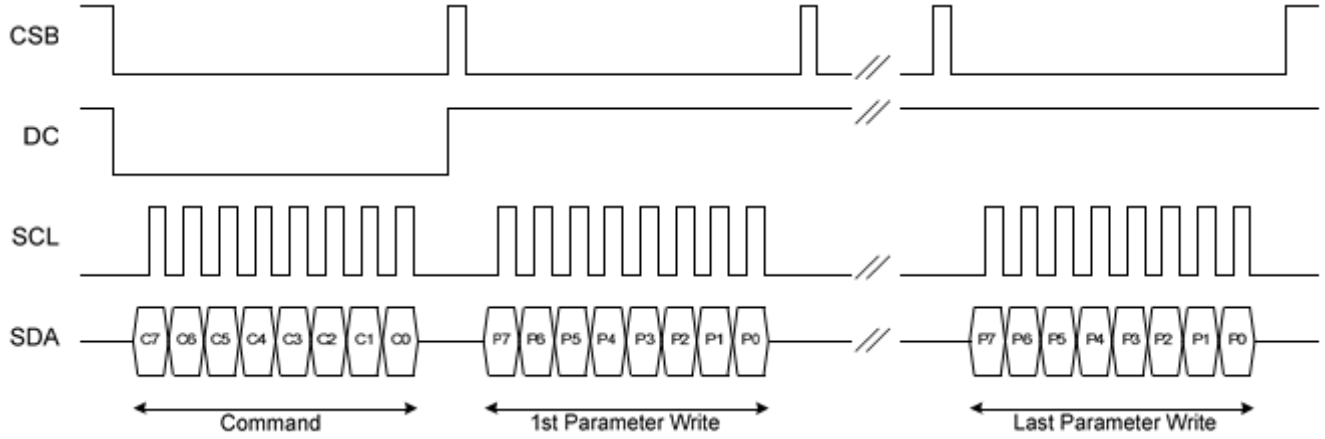


Figure: 4-wire SPI write opera

The MSB bit of data will be output at SDA pin after the CSB falling edge, if DC pin is High. Only in the case of OTP data read, the 1st packet of output data are dummy data.

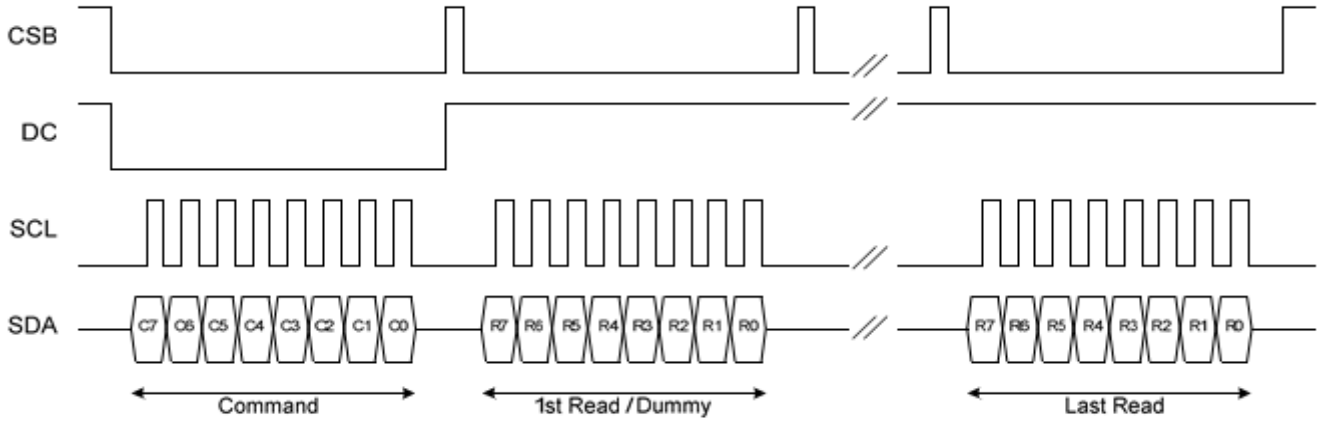


Figure: 4-wire SPI read operation

7.3 MCU Serial Peripheral Interface (3-wire SPI)

Data / Command is recognized with the first bit transferred. Data are transferred in the unit of 9 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 9 bits. (The serial counter is reset at the rising edge of the CSB signal.)

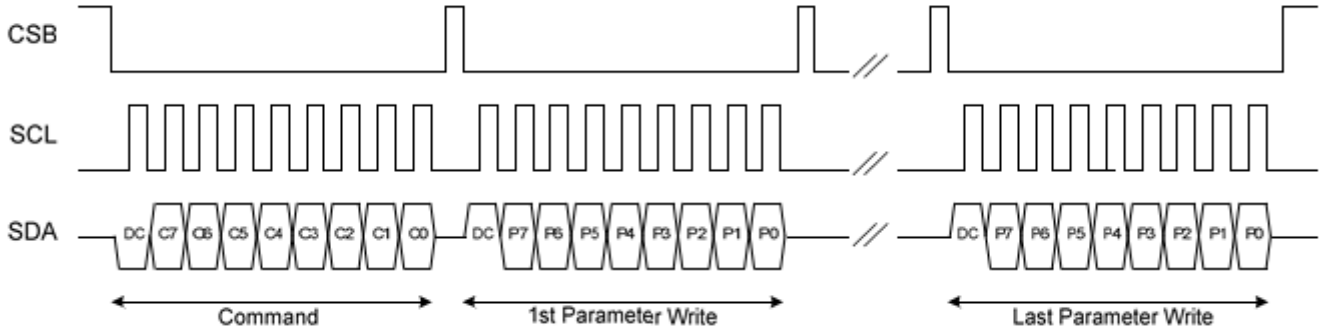


Figure: 3-wire SPI write operation

The MSB bit of data will be output at SDA pin after the 1st SCL falling edge, if the 1st input data at SDA is high. Only in the case of OTP data read, the 1st packet of output data are dummy data.

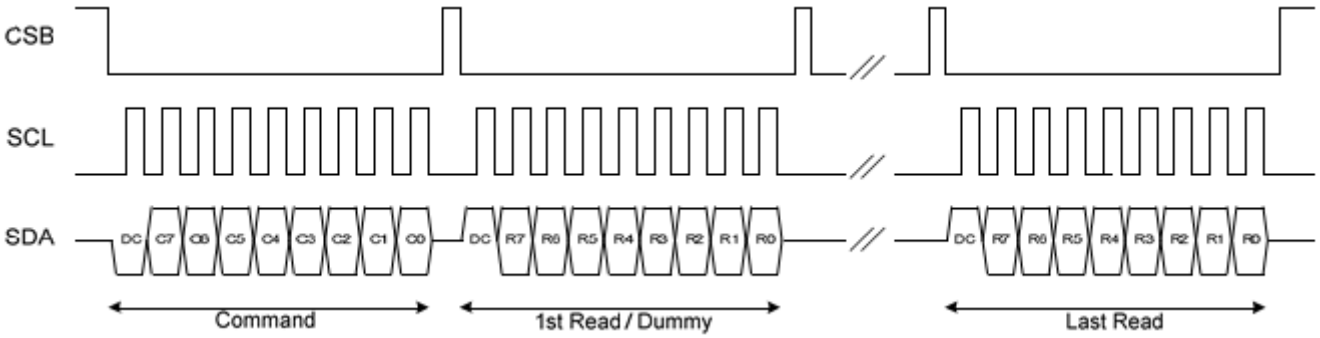


Figure: 3-wire SPI read operation

8. COMMAND TABLE

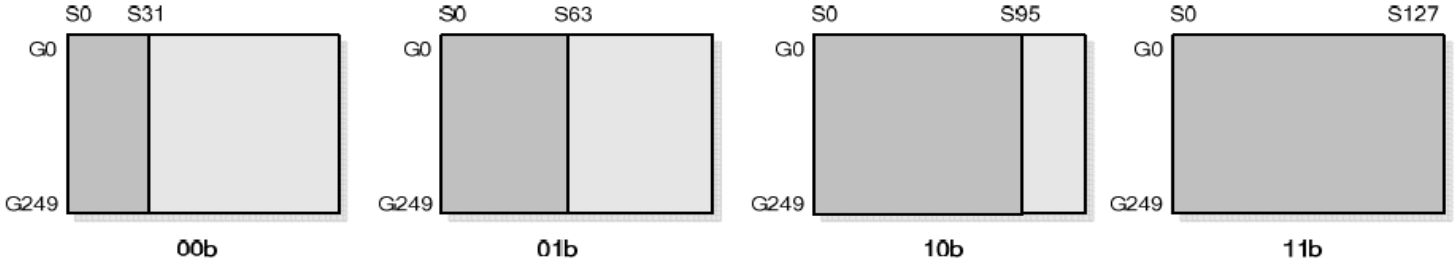
W/R: 0: Write Cycle / 1: Read Cycle C/D: 0: Command / 1: Data D7-D0: –: Don't Care

(1) PANEL SETTING (PSR) (REGISTER: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting the panel	0	0	0	0	0	0	0	0	0	0	00H
	0	1	RES1	RES0	REG	KW/R	UD	SHL	SHD_N	RST_N	0FH

RES[1:0]: Display Resolution setting (source x gate)

00b:32x250 (Default) Active source channels: S0 ~ S31. Active gate channels: G0 ~ G249.
01b:64x250 Active source channels: S0 ~ S63. Active gate channels: G0 ~ G249.
10b:96x250 Active source channels: S0 ~ S95. Active gate channels: G0 ~ G249.
11b:128x250 Active source channels: S0 ~ S127. Active gate channels: G0 ~ G249.



REG: LUT selection

0: LUT from OTP. (Default)
1: LUT from register.

KW/R: Black / White / Red

0: Pixel with Black/White/Red, KWR mode. (Default)
1: Pixel with Black/White, KW mode.

UD: Gate Scan Direction

0: Scan down. First line to Last line: Gn-1→ Gn-2 →Gn-3→ … →G0
1: Scan up. (Default) First line to Last line: G0 → G1 → G2 → … … . → Gn-1

SHL: Source Shift Direction

0: Shift left. First data to Last data: Sn-1 →Sn-2 → Sn-3 → …→ S0
1: Shift right. (Default) First data to Last data: S0 → S1 → S2 → … … . →Sn-1

SHD_N: Booster Switch

0: Booster OFF
1: Booster ON (Default)

When SHD_N becomes LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF. And Source/Gate/Border/VCOM will be released to floating.

RST_N: Soft Reset

0: Reset. Booster OFF, Register data are set to their default values, all drivers will be reset, and all functions will be disabled. Source/Gate/Border/VCOM will be released to floating. After soft reset is transmitted, the internal operation needs at least 50uS to execute. During this period of time, the BUSY_N pin keeps low and any command will be ignored.

1: No effect (Default).

(2) POWER SETTING (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Selecting Internal/External Power	0	0	0	0	0	0	0	0	0	1	01H
	0	1	-	-	-		-	-	VDS_EN	VDG_EN	03H
	0	1	-	-	-		VGHL[3:0]				00H
	0	1	-	-	VSH[5:0]						3FH
	0	1	-	-	VSL[5:0]						3FH
	0	1	OPTEN	VDHR[6:0]							0DH

VDS_EN: Source power selection
0 : External source power from VSH/VSL/VDHR pins
1 : Internal DC/DC function for generating VSH/VSL/VDHR. (Default)

VDG_EN: Gate power selection
0: External gate power from VGH/VGL pins
1: Internal DC/DC function for generating VGH/VGL. (Default)

VGHL[3:0]:VGH / VGL Voltage Level selection.

VGHL	VGH/VGL Voltage Level
0000 (Default)	VGH=20V, VGL= -20V

VSH[5:0]: Internal VSH power selection for B/W pixel.(Default value: 111111b)

VSH	Voltage
11 1111	**15.0 V**

VSL[5:0]: Internal VSL power selection for B/W pixel. (Default value: 111010b)

VSL	Voltage
11 1111	**-15.0 V**

VDHR[5:0]: Internal VDHR power selection for Red pixel. (Default value: 001101b)

VDHR	Voltage
001101	**5.0 V**

(3) POWER OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning OFF the power	0	0	0	0	0	0	0	0	1	0	02H

After the Power OFF command, the driver will be powered OFF. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn off booster, controller, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD turned OFF or Deep Sleep Mode. Source/Gate/Border/VCOM will be released to floating.

(4)POWER OFF SEQUENCE SETTING (PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1	03H
	0	1	-	-	T_VDS_OFF[1:0]		-	-	-	-	*00H*

T_VDS_OFF[1:0]: Source to gate power off interval time.

00b: 1 frame (Default) 01b: 2 frames 10b: 3 frames 11b: 4 frame

(5)POWER ON (PON) (REGISTER: R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning ON the power	0	0	0	0	0	0	0	1	0	0	04H

After the Power ON command, the driver will be powered ON. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn on booster, controller, regulators, and temperature sensor will be activated for one-time sensing before enabling booster. When all voltages are ready, the BUSY_N signal will return to high.

(6)BOOSTER SOFT START (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	0	0	1	1	0	06H
	0	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0	17H
	0	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0	17H
	0	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0	17H

BTPHA[7:6]: Soft start period of phase A.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHA[5:3]: Driving strength of phase A

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHA[2:0]: Minimum OFF time setting of GDR in phase A

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHB[7:6]: Soft start period of phase B.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHB[5:3]: Driving strength of phase B

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHB[2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHC[5:3]: Driving strength of phase C

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHC[2:0] : Minimum OFF time setting of GDR in phase C

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

(7)DEEP SLEEP (DSLP)(R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Deep Sleep	0	0	0	0	0	0	0	1	1	1	07H
	0	1	1	0	1	0	0	1	0	1	A5H

After this command is transmitted, the chip will enter Deep Sleep Mode to save power. Deep Sleep Mode will return to Standby Mode by hardware reset. The only one parameter is a check code, the command will be executed if check code = 0xA5.

(8)DATA START TRANSMISSION 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	0	0	10H
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	-
	0	1	:	:	:	:	:	:	:	:	-
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	-

This command starts transmitting data and write them into SRAM. In KW mode, this command writes "OLD" data to SRAM.
In KWR mode, this command writes "B/W" data to SRAM.
In Program mode, this command writes "OTP" data to SRAM for programming.

(9)DATA STOP (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Stopping data transmission	0	0	0	0	0	1	0	0	0	1	11H
	1	1	data_flag	-	-	-	-	-	-	-	*10H*

Check the completeness of data. If data is complete, start to refresh display.

Data_flag : Data flag of receiving user data.

0: Driver didn't receive all the data.

1: Driver has already received all the one-frame data (DTM1 and DTM2).

After "Data Start" (R10h) or "Data Stop" (R11h) commands and when data_flag=1, the refreshing of panel starts and BUSY_N signal will become "0".

(10)DISPLAY REFRESH (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Refreshing the display	0	0	0	0	0	1	0	0	1	0	12H

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT. After Display Refresh command, BUSY_N signal will become "0" and the refreshing of panel starts.

The waiting interval form BUSY_N falling to the first FLG command must be larger than 200uS.

(11)DATA START TRANSMISSION 2 (DTM2)(R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	1	1	13H
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	
	0	1	:	:	:	:	:	:	:	:	
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	

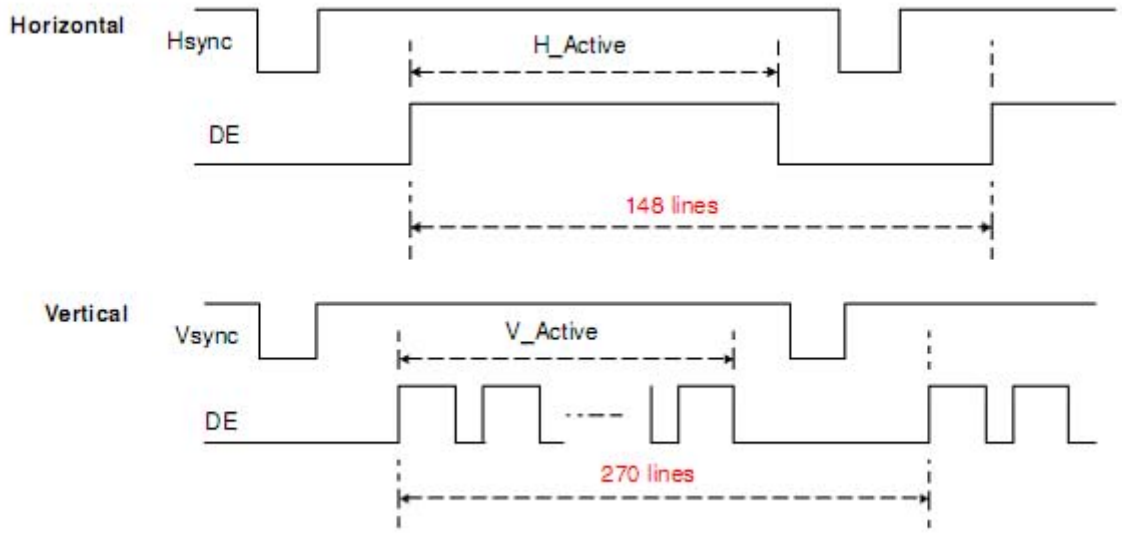
This command starts transmitting data and write them into SRAM.
In KW mode, this command writes "NEW" data to SRAM.
In KWR mode, this command writes "RED" data to SRAM.

(12) PLL CONTROL (PLL) (R30H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Controlling PLL	0	0	0	0	1	1	0	0	0	0	30H
	0	1	-	-	-	FRS[4:0]					09H

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:
FRS[4:0]: Frame rate setting

FRS	Frame rate	FRS	Frame rate
00000	5Hz	10000	85Hz
00001	10Hz	10001	90Hz
00010	15Hz	10010	95Hz
00011	20Hz	10011	100Hz
00100	25Hz	10100	105Hz
00101	30Hz	10101	110Hz
00110	35Hz	10110	115Hz
00111	40Hz	10111	120Hz
01000	45Hz	11000	130Hz
01001	**50Hz**	11001	140Hz
01010	55Hz	11010	150Hz
01011	60Hz	11011	160Hz
01100	65Hz	11100	170Hz
01101	70Hz	11101	180Hz
01110	75Hz	11110	190Hz
01111	80Hz	11111	200Hz



(13)VCOM AND DATA INTERVAL SETTING (CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Interval between VCOM and Data	0	0	0	1	0	1	0	0	0	0	50H
	0	1	VBD[1:0]		DDX[1:0]		CDI[3:0]				D7H

This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

VBD[1:0]: Border data selection
KWR mode (KW/R=0)

DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTR
	10	LUTW
	11	LUTK
1 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	Floating

KW mode (KW/R=1)

DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	Floating
1 (Default)	00	Floating
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	Floating

DDX[1:0]: Data polality.

Under KWR mode (KW/R=0):

DDX[1] is for RED data.

DDX[0] is for B/W data,

DDX[1:0]	Data {Red, B/W}	LUT
00	00	LUTW
	01	LUTK
	10	LUTR
	11	LUTR
01 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	LUTR

DDX[1:0]	Data {Red, B/W}	LUT
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTK
11	00	LUTR
	01	LUTR
	10	LUTK
	11	LUTW

Under KW mode (KW/R=1):

DDX[1]=0 is for KW mode with NEW/OLD,

DDX[1]=1 is for KW mode without NEW/OLD.

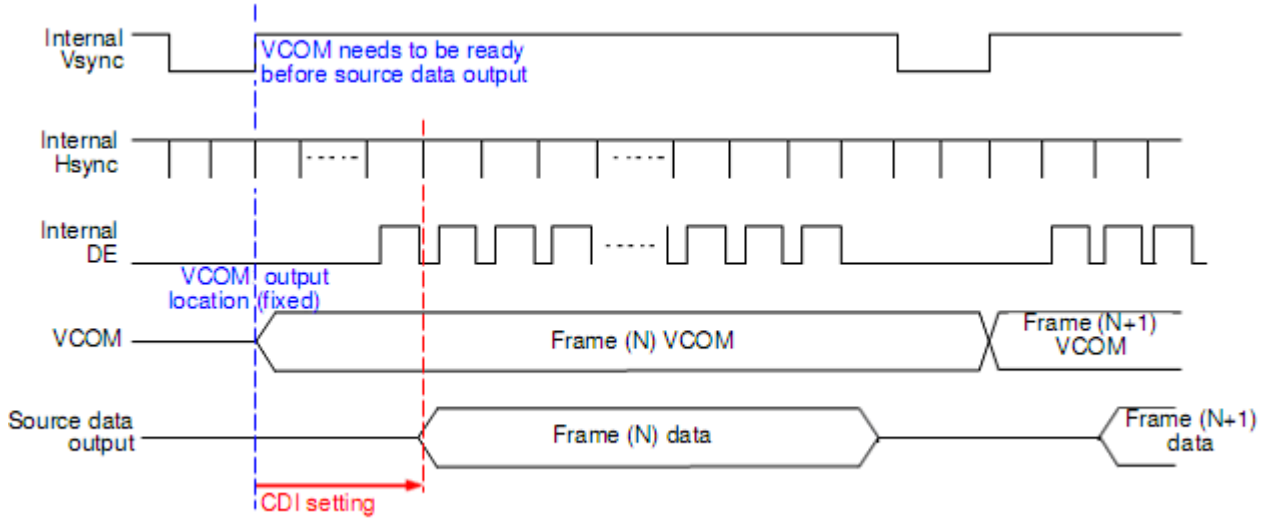
DDX[1:0]	Data {NEW, OLD}	LUT
00	00	LUTWW (0 → 0)
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	LUTKK (1 → 1)
01 (Default)	00	LUTKK (0 → 0)
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	LUTWW (1 → 1)

DDX[1:0]	Data {NEW}	LUT
10	0	LUTKW (1 → 0)
	1	LUTWK (0 → 1)
11	0	LUTWK (1 → 0)
	1	LUTKW (0 → 1)

CDI[3:0]: VCOM and data interval

CDI[3:0]	VCOM and Data Interval
0000 b	17 hsync
0001	16
0010	15
0011	14
0100	13
0101	12
0110	11

CDI[3:0]	VCOM and Data Interval
1000	9
1001	8
1010	7
1011	6
1100	5
1101	4
1110	3



(14)TCON SETTING (TCON) (R60H)

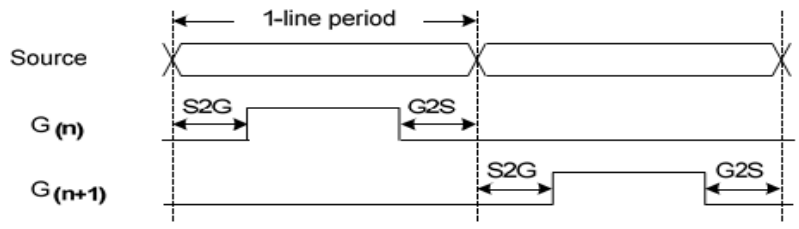
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Non-overlap Period	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**60H**
	0	1	S2G[3:0]				G2S[3:0]				**22H**

This command defines non-overlap period of Gate and Source.
S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period
0000 b	4
0001	8
0010	**12 (Default)**
0011	16
0100	20
0101	24
0110	28
0111	32

S2G[3:0] or G2S[3:0]	Period
1000 b	36
1001	40
1010	44
1011	48
1100	52
1101	56
1110	60
1111	64

Period Unit = 650 nS



(15) RESOLUTION SETTING (TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display Resolution	0	0	0	1	1	0	0	0	0	1	61H
	0	1	HRES[7:3]					0	0	0	00H
	0	1	VRES[7:0]								00H

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).
HRES[7:3]: Horizontal Display Resolution
VRES[7:0]: Vertical Display Resolution
Active channel calculation, assuming HST[7:0]=0, VST[7:0]=0:
Gate:First active gate= G0;
Last active gate = VRES[7:0] – 1
Source: First active source = S0;
Last active source= HRES[7:3]*8 - 1
Example: 128 (source) x 240 (gate), assuming HST[7:0]=0, VST[7:0]=0
Gate: First active gate = G0,
Last active gate= G239; (VRES[7:0]=240,240-1=239)
Source: First active source= S0,
Last active source= S127; (HRES[7:3]=16, 16*8 – 1 = 127)

(16) GATE/SOURCE START SETTING (GSST) (R65H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Start	0	0	0	1	1	0	0	1	0	1	65H
	0	1	HST[7:3]					0	0	0	00H
	0	1	VST[7:0]								00H

This command defines resolution start gate/source position.
HST[7:3]: Horizontal Display Start Position (Source)
VST[7:0]: Vertical Display Start Position (Gate)
Example : For 64(Source) x 204(Gate)
HST[7:3] = 4 (HST[7:0] = 4*8 = 32),
VST[7:0] = 32
Gate: First active gate = G32 (VST[7:0] = 32),
Last active gate = G235 (VST[7:0] = 32, VRES[7:0] =204 , 32+204-1=235)
Source: First active source = S32 (HST[7:0] = 32),
Last active source = S95 (HST[7:0] = 32, HRES[7:0] =64, 32+64-1=95)

(17)VCOM_DC SETTING (VDCS)(R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set VCOM_DC	0	0	1	0	0	0	0	0	1	0	82H
	0	1	-	VDCS[6:0]							00H

This command sets VCOM_DC value
VDCS[6:0]: VCOM_DC Setting

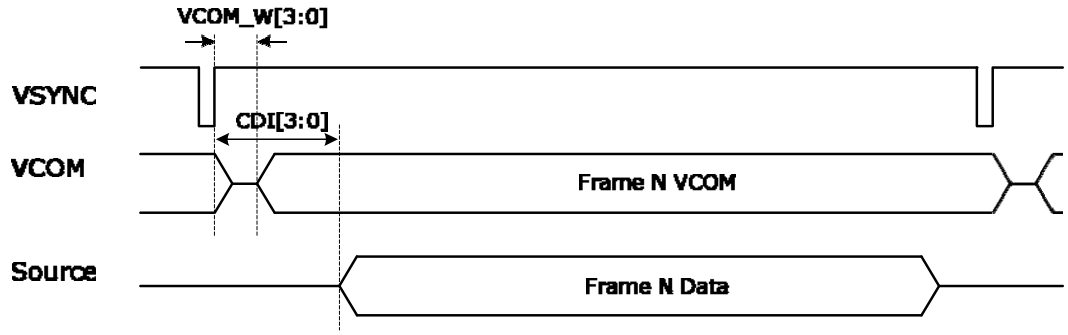
VDCS [6:0]	VCOM Voltage (V)	VDCS [6:0]	VCOM Voltage (V)	VDCS [6:0]	VCOM Voltage (V)
0000000b	-0.1	0101011b	-4.4	1010110b	-8.7
0000001b	-0.2	0101100b	-4.5	1010111b	-8.8
0000010b	-0.3	0101101b	-4.6	1011000b	-8.9
0000011b	-0.4	0101110b	-4.7	1011001b	-9
0000100b	-0.5	0101111b	-4.8	1011010b	-9.1
0000101b	-0.6	0110000b	-4.9	1011011b	-9.2
0000110b	-0.7	0110001b	-5	1011100b	-9.3
0000111b	-0.8	0110010b	-5.1	1011101b	-9.4
0001000b	-0.9	0110011b	-5.2	1011110b	-9.5
0001001b	-1	0110100b	-5.3	1011111b	-9.6
0001010b	-1.1	0110101b	-5.4	1100000b	-9.7
0001011b	-1.2	0110110b	-5.5	1100001b	-9.8
0001100b	-1.3	0110111b	-5.6	1100010b	-9.9
0001101b	-1.4	0111000b	-5.7	1100011b	-10
0001110b	-1.5	0111001b	-5.8	1100100b	-10.1
0001111b	-1.6	0111010b	-5.9	1100101b	-10.2
0010000b	-1.7	0111011b	-6	1100110b	-10.3
0010001b	-1.8	0111100b	-6.1	1100111b	-10.4
0010010b	-1.9	0111101b	-6.2	1101000b	-10.5
0010011b	-2	0111110b	-6.3	1101001b	-10.6
0010100b	-2.1	0111111b	-6.4	1101010b	-10.7
0010101b	-2.2	1000000b	-6.5	1101011b	-10.8
0010110b	-2.3	1000001b	-6.6	1101100b	-10.9
0010111b	-2.4	1000010b	-6.7	1101101b	-11
0011000b	-2.5	1000011b	-6.8	1101110b	-11.1
0011001b	-2.6	1000100b	-6.9	1101111b	-11.2
0011010b	-2.7	1000101b	-7	1110000b	-11.3
0011011b	-2.8	1000110b	-7.1	1110001b	-11.4
0011100b	-2.9	1000111b	-7.2	1110010b	-11.5
0011101b	-3	1001000b	-7.3	1110011b	-11.6
0011110b	-3.1	1001001b	-7.4	1110100b	-11.7
0011111b	-3.2	1001010b	-7.5	1110101b	-11.8
0100000b	-3.3	1001011b	-7.6	1110110b	-11.9
0100001b	-3.4	1001100b	-7.7	1110111b	-12
0100010b	-3.5	1001101b	-7.8	1111000b	-12.1
0100011b	-3.6	1001110b	-7.9	1111001b	-12.2
0100100b	-3.7	1001111b	-8	1111010b	-12.3
0100101b	-3.8	1010000b	-8.1	1111011b	-12.4
0100110b	-3.9	1010001b	-8.2	1111100b	-12.5
0100111b	-4	1010010b	-8.3	1111101b	-12.6
0101000b	-4.1	1010011b	-8.4	1111110b	-12.7
0101001b	-4.2	1010100b	-8.5		
0101010b	-4.3	1010101b	-8.6		

(18) POWER SAVING (PWS)(RE3H)

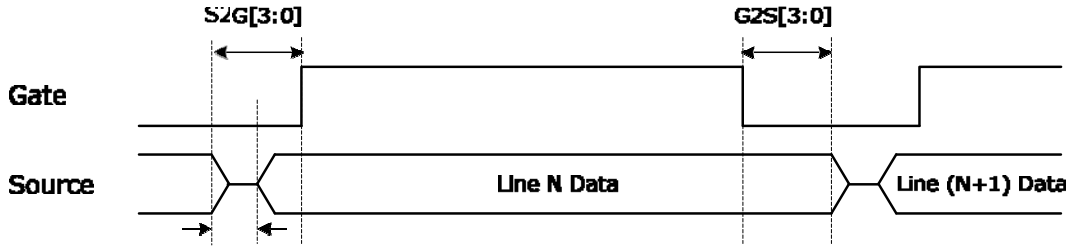
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Power Saving for VCOM & Source	0	0	1	1	1	0	0	0	1	1	E3H
	0	1	VCOM_W[3:0]				SD_W[3:0]				00H

This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W[3:0]: VCOM power saving width (unit = line period)



SD_W[3:0]: Source power saving width (unit = 650nS)



9. Reference Circuit

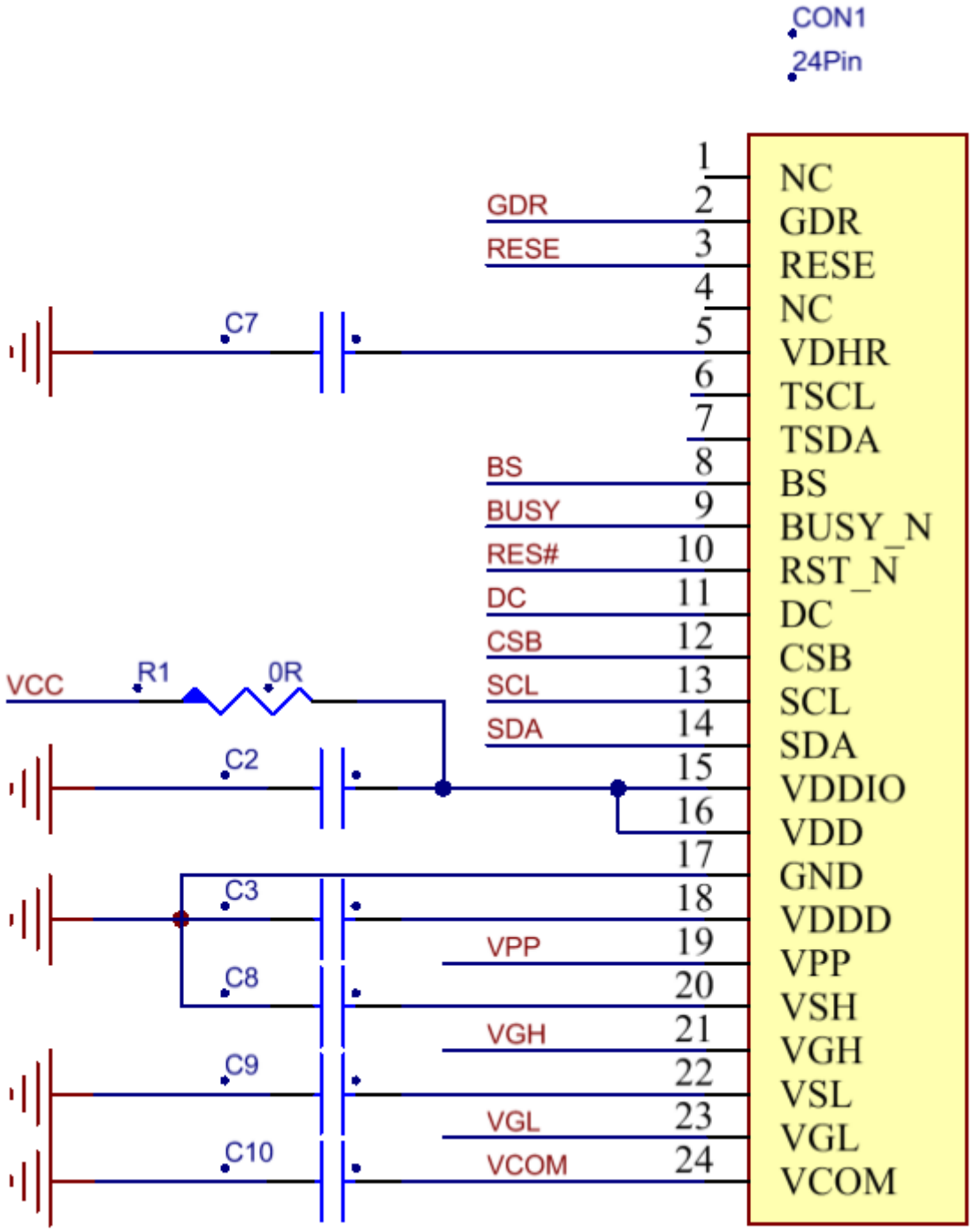


Figure. 9-1

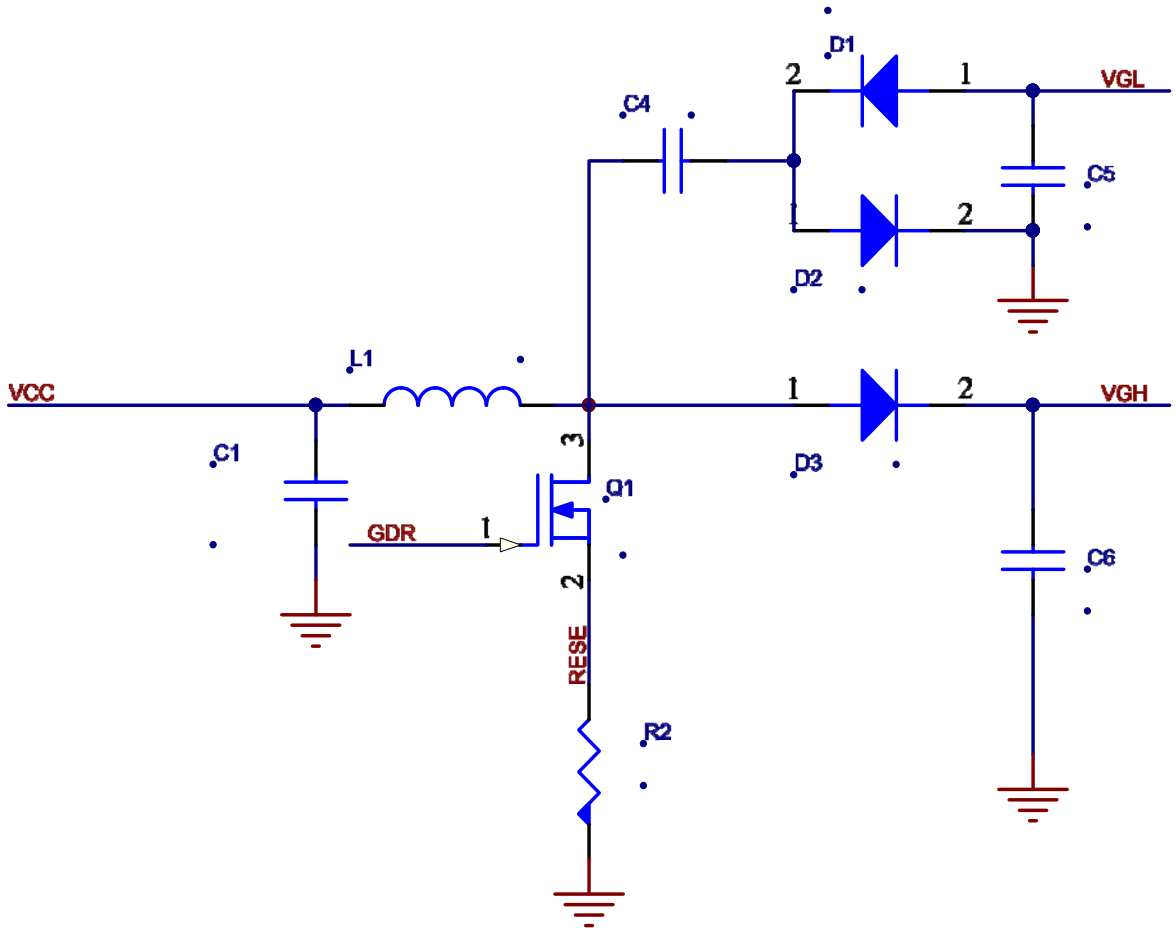


Figure. 9-2

Part Name	Value /reirement/Reference Part
C1—C3	1uF/0603;X5RR;Voltage Rating: 25V
C4	4.7uF/0603;X5R;Voltage Rating: 25V
C5—C10	1uF/0603;X5R;Voltage Rating: 25V
D1—D3	MBR0530 1) Reverse DC voltage≥30V 2) Forward current≥500mA 3)Forward voltage≤430mV
R2	0.47 Ω/0603：1% variation
Q1	NMOS:Si1308EDL 1） Drain-Source breakdown voltage ≥30V 2） Vgs（th）=0.9（Typ），1.3V（Max） 3） Rds on≤ 2.1Ω @ Vgs=2.5V
L1	10uH/NRH3010T100MN
CON24Pin	0.5mm ZIF Socket 24Pins,0.5mm pitch

10. ABSOLUTE MAXIMUM RATING

Table 10-1: Absolute Maximum Ratings of Panel

Symbol	Parameter	Rating	Unit	Humidity	Unit	Note
V_{DD}	Logic supply voltage	-0.3 to +6.0	V	-	-	Note10-1
T_{OPR}	Operation temperature range	0 to 50	℃	35 to70	%	
Tttg	Transportation temperature range	-25 to 60	℃	-	-	Note10-2
Tstg	Storage condition	0 to 40	℃	35 to70	%	Maximum storage time: 5 years

Note 10-1:VDD:Digital power , VDDIO:IO power, VDDA:Analog power ,Ta=25±2℃.

Note10-2: TSTG is the transportation condition ,the transport time is within 10 days for -25℃~0℃ or 50℃~60℃.

11. DC CHARACTERISTICS

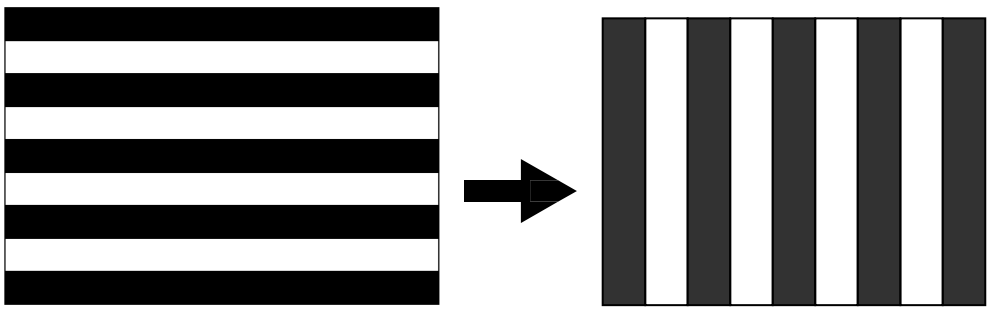
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
VDD	Supply voltage	-	2.5	3.3	3.6	V
VIH	High level input voltage	-	0.7VDDIO	-	-	V
VIL	Low level input voltage	-	0	-	0.2VDDIO	V
VOH	High level output voltage	IOH = 400uA	VDDIO-0.4	-	-	V
VOL	Low level output voltage	IOL = -400uA	0	-	0.4	V
Iupdate	Module operating current		-	3	-	mA
Isleep	Deep sleep mode	VDD=3.3V	-	-	3	uA

The following specifications apply for: VSS=0V, VDD=3.3V, TOPR=25±2℃.

- The Typical power consumption is measured using associated 25℃ waveform with following pattern transition: from horizontal scan pattern to vertical scan pattern. (Note 11-1)
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by XingTai.
- Vcom value will be OTP before in factory.

Note 11-1

The Typical power consumption



12. AC Characteristics

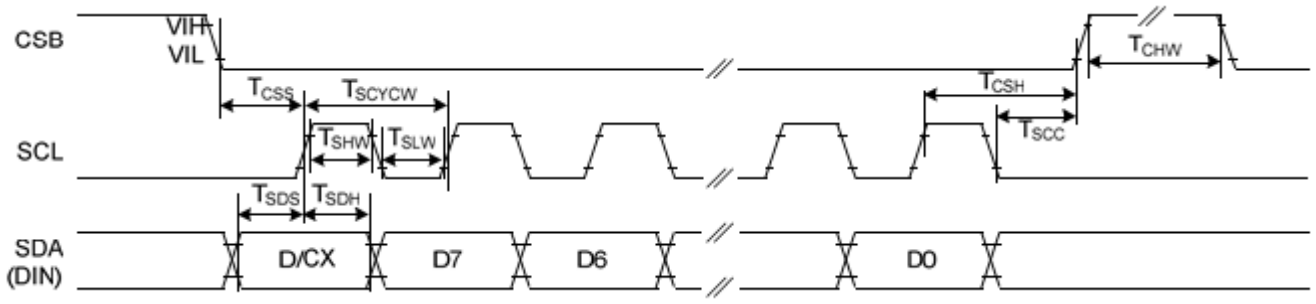


Figure. 12-1 3-wire serial interface Characteristics (Write mode)

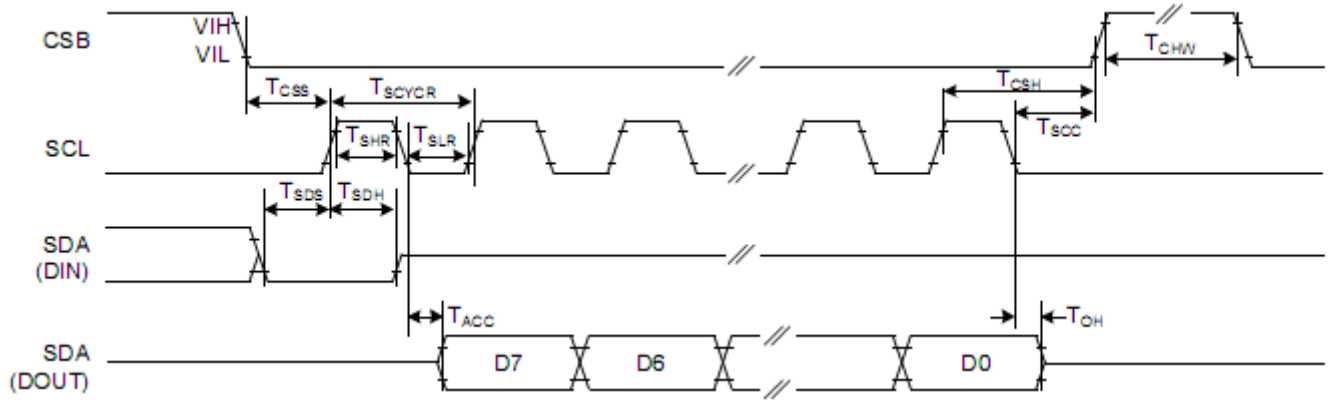


Figure. 12-2 3-wire serial interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60	-	-	ns
T_{CSH}		Chip select hold time	65	-	-	ns
T_{SCC}		Chip select setup time	20	-	-	ns
T_{CHW}		Chip select setup time	40	-	-	ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100	-	-	ns
T_{SHW}		SCL “H” pulse width (Write)	35	-	-	ns
T_{SLW}		SCL “L” pulse width (Write)	35	-	-	ns
T_{SCYCR}		Serial clock cycle (Read)	150	-	-	ns
T_{SHR}		SCL “H” pulse width (Read)	60	-	-	ns
T_{SLR}		SCL “L” pulse width (Read)	60	-	-	ns
T_{SDS}	SDA (DIN)	Data setup time	30	-	-	ns
T_{SDH}		Data hold time	30	-	-	ns
T_{ACC}	SDA (Dout)	Access time	-	-	150	ns
T_{OH}		Output disable time	15	-	-	ns

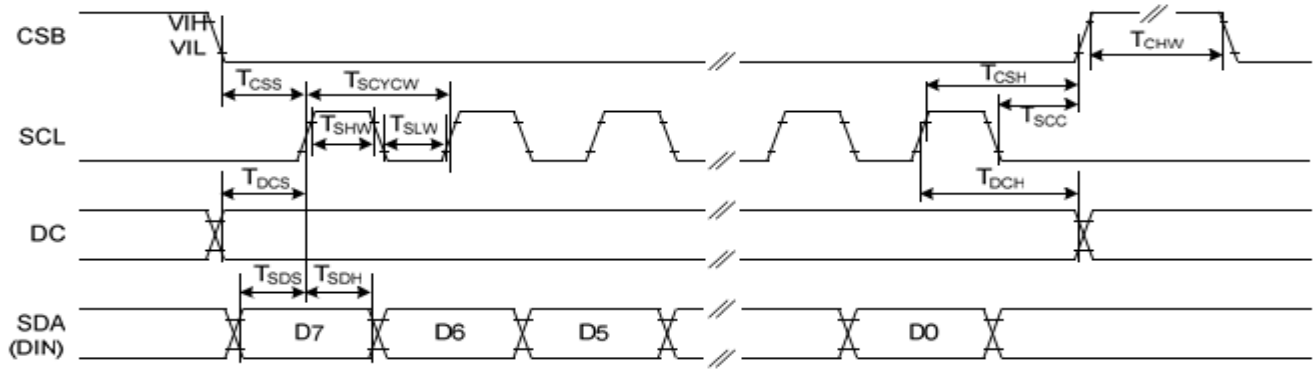


Figure. 12-3 4-wire serial interface Characteristics (Write mode)

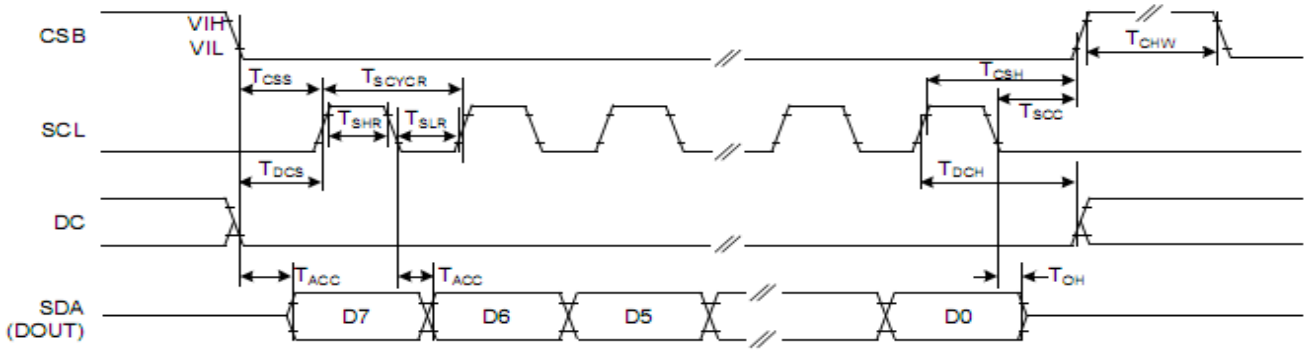
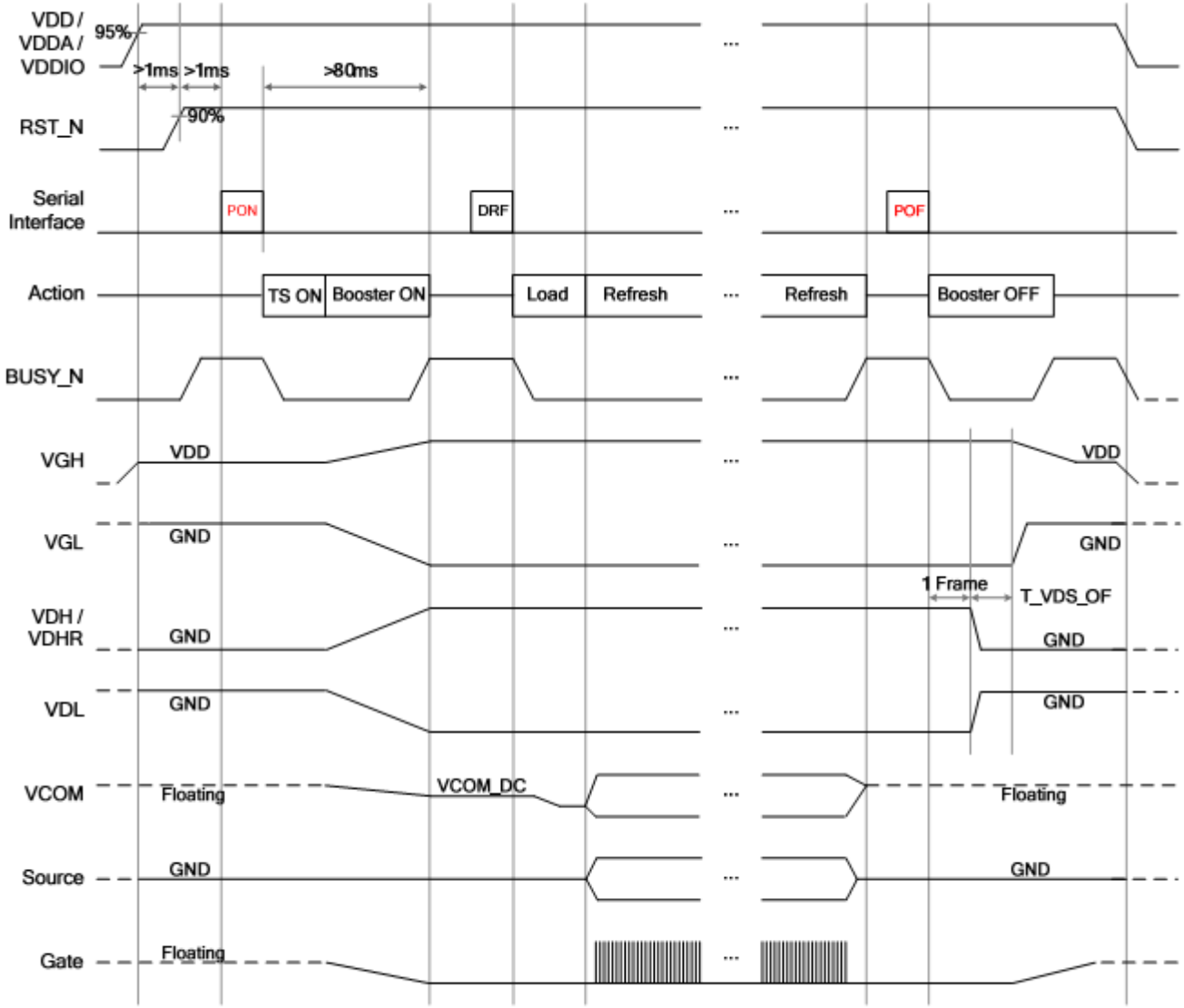


Figure. 12-4 4-wire serial interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60	-	-	ns
T_{CSH}		Chip select hold time	65	-	-	ns
T_{SCC}		Chip select setup time	20	-	-	ns
T_{CHW}		Chip select setup time	40	-	-	ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100	-	-	ns
T_{SHW}		SCL “H” pulse width (Write)	35	-	-	ns
T_{SLW}		SCL “L” pulse width (Write)	35	-	-	ns
T_{SCYCR}		Serial clock cycle (Read)	150	-	-	ns
T_{SHR}		SCL “H” pulse width (Read)	60	-	-	ns
T_{SLR}		SCL “L” pulse width (Read)	60	-	-	ns
T_{DCS}	DC	Data setup time	30	-		ns
T_{DCH}		Data hold time	30	-	-	ns
T_{SDS}	SDA (DIN)	Data setup time	30	-	-	ns
T_{SDH}		Data hold time	30	-	-	ns
T_{ACC}	SDA (Dout)	Access time	-	-	150	ns
T_{OH}		Output disable time	15	-	-	ns

13. Power ON /OFF Sequence

1. Temperature sensor will be activated automatically for one-time sensing before enabling booster.
2. After refreshing display, VCOM will be set to floating automatically.
3. In OTP mode (REG=0), the LUT in OTP will be copied to register automatically after the DSP/DRF command.
4. After RST_N rising, the waiting time for internal initial processing, greater than 1mS, is necessary. Any commands transmitted to chip during this time will be ignored.



14. Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25℃	-	30	mAs	-
Deep sleep mode	-	25℃	-	3	uA	-

MAs=update average current ×update time

15. Typical Operating Sequence

15.1 Normal Operation Flow

Sequence	Action by	Command	Action Description	Remark
1	User	-	Power on(VCI supply)	-
2	User	-	HW reset	-
	IC	-	After HW reset ,the driver IC will have registers load with POR value. Ready for command input. Vcom register loaded with OTP value.	-
3	-	-	Send initial code to driver including setting of.	-
	User	C00	Panel configuration: Resolution setting, LUT selection, BW/BWR mode.	-
	User	C50	Setting Vcom and Data interval.	-
4	-	-	Data operations.	-
	User	C61	Display resolution start and end active gate/source.	-
	User	C10 and C13	Write display data to RAM.	-
5	User	C04	Output gate/source voltage.	-
	User	C12	Boosters and regulators turn on. Load temperature register with sensor reading. Load LUT(register or OTP)	-
	User	C02	Turn off gate/source voltage.	-
6	User	-	Power off.	-

16. Optical characteristics

16.1 Optical Measurement Conditions

Item	Symbol	Value	Unit	Note
Ambient Temperature	Ta	25±2	℃	-
Ambient Humidity	Ha	50±10	%RH	-
Supply Voltage	VDD, VDDIO	3.3	V	-

Note 16-1： Image is updated with above condition

16.2 Optical Measurement

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 16-2
Gn	2Grey Level	-	-	KS+(WS-KS)×n(m-1)	-	L*	-
CR	Contrast Ratio	-	-	10	-	-	-
KS	Black State L* value	-	-	18	-	-	Note 16-2
	Black State a* value	-	-	0.2	-	-	Note 16-2
WS	White State L* value	-	-	67	-	-	Note 16-2
Panel	Image Update	Storage and transportation	-	Update the white screen	-	-	-
	Update Time	Operation	-	Suggest Updated once a day	-	-	-

WS : White state, KS : Dark state

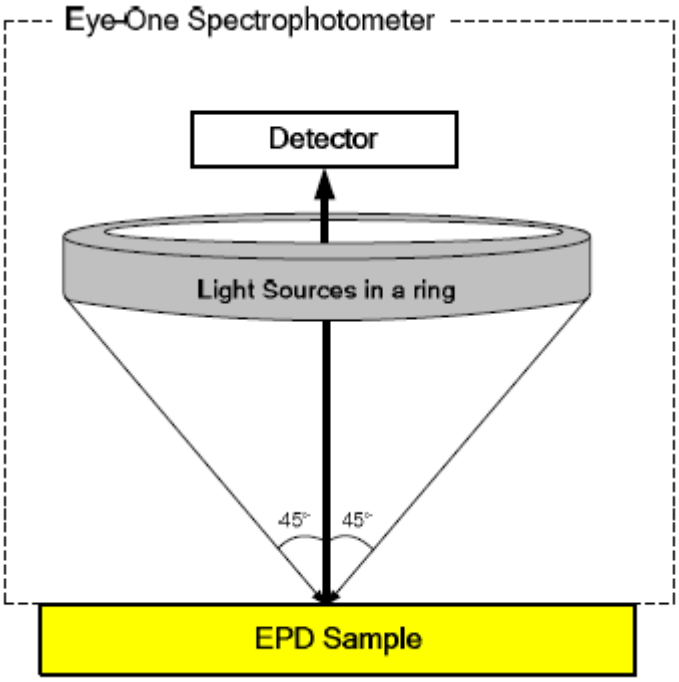
Note 16-2 : Luminance meter : i - One Pro Spectrophotometer ;

Note 16-3: We guarantee display quality from 0℃～30℃ generally, If operation ambient temperature from 0～50℃, will Offer special waveform by Xingtai.

16.3 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd):

CR = Rl/Rd



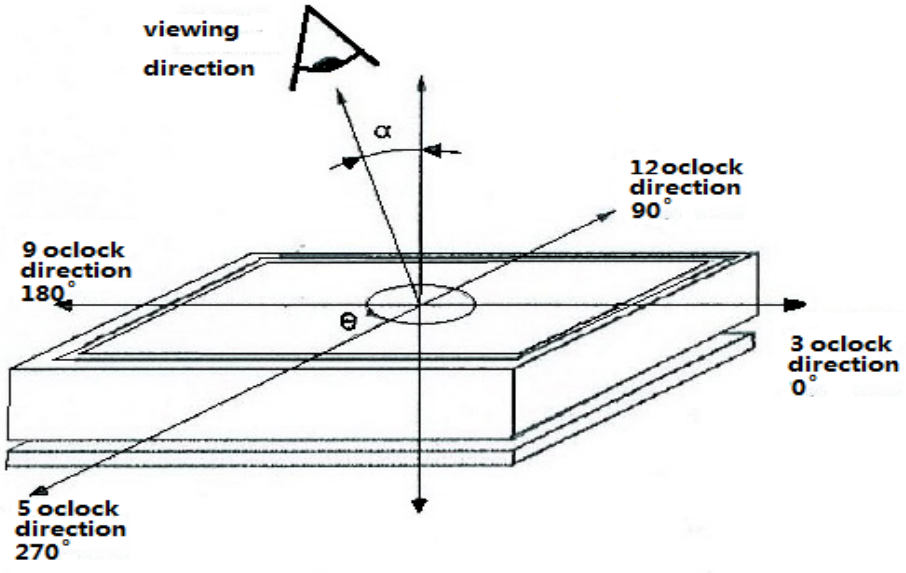
16.4 Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factor white board x (L center / L white board)

L center is the luminance measured at center in a white area (R=G =B=1). L white board is the luminance of a standard white.

board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



17. HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display module should be kept flat or fixed to a rigid, curved support with limited bending along the long axis. It should not be used for continual flexing and bending. Handle with care. Should the display break do not touch any material that leaks out. In case of contact with the leaked material then wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.
Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status	
Product specification	The data sheet contains final product specifications.

Limiting values
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.
Application information
Where application information is given, it is advisory and dose not form part of the specification.

Product Environmental certification
ROHS
REMARK
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

18. Reliability test

18.1 Reliability Test Items

	TEST	CONDITION	REMARK
1	High-Temperature Operation	T=40℃, RH=35%RH, For 240Hr	
2	Low-Temperature Operation	T = 0℃ for 240 hrs	
3	High-Temperature Storage	T=60℃ RH=35%RH For 240Hr	Test in white pattern
4	Low-Temperature Storage	T = -25℃ for 240 hrs	Test in white pattern
5	High Temperature, High-Humidity Operation	T=40℃,RH=90%RH, For 168Hr	
6	High Temperature, High-Humidity Storage	T=60℃,RH=80%RH,For 240Hr Test in white pattern	Test in white pattern
7	Temperature Cycle	-25℃(30min)~70℃(30min),100 Cycle	Test in white pattern
8	Package Vibration	1.04G,Frequency : 20~200Hz Direction : X,Y,Z Duration: 30 minutes in each direction	Full packed for shipment
9	Package Drop Impact	Drop from height of 100 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment
10	UV exposure Resistance	765 W/㎡ for 168hrs,40℃	
11	Electrostatic discharge	Machine model: +/-250V,0Ω,200pF	

Actual EMC level to be measured on customer application.

Note1：Stay white pattern for storage and non-operation test.

Note2：Operation is black/white pattern , hold time is 150S.

Note3：The function, appearance should meet the requirements of the test before and after the test.

Note4：Keep testing after 2 hours placing at 20℃-25℃

18.2 Product life time

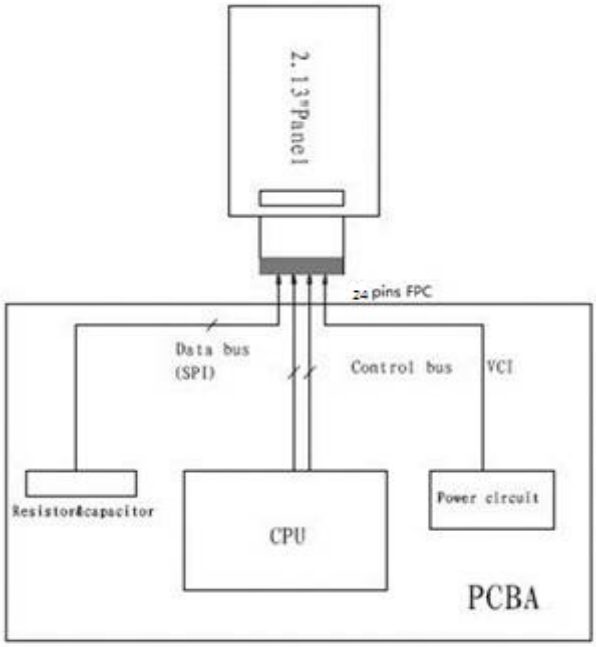
The EPD Module is designed for a 5-year life-time with 25 ℃/50%RH operation assumption. Reliability estimation testing with accelerated life-time theory would be demonstrated to provide confidence of EPD lifetime.

18.3 Product warranty

Warranty conditions have to be negotiated between Xingtai and individual customers.

Xingtai provides 12+1(one month delivery time) months warranty for all products which are purchased from Xingtai.

19. Block Diagram



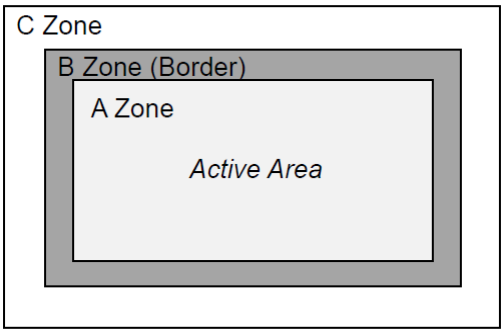
20. Shipment inspection specification

20.1 Zone Definition

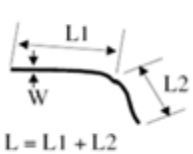
A Zone: Active Area

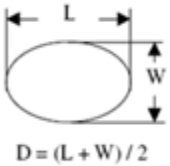
B Zone: Border Area

C Zone: From B Zone edge to panel edge

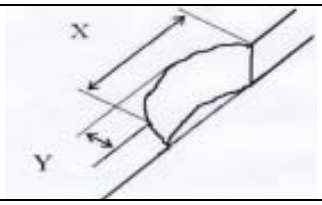
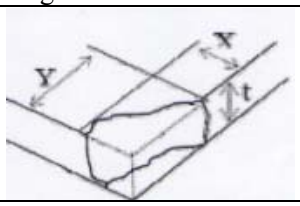


20.2 Line/Spot defect size





20.3 Point and line standard

Shipment Inspection Standard						
Equipment：Electrical test fixture, Point gauge						
Outline dimension	29.2(H)×59.2 (V) ×0.96(D)	Unit：㎜	Part-A	Active area	Part-B	Border area
Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle
	19℃～25℃	55%±10%RH	1200～1500Lux	300㎜	35Sec	
Defect type	Inspection method	Standard		Part-A		Part-B
Spot	Electric Display	D≤0.25㎜		Ignore		Ignore
		0.25㎜<D≤0.4㎜		N≤4		Ignore
		D>0.4㎜		Not Allow		Ignore
Display unwork	Electric Display	Not Allow		Not Allow		Ignore
Display error	Electric Display	Not Allow		Not Allow		Ignore
Scratch or line defect(include dirt)	Visual/Film card	L≤2㎜,W≤0.2㎜		Ignore		Ignore
		2.0mm<L≤5.0mm,0.2<W≤0.3mm,		N≤2		Ignore
		L>5㎜,W>0.3㎜		Not Allow		Ignore
PS Bubble	Visual/Film card	D≤0.2mm		Ignore		Ignore
		0.2mm≤D≤0.35mm		N≤4		Ignore
		D>0.35 mm		Not Allow		Ignore
Corner /Edge chipping	Visual/Film card	X≤6mm,Y≤0.4mm, Do not affect the electrode circuit (Edge chipping) X≤1mm,Y≤1mm, Do not affect the electrode circuit((Corner chipping) Ignore  				
Remark	1.Cannot be defect & failure cause by appearance defect;					
	2.Cannot be larger size cause by appearance defect;					
	L=long W=wide D=point size N=Defects NO					

21.Barcode

21.1 label appearance

ABBBBBBBCC
DDDEEEFGGG

21.2 QR scanned information（Total 28 code number+ 2 blank spaces）

A BBBBBBB CC □ DDD EEE F GGG □ H III JJ KK
① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑪

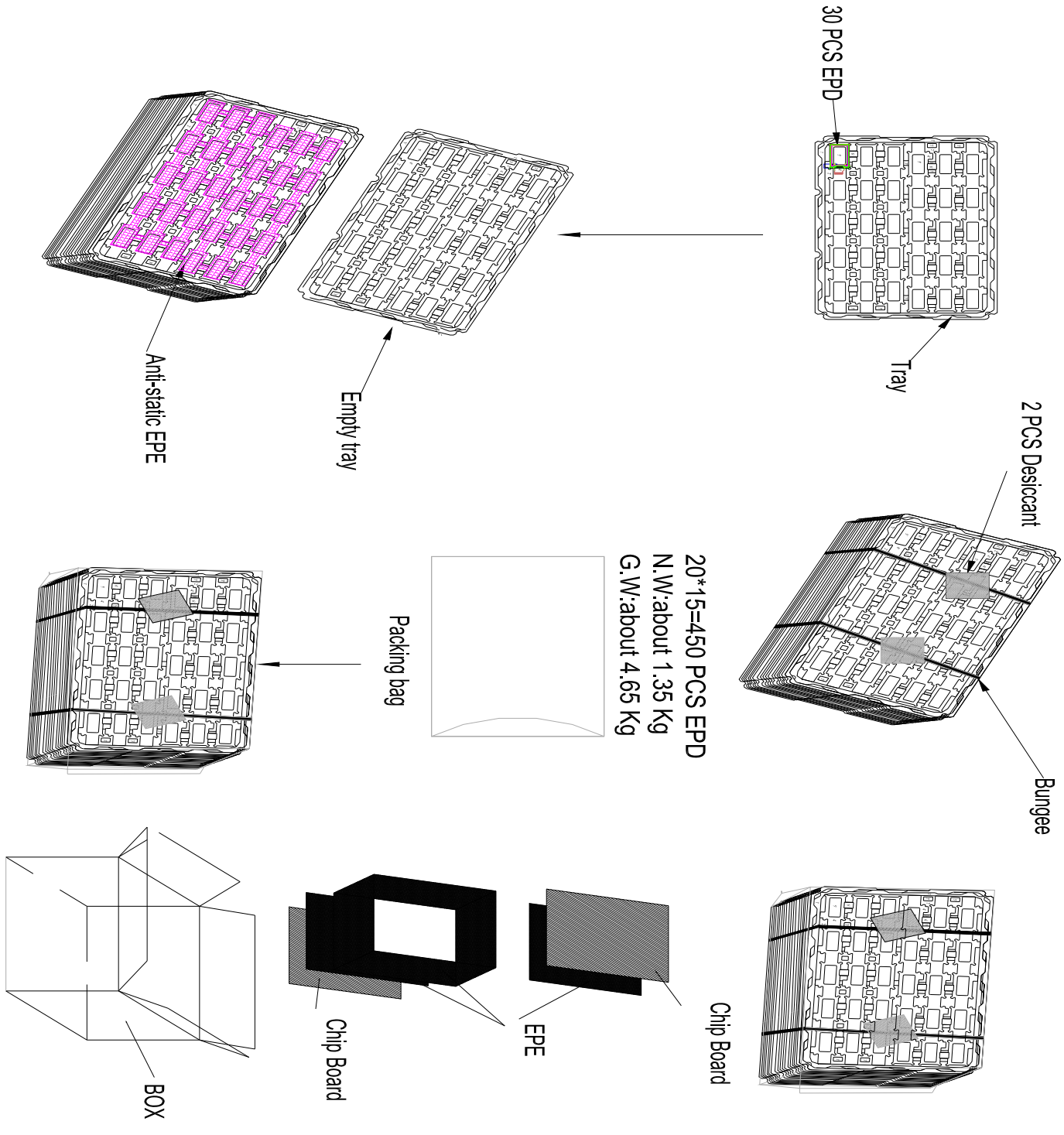
① A——The factory code
② BBBBBBB——Module name of EPD
③ CC——Production line
④ DDD——Date of production
⑤ EEE——Production lot
⑥ F——Separator
⑦ GGG——FPL Lot
⑧ H——Product status
⑨ III——TFT、PS、EC.
⑩ JJ——IC
⑪ KK——Serial NO.
□ blank spaces

22. Packing

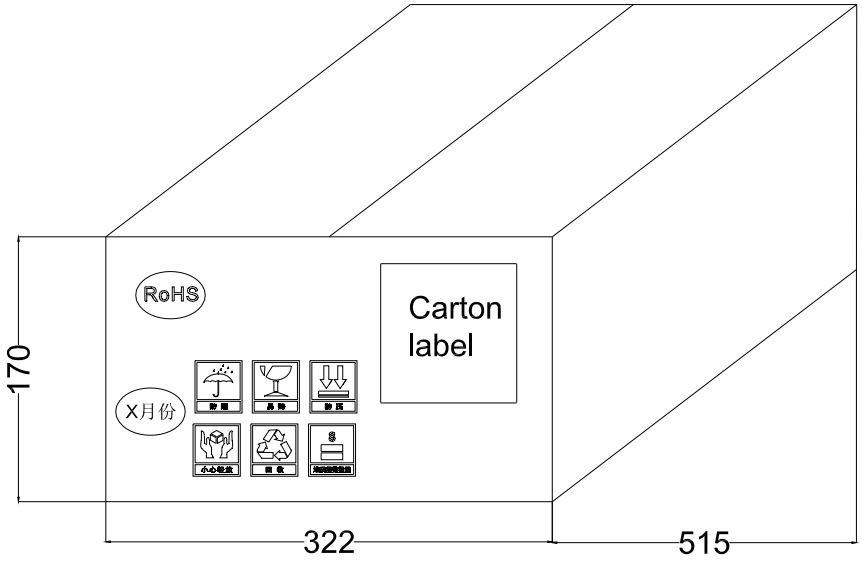
22.1 Packaging steps

Full carton: 15 pcs tray with products and 1 pcs empty tray.

Last carton: less 15pcs tray with products and 1 pcs empty tray. The packager will add the right amount of EPE to box so that the added EPE's height approximately close to the EPE height around the inside of the box.



22.2 Carton label position



22.3 Pallet

When the carton quantity is more than 15boxes,it is necessary to use pallet packaging for delivery.
The pallet packing method is: 5 boxes for each layer, up to 5 layers.
When the top carton quantity is less than 5 boxes, it needs to be filled with empty box,and the empty boxes must be labeled with "empty box"