Specification For HINK 2.66''EPD

Model NO.: HINK-E0266A85

Product VER:A0

Customer Approval

Customer	
Approval By	
Date Of Approval	

It will be agreed by the receiver,if not sign back the Specification within 15days.

Prepared By	Checked By	Approval By
Daisy Zhu	Yufeng Zhou	Ziping Hu

Version	Content	Date	Producer
A0	New release	2021/12/15	Daisy Zhu

CONTENTS

1. General Description

HINK-E0266A85 is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design. The 2.66" active area contains 152×296 pixels, and has 1-bit B/W/R full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

2.Features

- 152×296 pixels display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C signal master interface to read external temperature sensor I2C / built-in temperature sensor

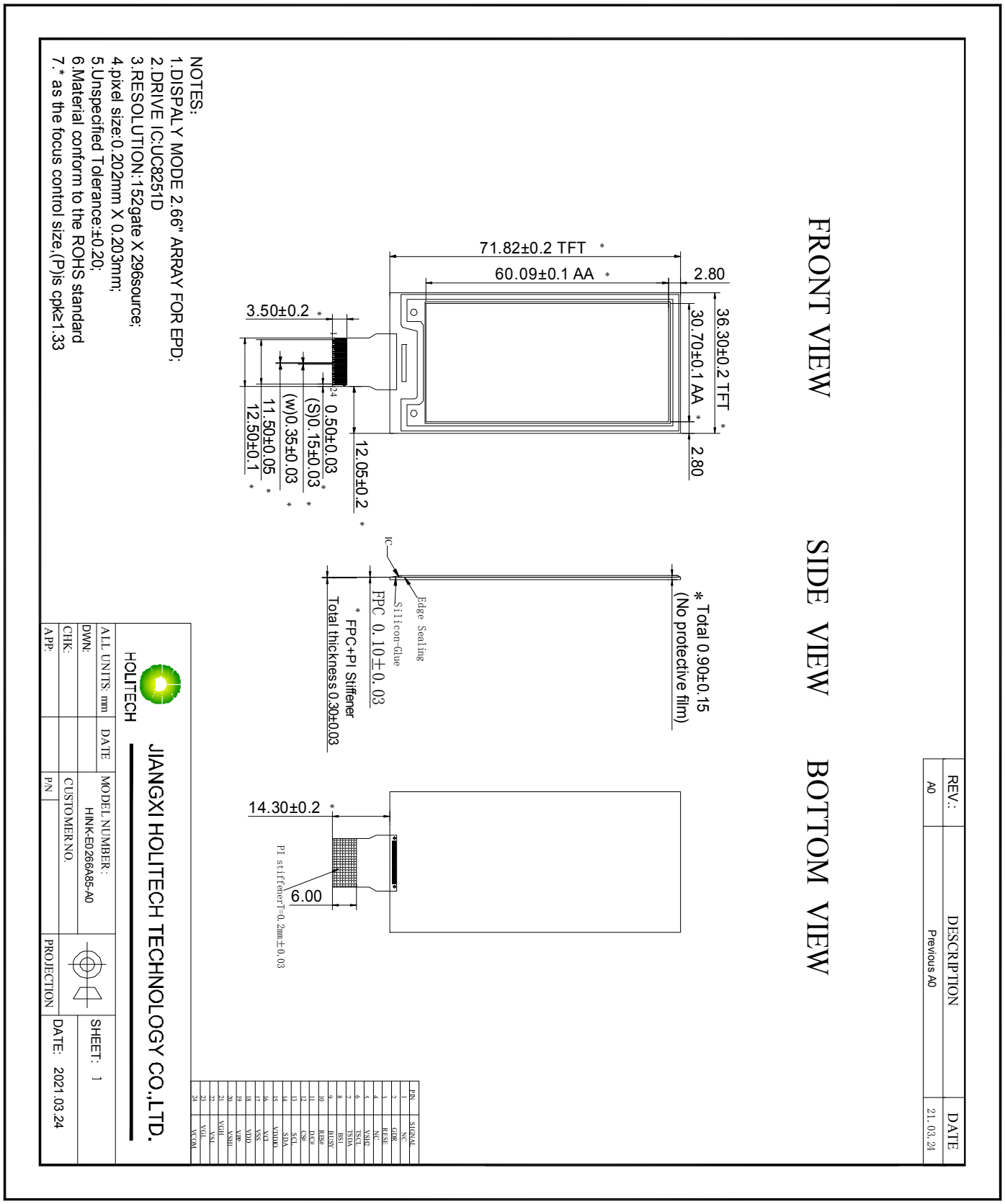
3. Application

Electronic Shelf Label System

4. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.66	Inch	
Display Resolution	152(H)×296(V)	Pixel	Dpi:125
Active Area	30.70(H)×60.09(V)	mm	
Pixel Pitch	0.202×0.203	mm	
Pixel Configuration	Rectangle		
Outline Dimension	36.3(H)×71.82(V) ×0.9(D)	mm	**Without masking film**
Weight	5±0.5	g	

5. Mechanical Drawing of EPD module



6. Input/Output Terminals

Pin #	Single	Description	Remark
1	NC	No connection and do not connect with other NC pins	Keep Open
2	GDR	N-Channel MOSFET Gate Drive Control	
3	RESE	Current Sense Input for the Control Loop	
4	NC	No connection and do not connect with other NC pins	Keep Open
5	VDHR	Positive Source driving voltage	
6	TSCL	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I2C Interface to digital temperature sensor Date pin	
8	BS	Bus selection pin	Note 6-5
9	BUSY_N	Busy state output pin	Note 6-4
10	RST_N	Reset	Note 6-3
11	DC	Data /Command control pin	Note 6-2
12	CSB	Chip Select input pin	Note 6-1
13	SCL	Serial communication clock input.	
14	SDA	Serial communication data input/output	
15	VDDIO	IO power	
16	VDD	Digital power	
17	GND	Ground	
18	VDDD	Digital power output (1.8V)	
19	VPP	OTP program power (7.75V)	
20	VDH	Positive source driver Voltage	
21	VGH	Positive Gate driving voltage	
22	VDL	Negative Source driving voltage	
23	VGL	Negative Gate voltage.	
24	VCOM	VCOM driving voltage	

Note 6-1: This pin (CSB) is the chip select input connecting to the MCU. The chip is enabled for MCU communication: only when CSB is pulled LOW.

Note 6-2: This pin (DC) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Note 6-3: This pin (RST_N) is reset signal input. When RST_N become low, driver will reset. All register will reset to
default value. Driver all function will disable.

Note 6-4: This pin (BUSY_N) is Busy state output pin.
L: Driver is Busy.
H: Host side can send command/data to driver.

Note 6-5: This pin (BS) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected.

7.COMMAND DESCRIPTION

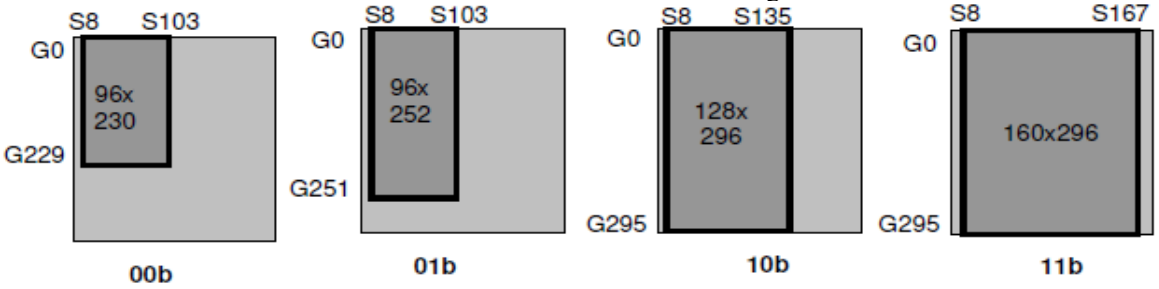
W/R: 0: Write Cycle / 1: Read Cycle C/D: 0: Command / 1: Data D7-D0: –: Don't Care

1)Panel Setting (PSR) (R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting the panel	0	0	0	0	0	0	0	0	0	0	00H
	0	1	RES1	RES0	REG	KW/R	UD	SHL	SHD_N	RST_N	0FH
	0	1	0	0	0	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	0DH

RES[1:0]: Display Resolution setting (source x gate)

00b: 96x230 (Default) Active source channels: S8 ~ S103. Active gate channels: G0 ~ G229.
01b: 96x252 Active source channels: S8 ~ S103. Active gate channels: G0 ~ G251.
10b: 128x296 Active source channels: S8 ~ S135. Active gate channels: G0 ~ G295.
11b: 160x296 Active source channels: S8 ~ S167. Active gate channels: G0 ~ G295.



(1) Minimum active GD is always G0 regardless of <UD>(R00H).
(2) Minimum active SD is always S0 regardless of <SHL>(R00H).

REG: LUT selection
0: LUT from OTP. (Default)
1: LUT from register.

KW/R: Black / White / Red
0: Pixel with Black/White/Red. (Default)
1: Pixel with Black/White. KW mode

UD: Gate Scan Direction
0: Scan down. First line to Last line: Gn-1 →Gn-2→Gn-3 →…→G0
1: Scan up. (Default) First line to Last line: G0 →G1 →G2 →… … . →Gn-1

SHL: Source Shift Direction
0: Shift left. First data to Last data: Sn-1 →Sn-2→Sn-3→…→S0
1: Shift right. (Default) First data to Last data: S0 →S1 →S2 →… … . →Sn-1

SHD_N: Booster Switch
0: Booster OFF
1: Booster ON (Default)
When SHD_N becomes LOW, charge pump will be turned OFF, register and SRAM data will be kept until VDD OFF, And Source/Gate/Border/ VCOM will be released to floating.

RST_N: Soft Reset
0: Reset. Booster OFF, Register data are set to their default values, all drivers will be reset, and all functions will be disabled. Source/Gate/Border/VCOM will be released to floating. After soft reset is transmitted, the internal operation needs at least 50uS to execute. During this period of time, the BUSY_N pin keeps low and any command will be ignored.
1: No effect (Default).

VCMZ: VCOM function
0: No effect (Default).
1: VCOM is always floating

TS_AUTO: Temperature sensor will be activated automatically one time.
0: No effect
1: Before enabling booster, Temperature Sensor will be activated automatically one time. (Default)

TIEG: VGL state function

0: No effect
1 : After power off booster, VGL will be tied to GND. (Default)

NORG: VCOM state during refreshing display
0: No effect (Default)
1: Expect refreshing display, VCOM is tied to GND.

VC_LUTZ: VCOM state during refreshing display
0: No effect
1: After refreshing display, the output of VCOM is set to floating automatically. (Default)
Note: Priority of Vcom setting: VCMZ > EOPT > NORG > VC_LUTZ

2)Power Setting (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Selecting Internal/External Power	0	0	0	0	0	0	0	0	0	1	01H
	0	1	-	-	-	-	-	-	VS_EN	VG_EN	03H
	0	1	-	-	-	-	VGHL_LV[3:0]				00H
	0	1	-	-	VSH[5:0]						3FH
	0	1	-	-	VSL[5:0]						3FH
	0	1	-	-	VDHR[5:0]						0DH

VS_EN: Source power selection
0 : External source power from VSH/VSL/VDHR pins
1 : Internal DC/DC function for generating VSH/VSL/VDHR. (Default)

VDG_EN: Gate power selection
0 : External gate power from VGH/VGL pins
1 : Internal DC/DC function for generating VGH/VGL. (Default)

VGHL_LV[3:0]: VGH / VGL Voltage Level selection.

VGHL_LV	VGHL Voltage Level
0000 (Default)	VGH=20V, VGL= -20V
0001	VGH=19V, VGL= -19V
0010	VGH=18V, VGL= -18V
0011	VGH=17V, VGL= -17V
0100	VGH=16V, VGL= -16V
0101	VGH=15V, VGL= -15V
0110	VGH=14V, VGL= -14V
0111	VGH=13V, VGL= -13V
1000	VGH=12V, VGL= -12V
1001	VGH=11V, VGL= -11V
1010	VGH=10V, VGL= -10V

VSH[5:0]: Internal VSH power selection for B/W pixel.(Default value: 11 1111b)

VSH	Voltage	VSH	Voltage	VSH	Voltage	VSH	Voltage
00 0000	2.4 V	01 0000	5.6 V	10 0000	8.8 V	11 0000	12.0 V
00 0001	2.6 V	01 0001	5.8 V	10 0001	9.0 V	11 0001	12.2 V
00 0010	2.8 V	01 0010	6.0 V	10 0010	9.2 V	11 0010	12.4 V
00 0011	3.0 V	01 0011	6.2 V	10 0011	9.4 V	11 0011	12.6 V
00 0100	3.2 V	01 0100	6.4 V	10 0100	9.6 V	11 0100	12.8 V
00 0101	3.4 V	01 0101	6.6 V	10 0101	9.8 V	11 0101	13.0 V
00 0110	3.6 V	01 0110	6.8 V	10 0110	10.0V	11 0110	13.2 V
00 0111	3.8 V	01 0111	7.0 V	10 0111	10.2 V	11 0111	13.4 V
00 1000	4.0 V	01 1000	7.2 V	10 1000	10.4 V	11 1000	13.6 V
00 1001	4.2 V	01 1001	7.4 V	10 1001	10.6 V	11 1001	13.8 V
00 1010	4.4 V	01 1010	7.6 V	10 1010	10.8 V	11 1010	14.0 V
00 1011	4.6 V	01 1011	7.8 V	10 1011	11.0 V	11 1011	14.2 V
00 1100	4.8 V	01 1100	8.0 V	10 1100	11.2 V	11 1100	14.4 V
00 1101	5.0 V	01 1101	8.2V	10 1101	11.4 V	11 1101	14.6 V
00 1110	5.2 V	01 1110	8.4 V	10 1110	11.6 V	11 1110	14.8 V
00 1111	5.4 V	01 1111	8.6 V	10 1111	11.8 V	**11 1111**	**15.0 V**

VSL[5:0]: Internal VSL power selection for B/W pixel. (Default value: 11 1111b)

VSL	Voltage	VSL	Voltage	VSL	Voltage	VSL	Voltage
00 0000	-2.4 V	01 0000	-5.6 V	10 0000	-8.8 V	11 0000	-12.0 V
00 0001	-2.6 V	01 0001	-5.8 V	10 0001	-9.0 V	11 0001	-12.2 V
00 0010	-2.8 V	01 0010	-6.0 V	10 0010	-9.2 V	11 0010	-12.4 V
00 0011	-3.0 V	01 0011	-6.2 V	10 0011	-9.4 V	11 0011	-12.6 V
00 0100	-3.2 V	01 0100	-6.4 V	10 0100	-9.6 V	11 0100	-12.8 V
00 0101	-3.4 V	01 0101	-6.6 V	10 0101	-9.8 V	11 0101	-13.0 V
00 0110	-3.6 V	01 0110	-6.8 V	10 0110	-10.0V	11 0110	-13.2 V
00 0111	-3.8 V	01 0111	-7.0 V	10 0111	-10.2 V	11 0111	-13.4 V
00 1000	-4.0 V	01 1000	-7.2 V	10 1000	-10.4 V	11 1000	-13.6 V
00 1001	-4.2 V	01 1001	-7.4 V	10 1001	-10.6 V	11 1001	-13.8 V
00 1010	-4.4 V	01 1010	-7.6 V	10 1010	-10.8 V	11 1010	-14.0 V
00 1011	-4.6 V	01 1011	-7.8 V	10 1011	-11.0 V	11 1011	-14.2 V
00 1100	-4.8 V	01 1100	-8.0 V	10 1100	-11.2 V	11 1100	-14.4 V
00 1101	-5.0 V	01 1101	-8.2V	10 1101	-11.4 V	11 1101	-14.6 V
00 1110	-5.2 V	01 1110	-8.4 V	10 1110	-11.6 V	11 1110	-14.8 V
00 1111	-5.4 V	01 1111	-8.6 V	10 1111	-11.8 V	**11 1111**	**-15.0 V**

VDHR[5:0]: Internal VDHR power selection for Red pixel. (Default value: 00 1101b)

VDHR	Voltage	VDHR	Voltage	VDHR	Voltage	VDHR	Voltage
00 0000	2.4 V	01 0000	5.6 V	10 0000	8.8 V	11 0000	12.0 V
00 0001	2.6 V	01 0001	5.8 V	10 0001	9.0 V	11 0001	12.2 V
00 0010	2.8 V	01 0010	6.0 V	10 0010	9.2 V	11 0010	12.4 V
00 0011	3.0 V	01 0011	6.2 V	10 0011	9.4 V	11 0011	12.6 V
00 0100	3.2 V	01 0100	6.4 V	10 0100	9.6 V	11 0100	12.8 V
00 0101	3.4 V	01 0101	6.6 V	10 0101	9.8 V	11 0101	13.0 V
00 0110	3.6 V	01 0110	6.8 V	10 0110	10.0V	11 0110	13.2 V
00 0111	3.8 V	01 0111	7.0 V	10 0111	10.2 V	11 0111	13.4 V
00 1000	4.0 V	01 1000	7.2 V	10 1000	10.4 V	11 1000	13.6 V
00 1001	4.2 V	01 1001	7.4 V	10 1001	10.6 V	11 1001	13.8 V
00 1010	4.4 V	01 1010	7.6 V	10 1010	10.8 V	11 1010	14.0 V
00 1011	4.6 V	01 1011	7.8 V	10 1011	11.0 V	11 1011	14.2 V
00 1100	4.8 V	01 1100	8.0 V	10 1100	11.2 V	11 1100	14.4 V
00 1101	**5.0 V**	01 1101	8.2V	10 1101	11.4 V	11 1101	14.6 V
00 1110	5.2 V	01 1110	8.4 V	10 1110	11.6 V	11 1110	14.8 V
00 1111	5.4 V	01 1111	8.6 V	10 1111	11.8 V	11 1111	15.0 V

3)Power OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning OFF the power	0	0	0	0	0	0	0	0	1	0	02H

After the Power OFF command, the driver will be powered OFF. The sequence refers to POWER MANAGEMENT section. This command will turn off booster, controller, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD turned OFF or Deep Sleep Mode.Source/Gate/Border/VCOM will be released to floating.

4)Power OFF Sequence Setting(PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1	03H
	0	1	-	-	T_VDS_OFF[1:0]		-	-	-	-	00H

T_VDS_OFF[1:0]: Power OFF Sequence of VDH and VDL.
00b: 1 frame (Default) 01b: 2 frames 10b: 3 frames 11b: 4 frame

5) Power ON (PON) (R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning ON the power	0	0	0	0	0	0	0	1	0	0	04H

After the Power ON command, the driver will be powered ON The sequence refers to POWER MANAGEMENT section. This command will turn on booster, controller, regulators, and temperature sensor will be activated for one-time sensing before enabling booster. When all voltages are ready, the BUSY_N signal will return to high.

6) Power ON MEASURE(PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
	0	0	0	0	0	0	0	1	0	1	05H

This command enables the internal bandgap, which will be cleared by the next POF.

7) Booster Soft Start (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	0	0	1	1	0	06H
	0	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0	17H
	0	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0	17H
	0	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0	17H

BTPHA[7:6]: Soft start period of phase A.
00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS
BTPHA[5:3]: Driving strength of phase A
000b: strength 1 001b: strength 2 010b: strength 3 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)
BTPHA[2:0]: Minimum OFF time setting of GDR in phase B
000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS 111b: 6.58uS
BTPHB[7:6]: Soft start period of phase B.
00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS
BTPHB[5:3]: Driving strength of phase B
000b: strength 1 001b: strength 2 010b: strength 3 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)
BTPHB[2:0]: Minimum OFF time setting of GDR in phase B
000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS 111b: 6.58uS
BTPHC[5:3]: Driving strength of phase C
000b: strength 1 001b: strength 2 010b: strength 3 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)
BTPHC[2:0]: Minimum OFF time setting of GDR in phase C
000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS 111b: 6.58uS

8) Deep sleep (DSLP) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Deep Sleep	0	0	0	0	0	0	0	1	1	1	07H
	0	1	1	0	1	0	0	1	0	1	A5H

After this command is transmitted, the chip will enter Deep Sleep Mode to save power. Deep Sleep Mode will return to Standby Mode by hardware reset. The only one parameter is a check code, the command will be executed if check code = 0xA5.

9) Data Start Transmission 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	0	0	10H
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	00H
	0	1	:	:	:	:	:	:	:	:	00H
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	00H

This command starts transmitting data and write them into SRAM.
In K/W mode, this command writes "OLD" data to SRAM.
In K/W/Red mode, this command writes "B/W" data to SRAM.
In Program mode, this command writes "OTP" data to SRAM for programming.

10) Data stop (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Stopping data transmission	0	0	0	0	0	1	0	0	0	1	11H
	1	1	data_flag	-	-	-	-	-	-	-	00H

Check the completeness of data. If data is complete, start to refresh display.
Data_flag: Data flag of receiving user data.
0: Driver didn't receive all the data.
1: Driver has already received all the one-frame data (DTM1 and DTM2).
After "Data Start" (R10h) or "Data Stop" (R11h) commands and when data_flag=1, the refreshing of panel starts and BUSY_N signal will become "0".

11) Display Refresh (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Refreshing the display	0	0	0	0	0	1	0	0	1	0	12H

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.
After Display Refresh command, BUSY_N signal will become "0" and the refreshing of panel starts.
The waiting interval form BUSY_N falling to the first FLG command must be > 200uS.

12) DATA START TRANSMISSION 2 (DTM2) (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	1	1	13H
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	00H
	0	1	:	:	:	:	:	:	:	:	00H
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	00H

This command starts transmitting data and write them into SRAM.
In K/W mode, this command writes "NEW" data to SRAM.
In K/W/Red mode, this command writes "RED" data to SRAM.

13) AUTO SEQUENCE (AUTO) (R17H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Auto Sequence	0	0	0	0	0	1	0	1	1	1	17H
	0	1	1	0	1	0	0	1	0	1	A5H

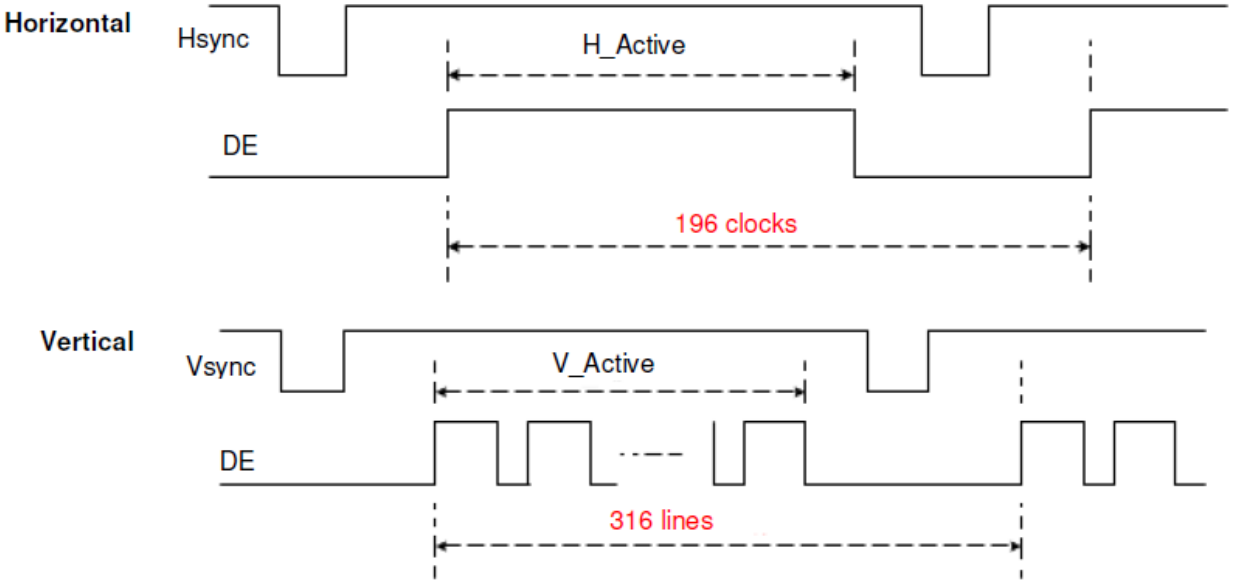
The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP.
AUTO (0x17) + Code(0xA5) = (PON → DRF → POF)
AUTO (0x17) + Code(0xA7) = (PON→ DRF→ POF→ DSLP)

14) PLL Control (PLL) (R30H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Controlling PLL	0	0	0	0	1	1	0	0	0	0	30H
	0	1	-	-	-	FRS[4:0]					09H

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:
FMR[4:0]: Frame rate setting

FRS	Frame rate	FRS	Frame rate
00000	5Hz	10000	85Hz
00001	10Hz	10001	90Hz
00010	15Hz	10010	95Hz
00011	20Hz	10011	100Hz
00100	25Hz	10100	105Hz
00101	30Hz	10101	110Hz
00110	35Hz	10110	115Hz
00111	40Hz	10111	120Hz
01000	45Hz	11000	130Hz
01001	**50Hz**	11001	140Hz
01010	55Hz	11010	150Hz
01011	60Hz	11011	160Hz
01100	65Hz	11100	170Hz
01101	70Hz	11101	180Hz
01110	75Hz	11110	190Hz
01111	80Hz	11111	200Hz



15) Temperature Sensor Calibration(TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Sensing Temperature	0	0	0	1	0	0	0	0	0	0	40H
	1	1	D10/TS7	D9/TS6	D8/TS5	D7/TS4	D6 / TS3	D5 / TS2	D4 / TS1	D3 / TS0	00H
	1	1	D2	D1	D0	-	-	-	-	-	00H

This command enables internal or external temperature sensor, and reads the result.
TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.
D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

TS[7:0]/D[10:3]	Temperature (°C)
1110_0111	-25
1110_1000	-24
1110_1001	-23
1110_1010	-22
1110_1011	-21
1110_1100	-20
1110_1101	-19
1110_1110	-18
1110_1111	-17
1111_0000	-16
1111_0001	-15
1111_0010	-14
1111_0011	-13
1111_0100	-12
1111_0101	-11
1111_0110	-10
1111_0111	-9
1111_1000	-8
1111_1001	-7
1111_1010	-6
1111_1011	-5
1111_1100	-4
1111_1101	-3
1111_1110	-2
1111_1111	-1

TS[7:0]/D[10:3]	Temperature(°C)
0000_0000	**0**
0000_0001	1
0000_0010	2
0000_0011	3
0000_0100	4
0000_0101	5
0000_0110	6
0000_0111	7
0000_1000	8
0000_1001	9
0000_1010	10
0000_1011	11
0000_1100	12
0000_1101	13
0000_1110	14
0000_1111	15
0001_0000	16
0001_0001	17
0001_0010	18
0001_0011	19
0001_0100	20
0001_0101	21
0001_0110	22
0001_0111	23
0001_1000	24

TS[7:0]/D[10:3]	Temperature(°C)
0001_1001	25
0001_1010	26
0001_1011	27
0001_1100	28
0001_1101	29
0001_1110	30
0001_1111	31
0010_0000	32
0010_0001	33
0010_0010	34
0010_0011	35
0010_0100	36
0010_0101	37
0010_0110	38
0010_0111	39
0010_1000	40
0010_1001	41
0010_1010	42
0010_1011	43
0010_1100	44
0010_1101	45
0010_1110	46
0010_1111	47
0011_0000	48
0011_0001	49

16) Temperature Sensor Enable(TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enable Temperature Sensor /Offset	0	0	0	1	0	0	0	0	0	1	41H
	0	1	TSE	-	-	-	TO[3:0]				00H

This command selects Internal or External temperature sensor.
TSE: Internal temperature sensor switch
0: Enable (default) 1: Disable; using external sensor.

TO[3:0]: Temperature offset.

TO[3:0]	Calculation
0000 b	+0 (Default)
0001	+1
0010	+2
0011	+3
0100	+4
0101	+5
0110	+6
0111	+7

TO[3:0]	Calculation
1000	-8
1001	-7
1010	-6
1011	-5
1100	-4
1101	-3
1110	-2
1111	-1

17) Temperature Sensor Write (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Write External Temperature Sensor	0	0	0	1	0	0	0	0	1	0	42H
	0	1	WATTR[7:0]								00H
	0	1	WMSB[7:0]								00H
	0	1	WLSB[7:0]								00H

This command reads the temperature sensed by the temperature sensor.
WATTR: D[7:6]: I2C Write Byte Number
00b : 1 byte (head byte only)
01b : 2 bytes (head byte + pointer)
10b : 3 bytes (head byte + pointer + 1st parameter)
11b : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)
D[5:3]: User-defined address bits (A2, A1, A0)
D[2:0]: Pointer setting
WMSB[7:0]: MSByte of write-data to external temperature sensor
WLSB[7:0]: LSByte of write-data to external temperature sensor

18) TEMPERATURE SENSOR READ (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read External Temperature Sensor	0	0	0	1	0	0	0	0	1	1	43H
	1	1	RMSB[7:0]								00H
	1	1	RLSB[7:0]								00H

This command reads the temperature sensed by the temperature sensor.
RMSB[7:0]: MSByte read data from external temperature sensor
RLSB[7:0]: LSByte read data from external temperature sensor

19) VCOM and Data Interval Setting(CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Interval between VCOM and Data	0	0	0	1	0	1	0	0	0	0	50h
	0	1	VBD[1:0]		DDX[1:0]		CDI[3:0]				31h

This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).
VBD[1:0]: Border data selection
Under K/W/Red mode (KW/R=0):

DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTR
	10	LUTW
	11	LUTK
1 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	Floating

Under K/W mode (KW/R=1):

DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	Floating
1 (Default)	00	Floating
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	Floating

DDX[1:0]: Data polality.
Under K/W/Red mode (KW/R=0):
DDX[1] is for RED data.
DDX[0] is for BW data

DDX[1:0]	Data {Red, K/W}	LUT
00	00	LUTW
	01	LUTK
	10	LUTR
	11	LUTR
01 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	LUTR

DDX[1:0]	Data {Red, K/W}	LUT
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTK
11	00	LUTR
	01	LUTR
	10	LUTK
	11	LUTW

Under K/W mode (KW/R=1):
DDX[1]=0 is for KW mode with NEW/OLD,
DDX[1]=1 is for KW mode without NEW/OLD.

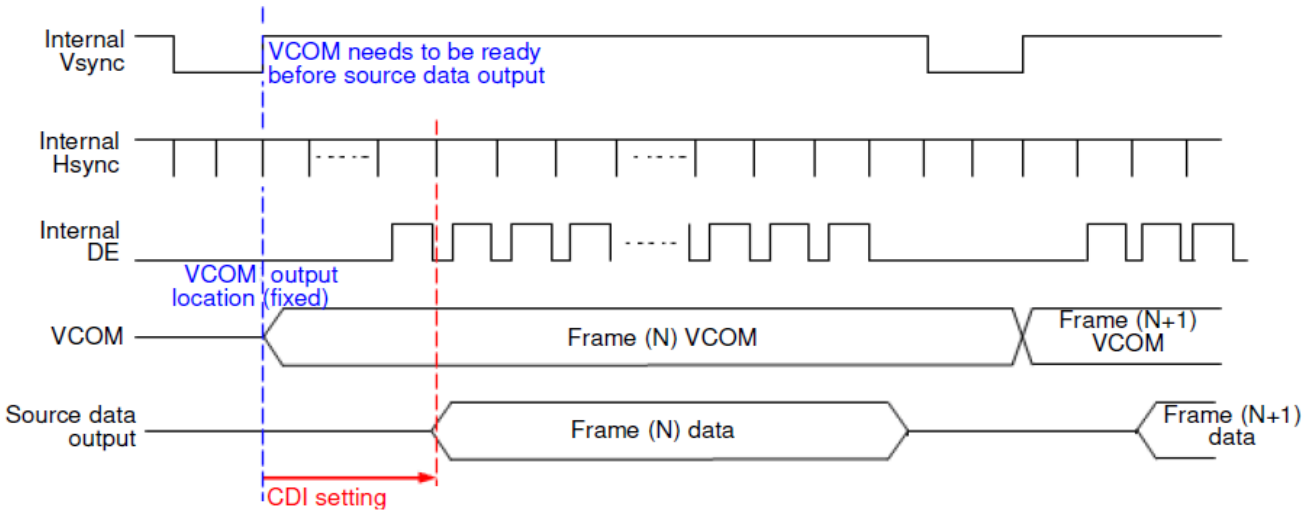
DDX[1:0]	Data {NEW, OLD}	LUT
00	00	LUTWW (0 → 0)
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	LUTKK (1 → 1)
01 (Default)	00	LUTKK (0 → 0)
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	LUTWW (1 → 1)

DDX[1:0]	Data {NEW}	LUT
10	0	LUTKW (1 → 0)
	1	LUTWK (0 → 1)
11	0	LUTWK (1 → 0)
	1	LUTKW (0 → 1)

CDI[3:0]: Vcom and data interval

CDI[3:0]	VCOM and Data Interval
0000 b	17 hsync
0001	16
0010	15
0011	14
0100	13
0101	12
0110	11
0111	**10 (Default)**

CDI[3:0]	VCOM and Data Interval
1000	9
1001	8
1010	7
1011	6
1100	5
1101	4
1110	3
1111	2



20) Low Power Detection(LPD) (R51h)

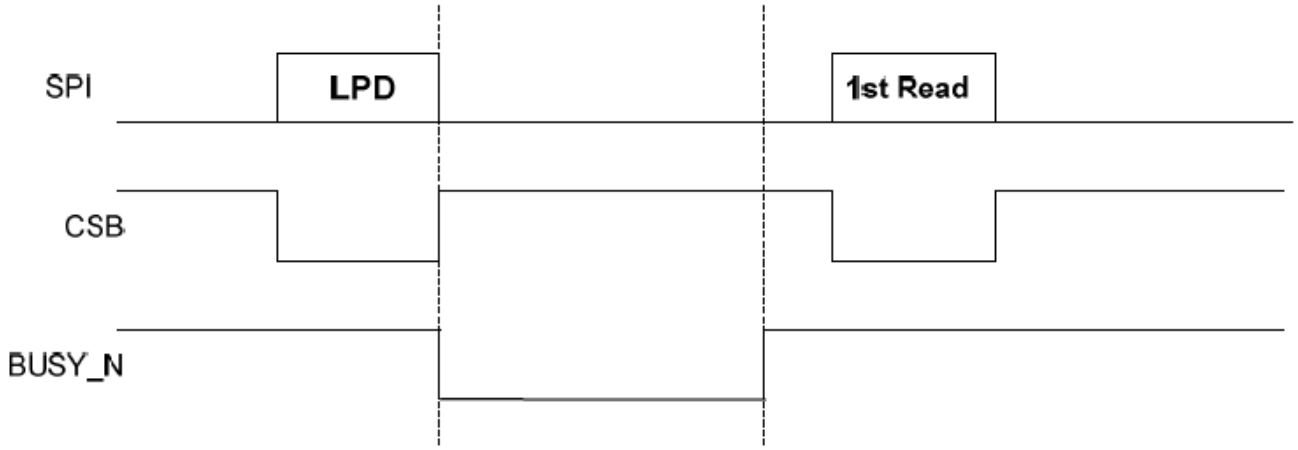
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Detect Low Power	0	0	0	1	0	1	0	0	0	1	51h
	1	1	-	-	-	-	-	-	-	LPD	01h

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal Low Power Detection Flag

0: Low power input (VDD<2.5V, selected by LVD_SEL[1:0] in command LVSEL)

1: Normal status (default)



21) TCON Setting(TCON) (R60h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Non-overlap Period	0	0	0	1	1	0	0	0	0	0	60h
	0	1	S2G[3:0]				G2S[3:0]				22h

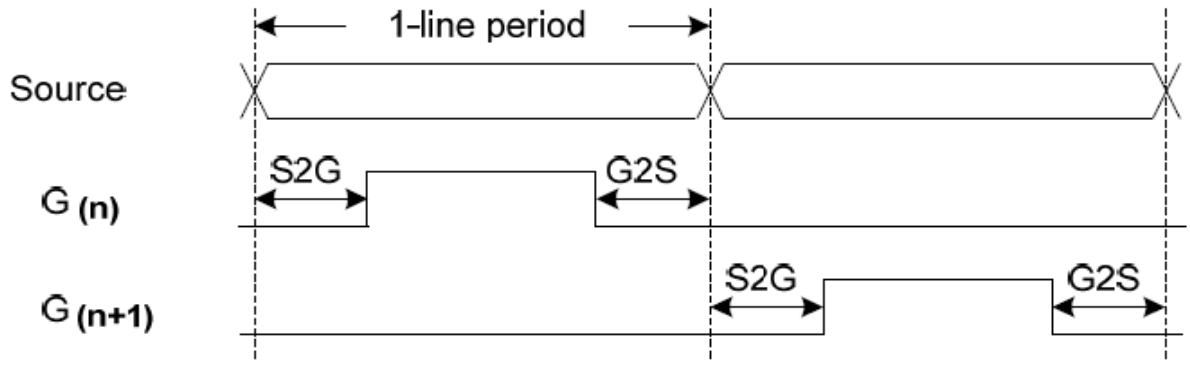
This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period
0000b	4
0001	8
0010	**12 (Default)**
0011	16
0100	20
0101	24
0110	28
0111	32

S2G[3:0] or G2S[3:0]	Period
1000b	36
1001	40
1010	44
1011	48
1100	52
1101	56
1110	60
1111	64

Period = 660 nS.



22) Resolution Setting(TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display Resolution	0	0	0	1	1	0	0	0	0	1	61h
	0	1	HRES[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	-	VRES[8]	00h
	0	1	VRES[7:0]								00h

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).
HRES[7:3]: Horizontal Display Resolution
VRES[8:0]: Vertical Display Resolution
Active channel calculation, assuming HST[7:3]=0, VST[8:0]=0:
Gate: First active gate = G0;
Last active gate = VRES[8:0] – 1
Source: First active source = X (If HRES[7:0]>160, X=0; otherwise, X=8)
Last active source = HRES[7:0] - 1 + X (If HRES[7:0]>160, X=0; otherwise, X=8)
Example: For 128 (source) x 272 (gate), assuming HST[7:3]=0, VST[8:0]=0
Gate: First active gate = G0,
Last active gate = G271 (VRES[8:0] = 272; 272 - 1= 271)
Source: First active source = S8, (HRES[7:0]≤160 therefore X=8)
Last active source = S135; (128 - 1 + 8 = 135)

23) GATE/SOURCE START SETTING (GSST) (R65H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Start	0	0	0	1	1	0	0	1	0	1	65h
	0	1	HST[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	-	VST[8]	00h
	0	1	VST[7:0]								00h

This command defines resolution start gate/source position.
HST[7:3]: Horizontal Display Start Position (Source)
VST[8:0]: Vertical Display Start Position (Gate)
Example : For 128(Source) x 240(Gate)
HST[7:0] = 32
VST[8:0] = 32
Gate: First active gate = G32 (VST[8:0] = 32),
Last active gate = G271 (240-1+32=271)
Source: First active source = S40 (HST[7:0] = 32, X=8, 32+8 = 40), (Note)
Last active source = S167 (128-1+32+8=167)
Note: If HRES[7:0] > 160, X=8; otherwise X=8.

24) Revision(REV) (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Chip Revision	0	0	0	1	1	1	0	0	0	0	70h
	1	1	Reserved								00h
	1	1	CHIP_REV[7:0]								0Ah
	1	1	LUT_REV[7:0]								FFh
	1	1	LUT_REV[15:8]								FFh
	1	1	LUT_REV[23:16]								FFh

The LUT_REV is read from OTP address = 0x0017~0X0019 / 0x1017~0X1019.
CHIP_REV[7:0]: Chip Revision, it is fixed by “0x0Ah”.

25) Get status(FLG) (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read Flags	0	0	0	1	1	1	0	0	0	1	71h
	1	1	-	PTL_ flag	I²C_ERR	I²C_ BUSYN	data_ flag	PON	POF	BUSY_N	13h

This command reads the IC status.
PTL_FLAG Partial display status (high: partial mode)
I²C_ERR: I²C master error status
I²C_BUSYN: I²C master busy status (low active)
data_flag: Driver has already received all the one frame data
PON: Power ON status
POF: Power OFF status
BUSY_N: Driver busy status (low active)

26) Auto measure vcom(AMV) (R80h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure VCOM	0	0	1	0	0	0	0	0	0	0	80h
	0	1	-	-	AMVT[1:0]		XON	AMVS	AMV	AMVE	10h

This command reads the IC status.
AMVT[1:0]: Auto Measure VCOM Time
00b: 3s 01b: 5s (default)
10b: 8s 11b: 10s
XON: All Gate ON of AMV
0: Gate normally scan during Auto Measure VCOM period. (default)
1: All Gate ON during Auto Measure VCOM period.
AMVS: Source output of AMV
0: Source output 0V during Auto Measure VCOM period. (default)
1: Source output VDHR during Auto Measure VCOM period.
AMV: Analog signal
0: Get VCOM value with the VV command (R81h) (default)
1: Get VCOM value in analog signal. (External analog to digital converter)
AMVE: Auto Measure VCOM Enable (/Disable)
0: No effect
1: Trigger auto VCOM sensing.

27) VCOM Value(VV) (R81h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure VCOM	0	0	1	0	0	0	0	0	0	1	81h
	1	1	-	VV[6:0]							00h

This command gets the VCOM value.

VV[6:0]: VCOM Value Output

VV [6:0]	VCOM Voltage (V)	VV [6:0]	VCOM Voltage (V)	VV [6:0]	VCOM Voltage (V)
0000000b	-0.1	0101011b	-4.4	1010110b	-8.7
0000001b	-0.2	0101100b	-4.5	1010111b	-8.8
0000010b	-0.3	0101101b	-4.6	1011000b	-8.9
0000011b	-0.4	0101110b	-4.7	1011001b	-9
0000100b	-0.5	0101111b	-4.8	1011010b	-9.1
0000101b	-0.6	0110000b	-4.9	1011011b	-9.2
0000110b	-0.7	0110001b	-5	1011100b	-9.3
0000111b	-0.8	0110010b	-5.1	1011101b	-9.4
0001000b	-0.9	0110011b	-5.2	1011110b	-9.5
0001001b	-1	0110100b	-5.3	1011111b	-9.6
0001010b	-1.1	0110101b	-5.4	1100000b	-9.7
0001011b	-1.2	0110110b	-5.5	1100001b	-9.8
0001100b	-1.3	0110111b	-5.6	1100010b	-9.9
0001101b	-1.4	0111000b	-5.7	1100011b	-10
0001110b	-1.5	0111001b	-5.8	1100100b	-10.1
0001111b	-1.6	0111010b	-5.9	1100101b	-10.2
0010000b	-1.7	0111011b	-6	1100110b	-10.3
0010001b	-1.8	0111100b	-6.1	1100111b	-10.4
0010010b	-1.9	0111101b	-6.2	1101000b	-10.5
0010011b	-2	0111110b	-6.3	1101001b	-10.6
0010100b	-2.1	0111111b	-6.4	1101010b	-10.7
0010101b	-2.2	1000000b	-6.5	1101011b	-10.8
0010110b	-2.3	1000001b	-6.6	1101100b	-10.9
0010111b	-2.4	1000010b	-6.7	1101101b	-11
0011000b	-2.5	1000011b	-6.8	1101110b	-11.1
0011001b	-2.6	1000100b	-6.9	1101111b	-11.2
0011010b	-2.7	1000101b	-7	1110000b	-11.3
0011011b	-2.8	1000110b	-7.1	1110001b	-11.4
0011100b	-2.9	1000111b	-7.2	1110010b	-11.5
0011101b	-3	1001000b	-7.3	1110011b	-11.6
0011110b	-3.1	1001001b	-7.4	1110100b	-11.7
0011111b	-3.2	1001010b	-7.5	1110101b	-11.8
0100000b	-3.3	1001011b	-7.6	1110110b	-11.9
0100001b	-3.4	1001100b	-7.7	1110111b	-12
0100010b	-3.5	1001101b	-7.8	1111000b	-12.1
0100011b	-3.6	1001110b	-7.9	1111001b	-12.2
0100100b	-3.7	1001111b	-8	1111010b	-12.3
0100101b	-3.8	1010000b	-8.1	1111011b	-12.4
0100110b	-3.9	1010001b	-8.2	1111100b	-12.5
0100111b	-4	1010010b	-8.3	1111101b	-12.6
0101000b	-4.1	1010011b	-8.4	1111110b	-12.7
0101001b	-4.2	1010100b	-8.5		
0101010b	-4.3	1010101b	-8.6		

28) VCOM-DC Setting(VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set VCOM_DC	0	0	1	0	0	0	0	0	1	0	82h
	0	1	-	VDCS[6:0]							00h

This command sets VCOM_DC value

VDCS[6:0]: VCOM_DC Setting

VDCS [6:0]	VCOM Voltage (V)	VDCS [6:0]	VCOM Voltage (V)	VDCS [6:0]	VCOM Voltage (V)
0000000b	-0.1	0101011b	-4.4	1010110b	-8.7
0000001b	-0.2	0101100b	-4.5	1010111b	-8.8
0000010b	-0.3	0101101b	-4.6	1011000b	-8.9
0000011b	-0.4	0101110b	-4.7	1011001b	-9
0000100b	-0.5	0101111b	-4.8	1011010b	-9.1
0000101b	-0.6	0110000b	-4.9	1011011b	-9.2
0000110b	-0.7	0110001b	-5	1011100b	-9.3
0000111b	-0.8	0110010b	-5.1	1011101b	-9.4
0001000b	-0.9	0110011b	-5.2	1011110b	-9.5
0001001b	-1	0110100b	-5.3	1011111b	-9.6
0001010b	-1.1	0110101b	-5.4	1100000b	-9.7
0001011b	-1.2	0110110b	-5.5	1100001b	-9.8
0001100b	-1.3	0110111b	-5.6	1100010b	-9.9
0001101b	-1.4	0111000b	-5.7	1100011b	-10
0001110b	-1.5	0111001b	-5.8	1100100b	-10.1
0001111b	-1.6	0111010b	-5.9	1100101b	-10.2
0010000b	-1.7	0111011b	-6	1100110b	-10.3
0010001b	-1.8	0111100b	-6.1	1100111b	-10.4
0010010b	-1.9	0111101b	-6.2	1101000b	-10.5
0010011b	-2	0111110b	-6.3	1101001b	-10.6
0010100b	-2.1	0111111b	-6.4	1101010b	-10.7
0010101b	-2.2	1000000b	-6.5	1101011b	-10.8
0010110b	-2.3	1000001b	-6.6	1101100b	-10.9
0010111b	-2.4	1000010b	-6.7	1101101b	-11
0011000b	-2.5	1000011b	-6.8	1101110b	-11.1
0011001b	-2.6	1000100b	-6.9	1101111b	-11.2
0011010b	-2.7	1000101b	-7	1110000b	-11.3
0011011b	-2.8	1000110b	-7.1	1110001b	-11.4
0011100b	-2.9	1000111b	-7.2	1110010b	-11.5
0011101b	-3	1001000b	-7.3	1110011b	-11.6
0011110b	-3.1	1001001b	-7.4	1110100b	-11.7
0011111b	-3.2	1001010b	-7.5	1110101b	-11.8
0100000b	-3.3	1001011b	-7.6	1110110b	-11.9
0100001b	-3.4	1001100b	-7.7	1110111b	-12
0100010b	-3.5	1001101b	-7.8	1111000b	-12.1
0100011b	-3.6	1001110b	-7.9	1111001b	-12.2
0100100b	-3.7	1001111b	-8	1111010b	-12.3
0100101b	-3.8	1010000b	-8.1	1111011b	-12.4
0100110b	-3.9	1010001b	-8.2	1111100b	-12.5
0100111b	-4	1010010b	-8.3	1111101b	-12.6
0101000b	-4.1	1010011b	-8.4	1111110b	-12.7
0101001b	-4.2	1010100b	-8.5		
0101010b	-4.3	1010101b	-8.6		

29) PARTIAL WINDOW (PTL) (R90H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Partial Window	0	0	1	0	0	0	0	0	1	0	90h
	0	1	HRST[7:3]					0	0	0	00h
	0	1	HRED[7:3]					1	1	1	07h
	0	1	-	-	-	-	-	-	-	VRST[8]	00h
	0	1	VRST[7:0]								00h
	0	1	-	-	-	-	-	-	-	VRED[8]	00h
	0	1	VRED[7:0]								00h
	0	1	-	-	-	-	-	-	-	PT_SCAN	01h

This command sets partial window.
HRST[7:3]: Horizontal start channel bank. (value 00h~13h)
HRED[7:3]: Horizontal end channel bank. (value 00h~13h). HRED must be greater than HRST.
VRST[8:0]: Vertical start line. (value 000h~127h)
VRED[8:0]: Vertical end line. (value 000h~127h). VRED must be greater than VRST.
PT_SCAN: 0: Gates scan only inside of the partial window.
1: Gates scan both inside and outside of the partial window. (default)

30) PARTIAL IN (PTIN) (R91H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial In	0	0	1	0	0	1	0	0	0	1	91h

This command makes the display enter partial mode.

31) PARTIAL OUT (PTOUT) (R92H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial Out	0	0	1	0	0	1	0	0	1	0	92h

This command makes the display exit partial mode and enter normal mode.

32) PROGRAM MODE (PGM) (RA0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enter Program Mode	0	0	1	0	1	0	0	0	0	0	A0h

After this command is issued, the chip would enter the program mode.
After the programming procedure completed, a hardware reset is necessary for leaving program mode.

33) ACTIVE PROGRAM (APG) (RA1H)

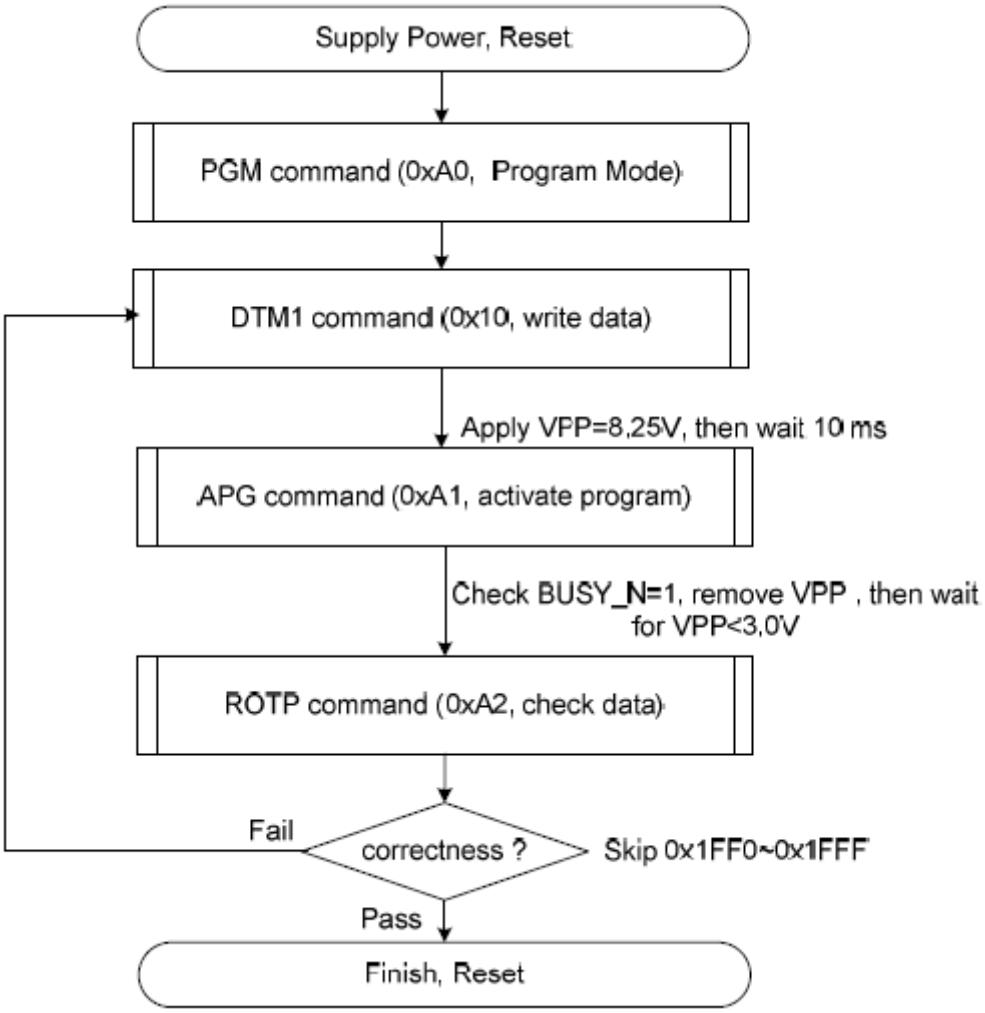
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Active Program OTP	0	0	1	0	1	0	0	0	0	1	A1h

After this command is transmitted, the programming state machine would be activated.
The BUSY flag would fall to 0 until the programming is completed.

34) READ OTP DATA (ROTP) (RA2H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read OTP data for check	0	0	1	0	1	0	0	0	1	0	A2h
	1	1	Dummy								--
	1	1	The data of address 0x000 in the OTP								--
	1	1	The data of address 0x001 in the OTP								--
	1	1	:								--
	1	1	The data of address (n-1) in the OTP								--
	1	1	The data of address (n) in the OTP								--

The command is used for reading the content of OTP for checking the data of programming.
The value of (n) is depending on the amount of programmed data, the max address = 0x17FF.



35) CASCADE SETTING (CCSET) (RE0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Cascade Option	0	0	1	1	1	0	0	0	0	0	E0h
	0	1	-	-	-	-	-	-	TSFIX	CCEN	00h

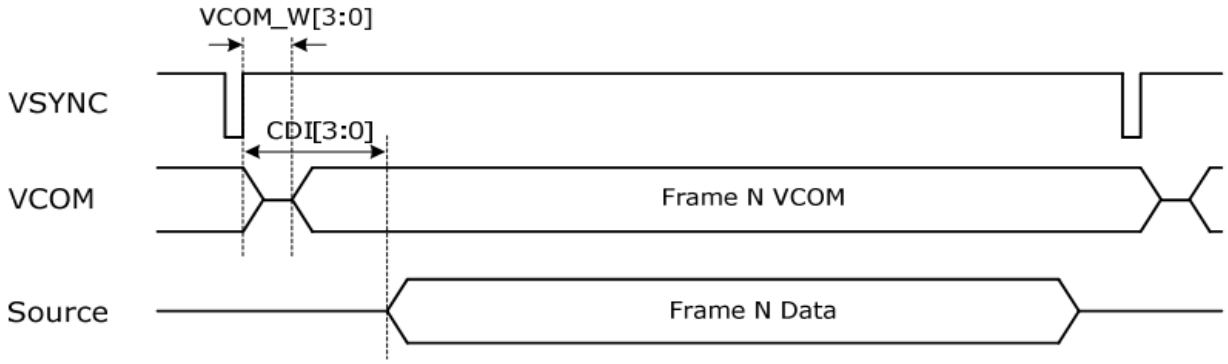
This command is used for cascade.
CCEN: Output clock enable/disable.
0: Output 0V at CL pin. (default)
1: Output clock at CL pin for slave chip.
TSFIX: Let the value of slave's temperature is same as the master's.
0: Temperature value is defined by internal temperature sensor / external LM75. (default)
1: Temperature value is defined by TS_SET[7:0] registers.

36) POWER SAVING (PWS) (RE3H)

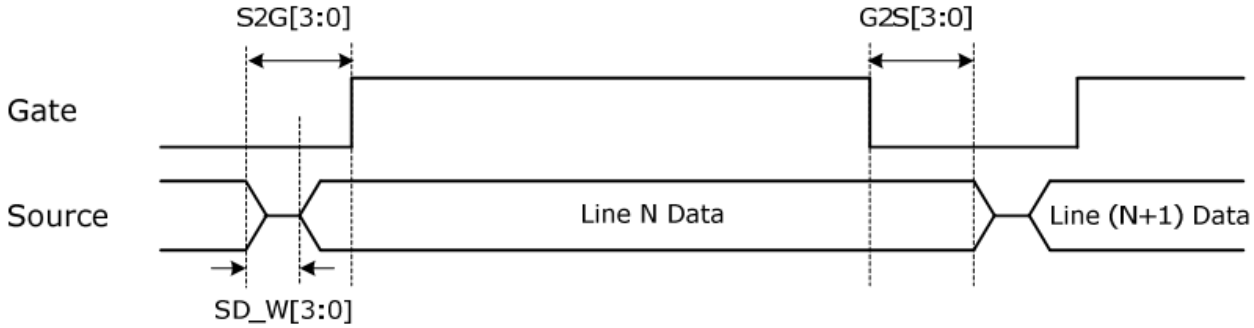
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Power Saving for VCOM & Source	0	0	1	1	1	0	0	0	1	1	E3h
	0	1	VCOM_W[3:0]				SD_W[3:0]				00h

This command is set for saving power during fresh period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W[3:0]: VCOM power saving width (unit = line period)



SD_W[3:0]: Source power saving width (unit = 660nS)



37) LVD VOLTAGE SELECT (LVSEL) (RE4H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Select LVD Voltage	0	0	1	1	1	0	0	1	0	0	E4h
	0	1	-	-	-	-	-	-	LVD_SEL[1:0]		03h

LVD_SEL[1:0]: Low Power Voltage selection

LVD_SEL[1:0]	LVD value
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5 V (default)

38) FORCE TEMPERATURE (TSSET) (RE5H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Force Temperature Value for Cascade	0	0	1	1	1	0	0	1	0	1	E5h
	0	1	TS_SET[7:0]								00h

This command is used for cascade to fix the temperature value of master and slave chip.

8 . HOST INTERFACES

E0213A108 provides 3-wire/4-wire serial interface for command and display data transferred from the MCU. The serial interface supports 8-bit mode. Data can be input/output by clocks while the chip is active (CSB =LOW). While input, data are written in order from MSB at the clock rising edge. When too many parameters are input, the chip accepts only defined parameters, and ignores undefined ones.

BS	Interface	CSB	DC	SCL	SDA
High	3-wire SPI	Available	Fix to GND	Available	Available
Low	4-wire SPI	Available	Available	Available	Available

3 wire SPI format

Data / Command is recognized with the first bit transferred. Data are transferred in the unit of 9 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 9 bits. (The serial counter is reset at the rising edge of the CSB signal.)

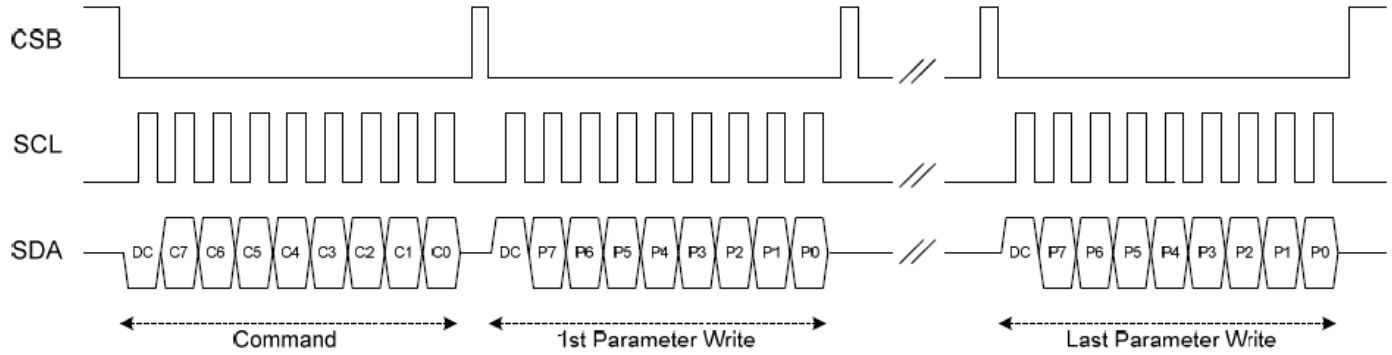


Figure: 3-wire SPI write operation

The MSB bit of data will be output at SDA pin after the 1st SCL falling edge, if the 1st input data at SDA is high. Only in the case of OTP data read, the 1st packet of output data are dummy data.

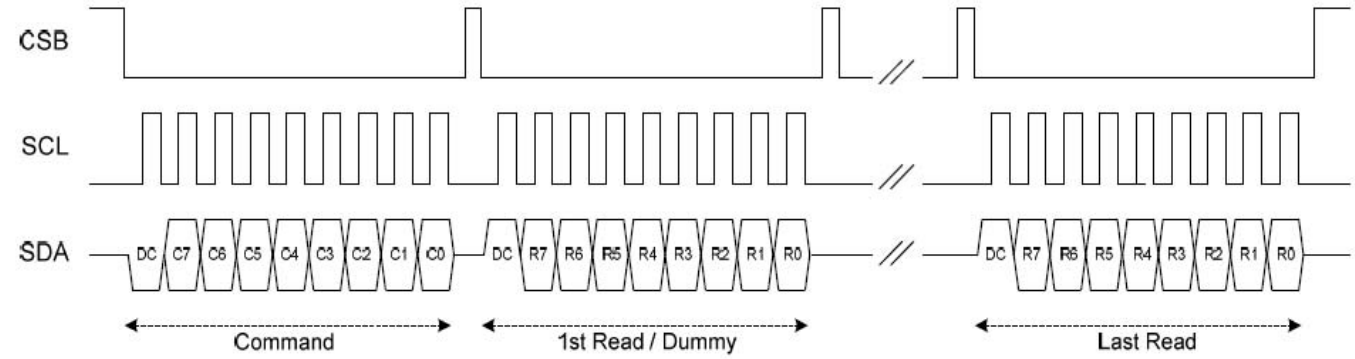


Figure: 3-wire SPI read operation

4 wire SPI format

Data / Command is recognized with DC pin. Data are transferred in the unit of 8 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 8 bits. (The serial counter is reset at the rising edge of the CSB signal.)

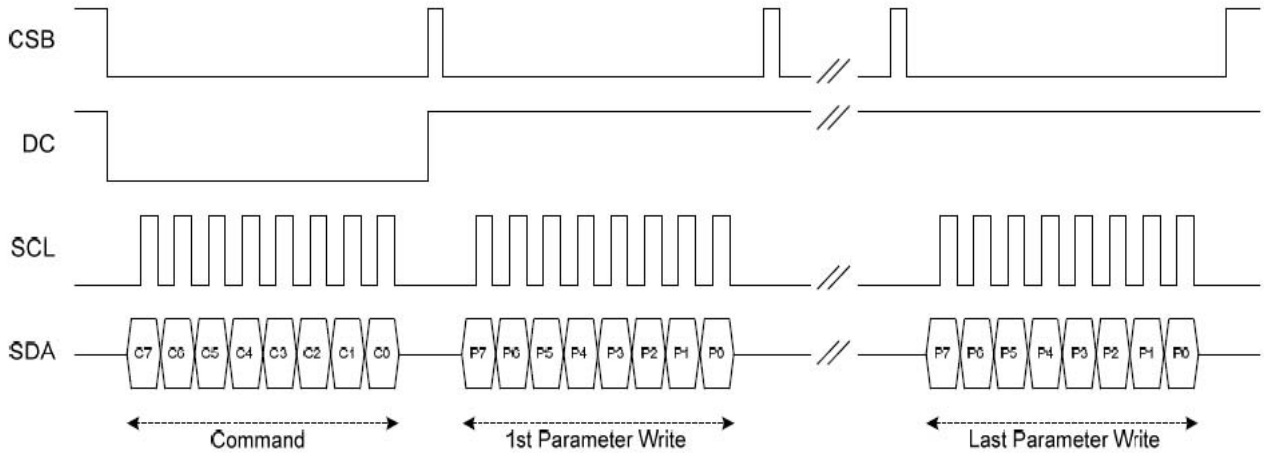


Figure: 4-wire SPI write operation

The MSB bit of data will be output at SDA pin after the CSB falling edge, if DC pin is High. Only in the case of OTP data read, the 1st packet of output data are dummy data.

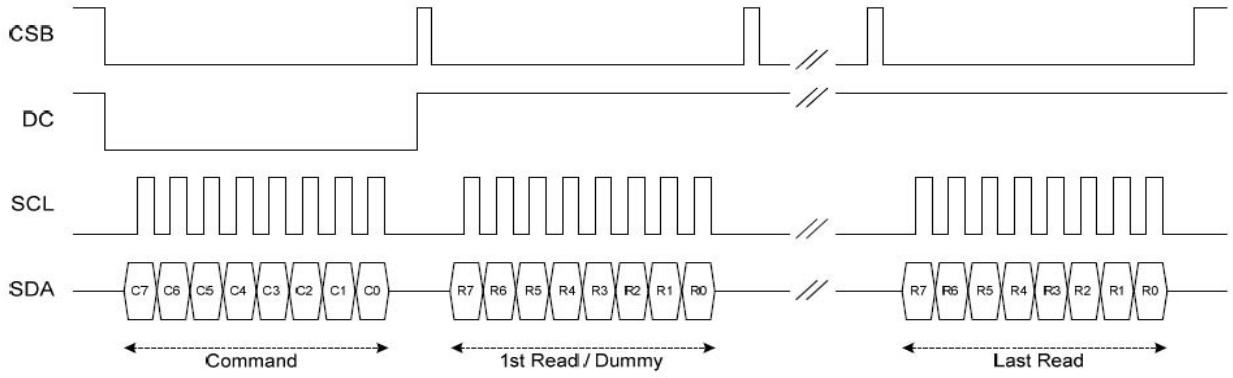
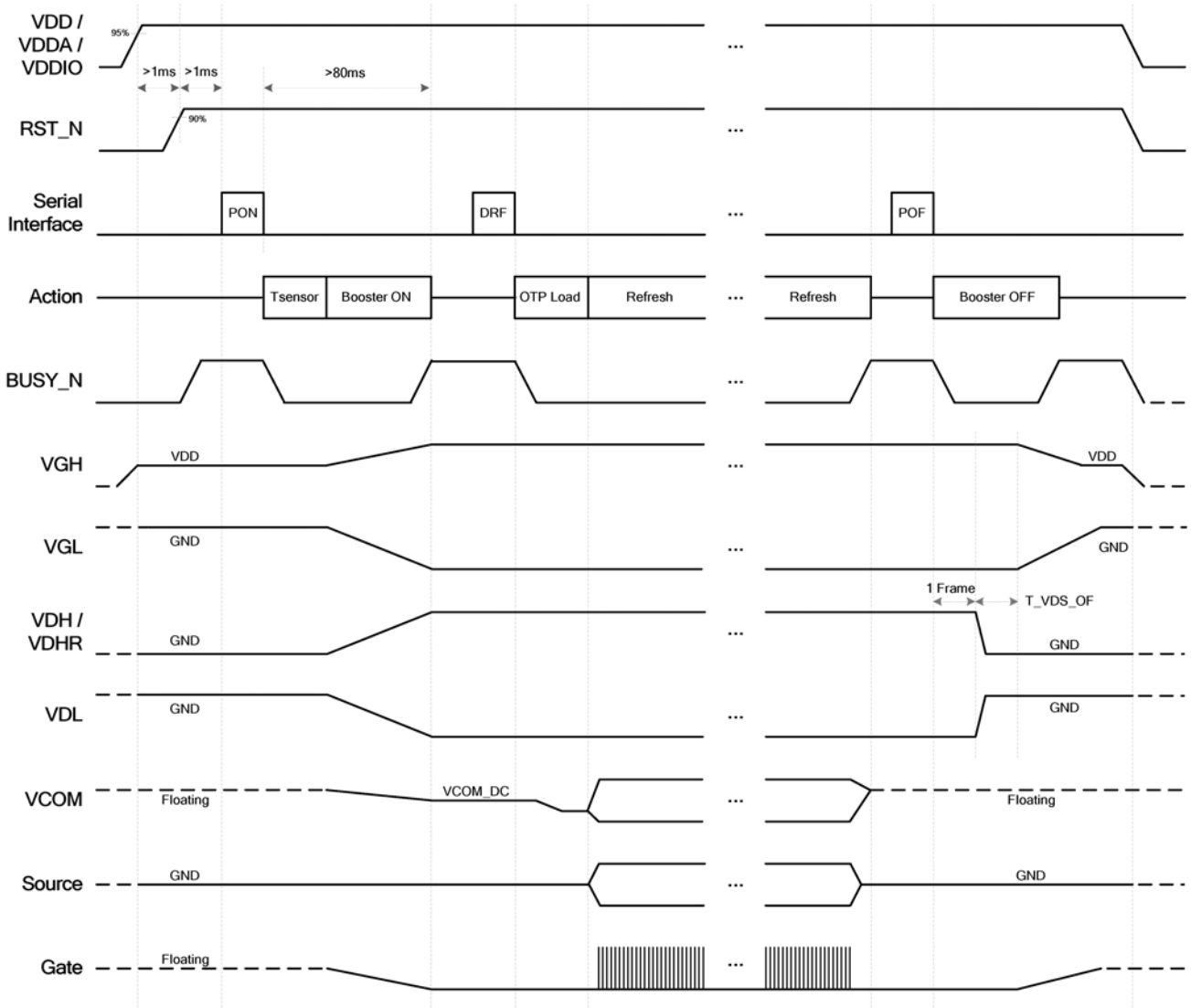


Figure: 4-wire SPI read operation

9. Power ON/OFF Sequence

1. Temperature sensor will be activated automatically for one-time sensing before enabling booster.
2. After refreshing display, VCOM will be set to floating automatically.
3. In OTP mode (REG_EN=0), the LUT in OTP will be copied to register automatically after the DSP/DRF command.
4. After RST_N rising, the waiting time for internal initial processing, greater than 1mS, is necessary. Any commands transmitted to chip during this time will be ignored.



10. Reference Circuit

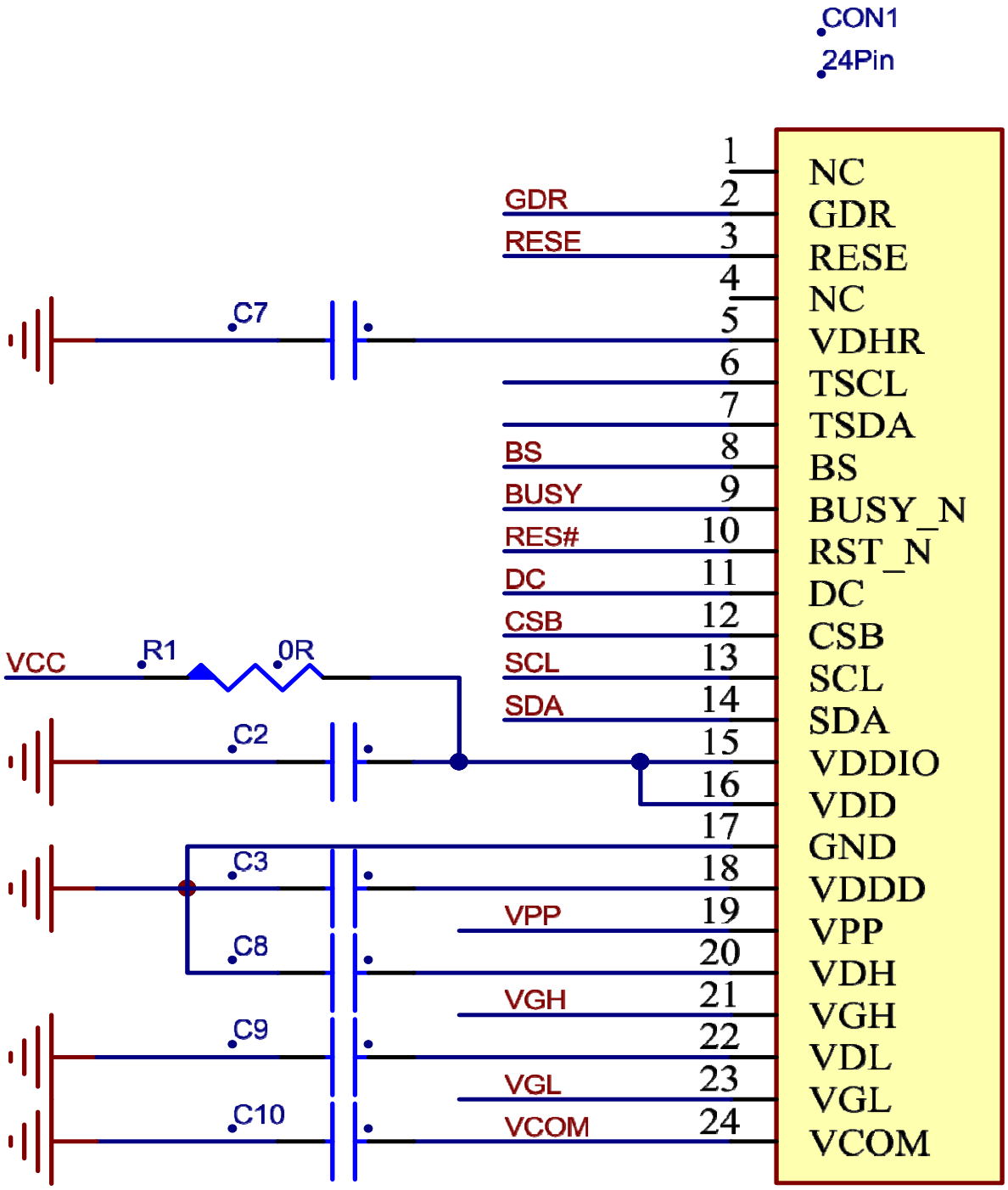


Figure 10-1

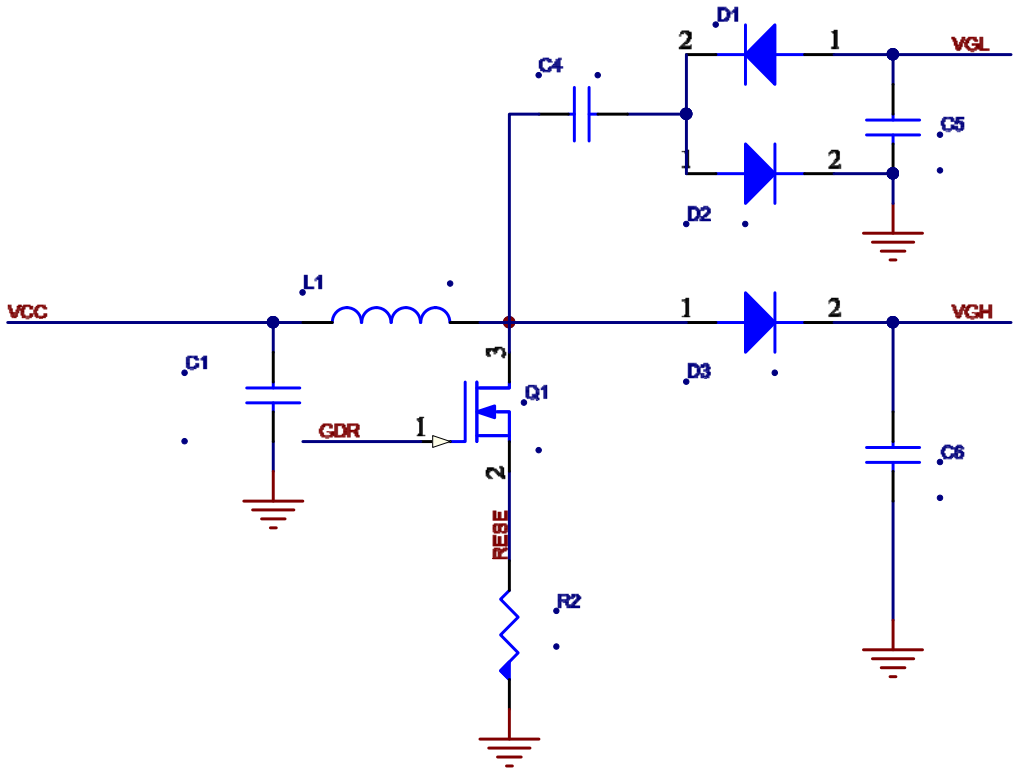


Figure 10-2

Part Name	Value /requirement/Reference Part
C1—C3	1uF/0603;X5R/;Voltage Rating: 25V
C4	4.7uF/0603;X5R;Voltage Rating: 25V
C5-C10	1uF/0603;X5R;Voltage Rating: 25V
D1—D3	MBR0530 1) Reverse DC voltage≥30V 2) Forward current≥500mA 3)Forward voltage≤430mV
R2	0.47 Ω/0603： 1% variation
Q1	NMOS:Si1308EDL 1） Drain-Source breakdown voltage ≥30V 2） Vgs（th）=0.9（Typ），1.3V（Max） 3） Rds on≤ 2.1Ω @ Vgs=2.5V
L1	10uH/NRH3010T100MN
CON24Pin	0.5mm ZIF Socket 24Pins,0.5mm pitch

11. ABSOLUTE MAXIMUM RATINGS

Table 11-1: Maximum Ratings

Symbol	Parameter	Rating	Unit	Humidity	Unit	Note
V_{DD}	Logic supply voltage	-0.3 to +6.0	V	-	-	
T_{OPR}	Operation temperature range	0 to 40	℃	45 to70	%	Note 11-1
Tttg	Transportation temperature range	-25 to 60	℃	45 to70	%	Note11-2
Tstg	Storage condition	0 to 40	℃	45 to70	%	Maximum storage time: 5 years
-	After opening the package	0 to 40	℃	45 to70	%	

Note 11-1： We guarantee the single pixel display quality for 0-35℃, but we only guarantee the barcode readable for 35-40℃. Normal use is recommended to refresh every 24 hours.

Note11-2： Tttg is the transportation condition, the transport time is within 10 days for -25℃~0℃ or 40℃~60℃.

Note 11-3： When the three-color product is stored. The display screen should be kept white and face up. In addition, please be sure to refresh the e-paper every three months. We suggest that the full black and full white picture could be added to clear the screen after the module is refreshed for a long time, the display effect would be better.

12. DC CHARACTERISTICS

The following specifications apply for: VSS=0V, VDD=3.3V, T_{OPR}=25℃.

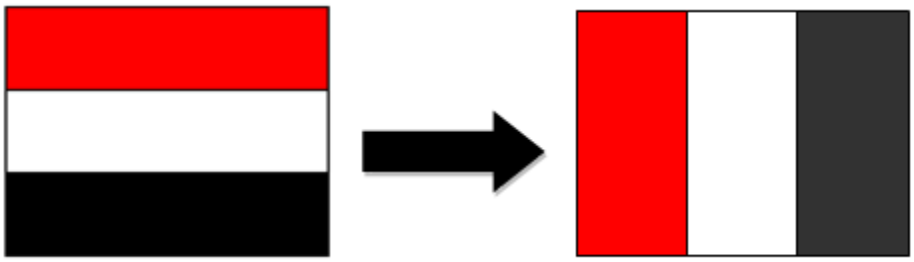
Table 12-1: DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	VDD operation voltage	-	2.5	3.3	3.6	V
VIH	High level input voltage	Digital input pins	0.7xVDDIO	-	VDDIO	V
VIL	Low level input voltage	Digital input pins	0	-	0.3xVDD	V
VOH	High level output voltage	IOH = 400uA	VDDIO-0.4	-	-	V
VOL	Low level output voltage	IOL = -400uA	0	-	0.4	V
Iupdate	Module operating current	-	-	4	-	mA
Isleep	Deep sleep mode	VDD=3.3V	-	-	0.3	uA

- The Typical power consumption is measured using associated 25℃ waveform with following pattern transition: from horizontal scan pattern to vertical scan pattern. (Note 12-1)
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by XingTai.
- Vcom value will be OTP before in factory or present on the label sticker.

Note 12-1

The Typical power consumption



13. AC CHARACTERISTICS

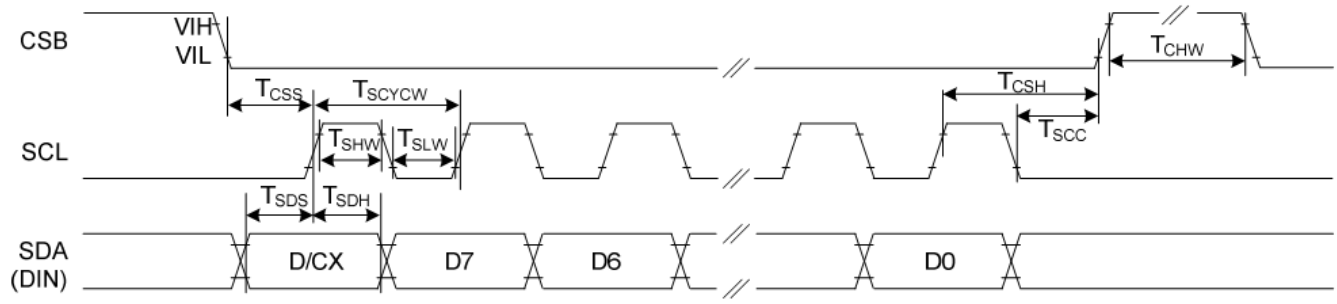


Figure: 3-wire Serial Interface Characteristics (Write mode)

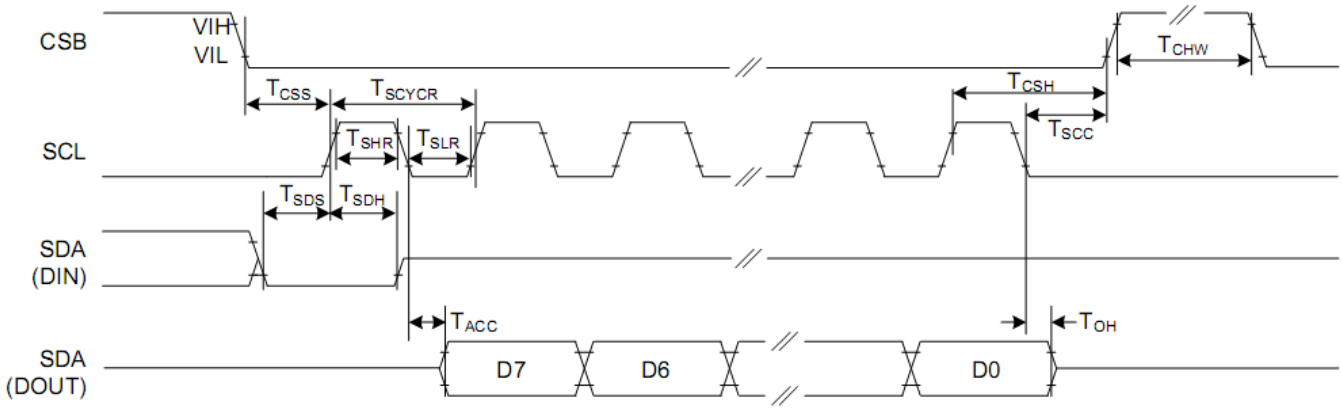


Figure: 3-wire Serial Interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	MIN	TYP.	MAX.	Unit
TCSS	CSB	Chip select setup time	60			ns
TCSH		Chip select hold time	65			ns
TSCC		Chip select setup time	20			ns
TCHW		Chip select setup time	40			ns
TSCYCW	SCL	Serial clock cycle (Write)	100			ns
TSHW		SCL “H” pulse width (Write)	35			ns
TSLW		SCL “L” pulse width (Write)	35			ns
TSCYCR		Serial clock cycle (Read)	240			ns
TSHR		SCL “H” pulse width (Read)	110			ns
TSLR		SCL “L” pulse width (Read)	110			ns
TSDS	SDA (DIN)	Data setup time	30			ns
TSDH		Data hold time	30			ns
TACC	SDA (DOUT)	Access time			240	ns
TOH		Output disable time	15			ns

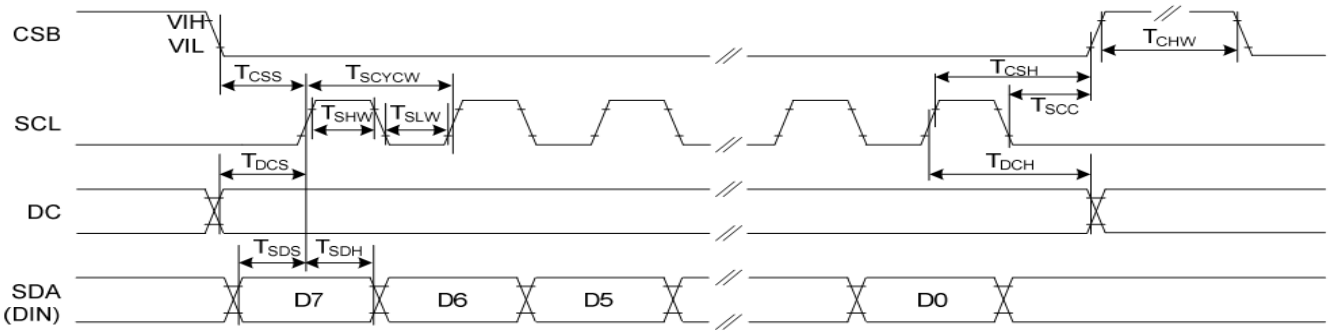


Figure: 4-wire Serial Interface Characteristics (Write mode)

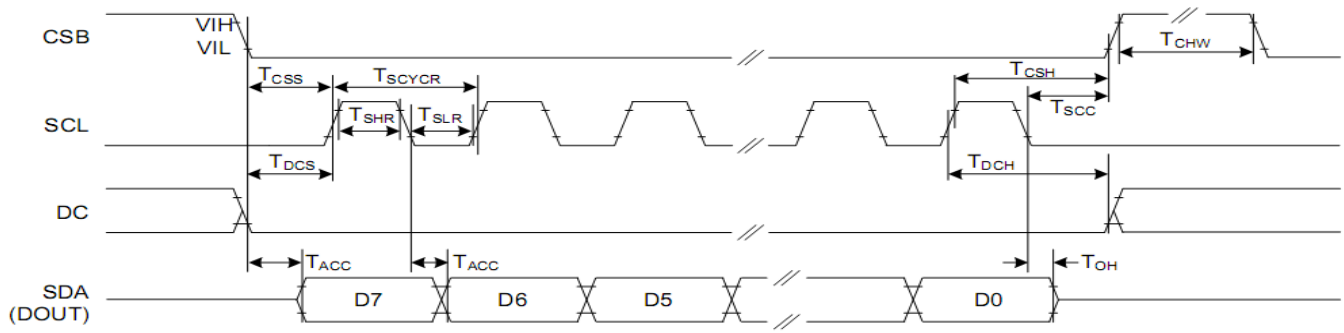


Figure: 4-wire Serial Interface Characteristics (Read mode)

TCSS	CSB	Chip select setup time	60			ns
TCSH		Chip select hold time	65			ns
TSCC		Chip select setup time	20			ns
TCHW		Chip select setup time	40			ns
TSCYCW	SCL	Serial clock cycle (Write)	100			ns
TSHW		SCL “H” pulse width (Write)	35			ns
TSLW		SCL “L” pulse width (Write)	35			ns
TSCYCR		Serial clock cycle (Read)	240			ns
TSHR		SCL “H” pulse width (Read)	110			ns
TSLR		SCL “L” pulse width (Read)	110			ns
TDCS	DC	DC setup time	30			ns
TDCH		DC hold time	30			ns
TSDS	SDA (DIN)	Data setup time	30			ns
TSDH		Data hold time	30			ns
TACC	SDA (DOUT)	Access time			240	ns
TOH		Output disable time	15			ns

14. Power Consumption

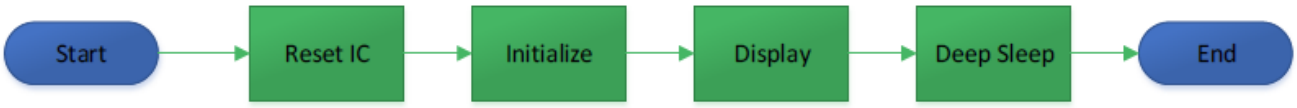
Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25℃	-	120	mAs	-
Deep sleep mode	-	25℃	-	3	uA	-

mAs=update average current× update time

15 . Typical Operating Sequence

The flow chart below to update the EPD. The steps below refer to the flow chart in the respective sections.

● EPD Driving Flow Chart

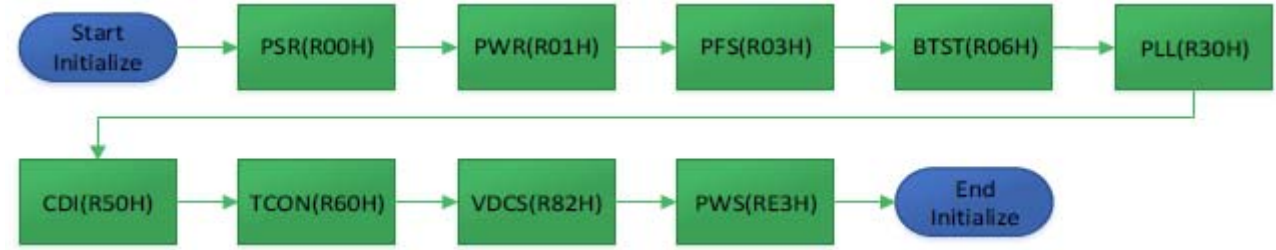


Start: To supply 2.5V –3.6V on VDD/VDDA/VDDIO then wait VDD= 95% × (2.3V~3.6V) for at least> 1ms.
End: To remove 2.5V –3.6V from VDD/VDDA/VDDIO to 0V.

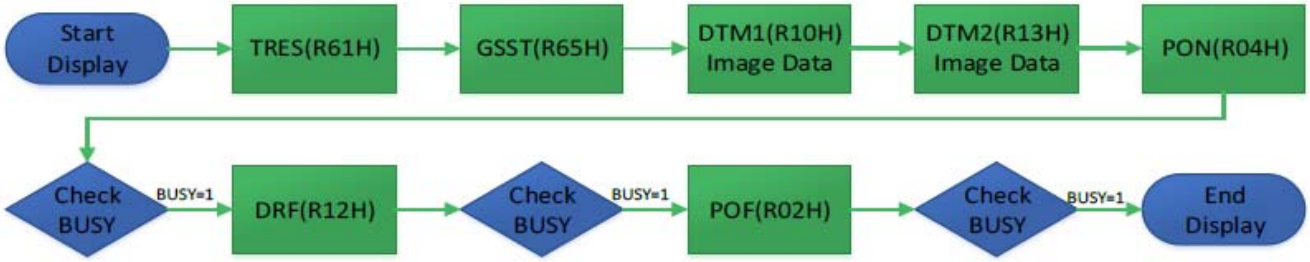
● Reset IC

End Reset IC: At this moment we will see RST_N= High, BUSY= High and VDD current is less than or equal to34uA.

● Initialize IC



● Display



End Display: At this moment we will see VGH= VDD, VGL/VDH/VDHR/VDL=0V and VDD current is less than or equal to34uA.

● Deep Sleep

End Deep Sleep: At this moment we will see VDDDO is approximately equal to0V and VDD current is less than or equal to1.1uA.Control pins defined as input types cannot be floating.

16 . Optical characteristics

16. 1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25±2℃ , VDD=3.3V

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 16-1
Gn	2Grey Level	-	-	KS+(WS-KS)×n(m-1)	-	L*	-
CR	Contrast Ratio	-	10	15	-		-
KS	Black State L* value		-	13	14		Note 16-1
	Black State a* value		-	3	4		Note 16-1
WS	White State L* value		63	65	-		Note 16-1
RS	Red State L* value	Red	25	28	-		Note 16-1
	Red State a* value	Red	36	40	-		Note 16-1
Panel	Image Update	Storage and transportation	-	Update the white screen	-	-	-
	Update Time	Operation	-	Suggest Updated once a day	-	-	-

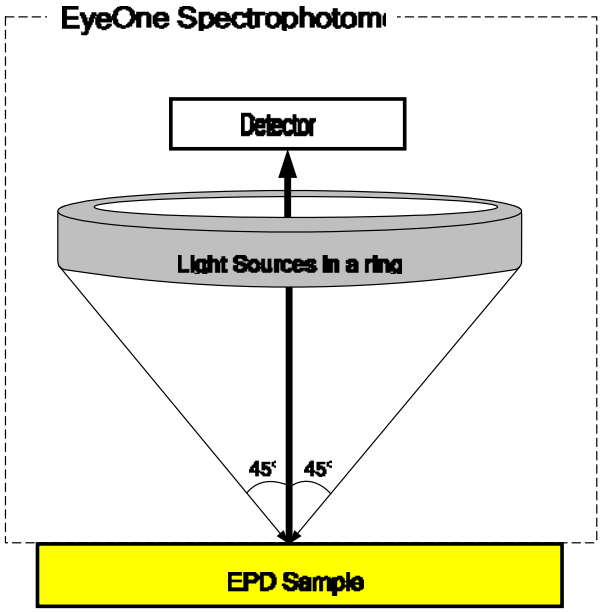
WS : White state, KS : Black State, RS: Red State

Note 16-1 : Luminance meter : i - One Pro Spectrophotometer

16. 2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd):

CR = Rl/Rd

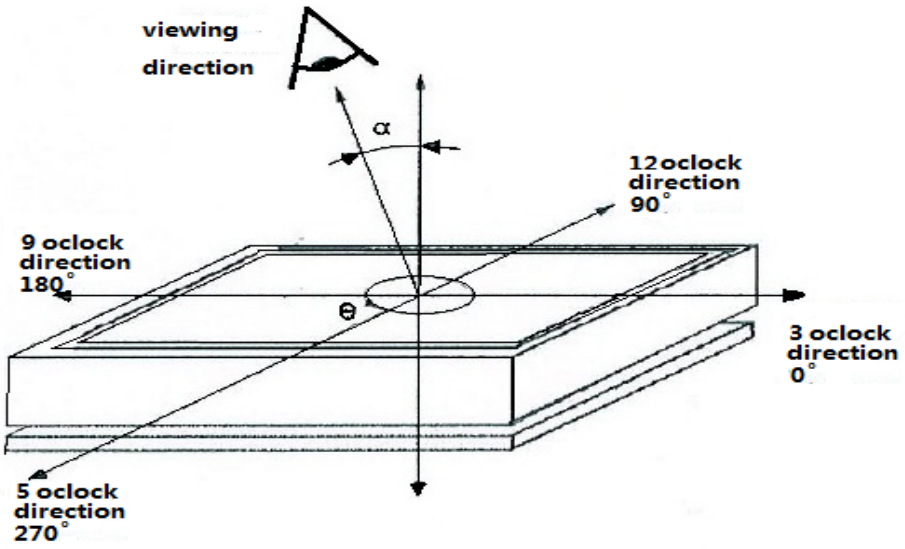


16. 3 Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factor $_{\text{white board}}$ x (L_{center} / $L_{\text{white board}}$)

L_{center} is the luminance measured at center in a white area (R=G =B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



17 . HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display module should be kept flat or fixed to a rigid, curved support with limited bending along the long axis. It should not be used for continual flexing and bending. Handle with care. Should the display break do not touch any material that leaks out. In case of contact with the leaked material then wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.
Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status	
Product specification	The data sheet contains final product specifications.

Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and dose not form part of the specification.

Product Environmental certification

ROHS

REMARK

All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

18 . Reliability test

18.1 Reliability Test Items

	TEST	CONDITION	REMARK
1	High-Temperature Operation	T=40℃, RH=35%RH, For 240Hr	
2	Low-Temperature Operation	T = 0℃ for 240 hrs	
3	High-Temperature Storage	T=50℃ RH=35%RH For 240Hr	Test in white pattern
4	Low-Temperature Storage	T = -25℃ for 240 hrs	Test in white pattern
5	High Temperature, High-Humidity Operation	T=40℃,RH=90%RH, For 168Hr	
6	High Temperature, High-Humidity Storage	T=50℃,RH=90%RH,For 240Hr	Test in white pattern
7	Temperature Cycle	-25℃(30min)~60℃(30min),50 Cycle	Test in white pattern
8	Package Vibration	1.04G,Frequency : 20~200Hz Direction : X,Y,Z Duration: 30 minutes in each direction	Full packed for shipment
9	Package Drop Impact	Drop from height of 100 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment
10	UV exposure Resistance	765 W/㎡ for 168hrs,40℃	
11	Electrostatic discharge	Machine model: +/-250V,0Ω,200pF	

Actual EMC level to be measured on customer application.

Note1：Stay white pattern for storage and non-operation test.

Note2：Operation is black/white/red pattern , hold time is 150S.

Note3：The function, appearance should meet the requirements of the test before and after the test.

Note4：Keep testing after 2 hours placing at 20℃-25℃

18.2 Product life time

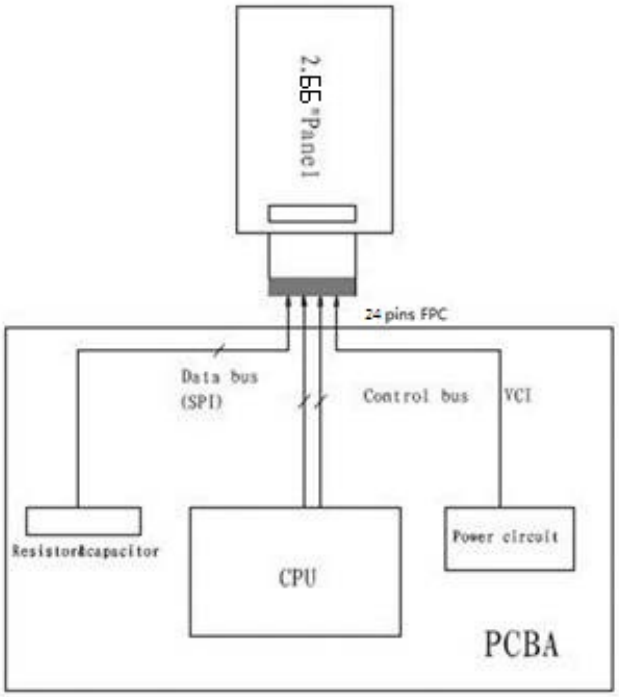
The EPD Module is designed for a 5-year life-time with 25 ℃/60%RH operation assumption. Reliability estimation testing with accelerated life-time theory would be demonstrated to provide confidence of EPD lifetime.

18.3 Product warranty

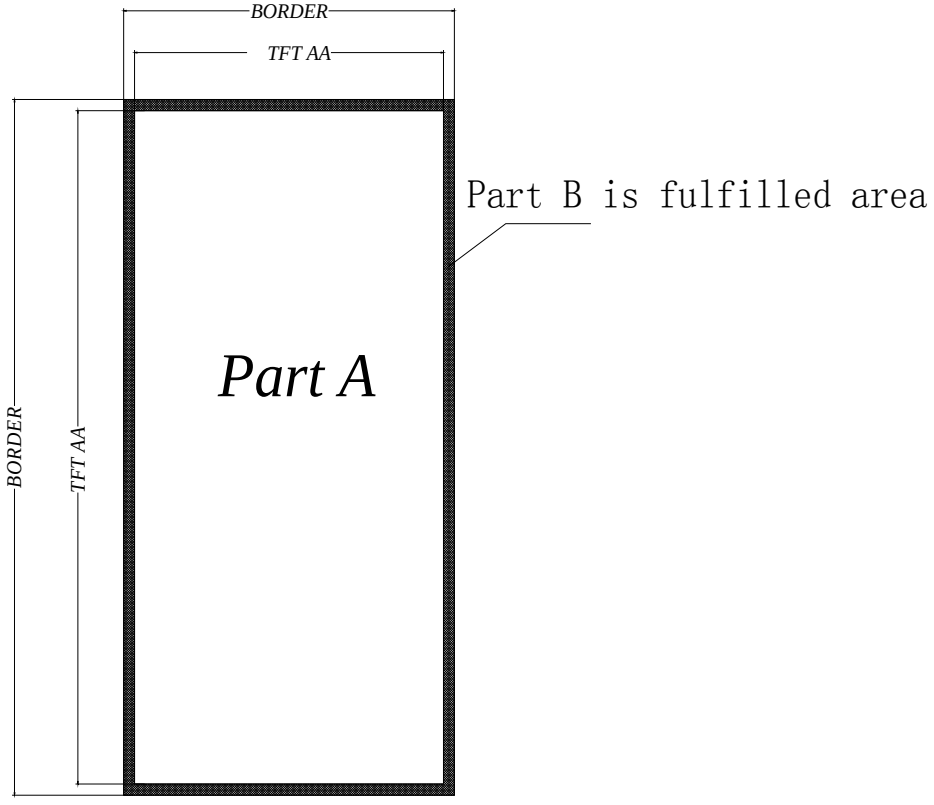
Warranty conditions have to be negotiated between Xingtai and individual customers.

Xingtai provides 12+1(one month delivery time) months warranty for all products which are purchased from Xingtai.

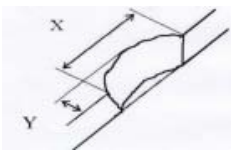
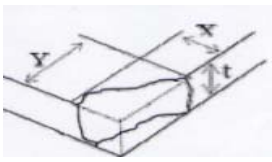
19.Block Diagram

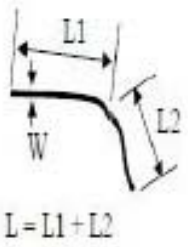


20. PartA/PartB specification

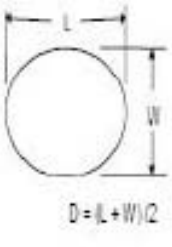


21. Point and line standard

Shipment Inspection Standard						
Equipment：Electrical test fixture, Point gauge						
Outline dimension	36.3(H)×71.82(V) ×0.9(D)	Unit：㎜	Part-A	Active area	Part-B	Border area
Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle
	19℃～25℃	55%±5%RH	800～1300Lux	300 ㎜	35Sec	
Defect type	Inspection method	Standard		Part-A		Part-B
Spot	Electric Display	D≤0.25 ㎜		Ignore		Ignore
		0.25 ㎜＜D≤0.4 ㎜		N≤4		Ignore
		D＞0.4 ㎜		Not Allow		Ignore
Display unwork	Electric Display	Not Allow		Not Allow		Ignore
Display error	Electric Display	Not Allow		Not Allow		Ignore
Scratch or line defect(include dirt)	Visual/Film card	L≤2 ㎜,W≤0.2 ㎜		Ignore		Ignore
		2.0mm＜L≤5.0mm,0.2＜W≤ 0.3mm,		N≤2		Ignore
		L＞5 ㎜,W＞0.3 ㎜		Not Allow		Ignore
PS Bubble	Visual/Film card	D≤0.2mm		Ignore		Ignore
		0.2mm≤D≤0.35mm		N≤4		Ignore
		D＞0.35 mm		Not Allow		Ignore
Corner /Edge chipping	Visual/Film card	X≤6mm,Y≤0.4mm, Do not affect the electrode circuit (Edge chipping), X≤1mm,Y≤1mm, Do not affect the electrode circuit((Corner chipping),ignore				
		 				
Remark	1. Appearance defect should not cause electrical defects					
	2. Appearance defects should not cause dimensional accuracy problems					
	L=long W=wide D=point size N=Defects NO					



Line Defect



Spot Defect

L=long W=wide D=point size

22.Barcode

22.1 label appearance

ABBBBBBBCC
DDDEEEFGGG

22.2 QR scanned information（Total 28 code number+ 2 blank spaces）

A BBBBBBB CC □ DDD EEE F GGG □ H III JJ KK
① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑪

① A——The factory code
② BBBBBBB——Module name of EPD
③ CC——Production line
④ DDD——Date of production
⑤ EEE——Production lot
⑥ F——Separator
⑦ GGG——FPL Lot
⑧ H——Product status
⑨ III——TFT、PS、EC.
⑩ JJ——IC
⑪ KK——Serial NO.
□ blank spaces

23. Packing

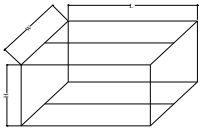
Packing Spec

Sheet No :

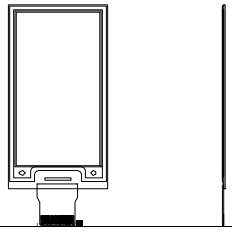
HOLITECH	Part No	HINK-E0266A**	DATE	2020.07.22	VER	A0	Page	1-1

一, Package Type: Box

Box No	Holitech shipping box
Box size	515*322*170
Containment	288PCS

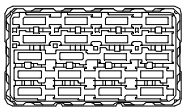


PRODUCT DRAWING

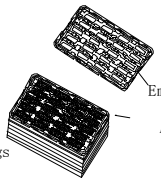


二, Inside package type:Plastic Tray unit: mm

Plastic Tray	465*280*15	13 pcs
Anti-static foil bags	700*530*0.1	1 pcs
EPE(inside)	408.86*231.5*2	12 pcs
EPE(Up-Down)	485*145*10	2 pcs
EPE(Left-Right)	285*480*10	2 pcs
EPE(Front-back)	310*145*10	2 pcs
Chip board	500*306*5	2 pcs
Quantity/tray	24 pcs	
Tray number/sheet	12+1 Sheets	
Box	1	

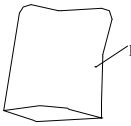


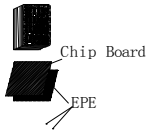
Step 1:
Material: Tray, EPE
Put the product in to the tray and keep the dispaly side up. Then put anti-static EPE in to each holes.

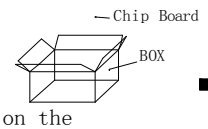


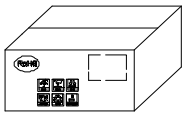
Step 2:
1) Must keep the angle 180 degree placed between the neighboring Plastic trays.
2) There are 12 layers product, total 24*12=288 pcs。
3) An empty Plastic tray intersects put on the top of the plastic trays.

Step 3:
1) In each case, put 2 bags of desiccant. then seal the trays with adhesive tapes.
2) Put the trays into foil bags.
3) heat seal the foil bags.









Step 4:
1)First put a chip board on the buttom of the box, then placed the down EPE, the left - right and front -back EPE.
2) Placed the sealed products into the box.
3) The last placed the up EPE on the top of the trays, and place a chip board on it.

Step 5:
1) Seal the box with adhensive tapes 。
2) Paste the lable onto the exterior box, and the lable can't cover the safety , transfer and RoSH sign。

Design	Z.Z.Q	Approve	H.Z.P	Confirm	X.X.M
Date	2020.07.22	Date	2020.07.22	Date	2020.07.22