Specification For HINK 2.7''EPD

Model NO.: HINK-E027A15

Product VER:A0

Customer Approval

Customer	
Approval By	
Date Of Approval	

It will be agreed by the receiver,if not sign back the Specification within 15days.

Prepared By	Checked By	Approval By
Daisy Zhu	Xiao zhongping Zhou yufeng Zhu shengyuan	Hu ziping

CONTENTS

Version	Content	Date	Producer
A0	New release	20120/03/06	Daisy Zhu

1. General Description

HINK-E027A15 is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design. The 2.7" active area contains 176×264 pixels, and has 1-bit B/W/R full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC. SRAM.LUT, VCOM and border are supplied with each panel.

2. Features

- 176×264 pixels display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C signal master interface to read external temperature sensor/built-in temperature sensor

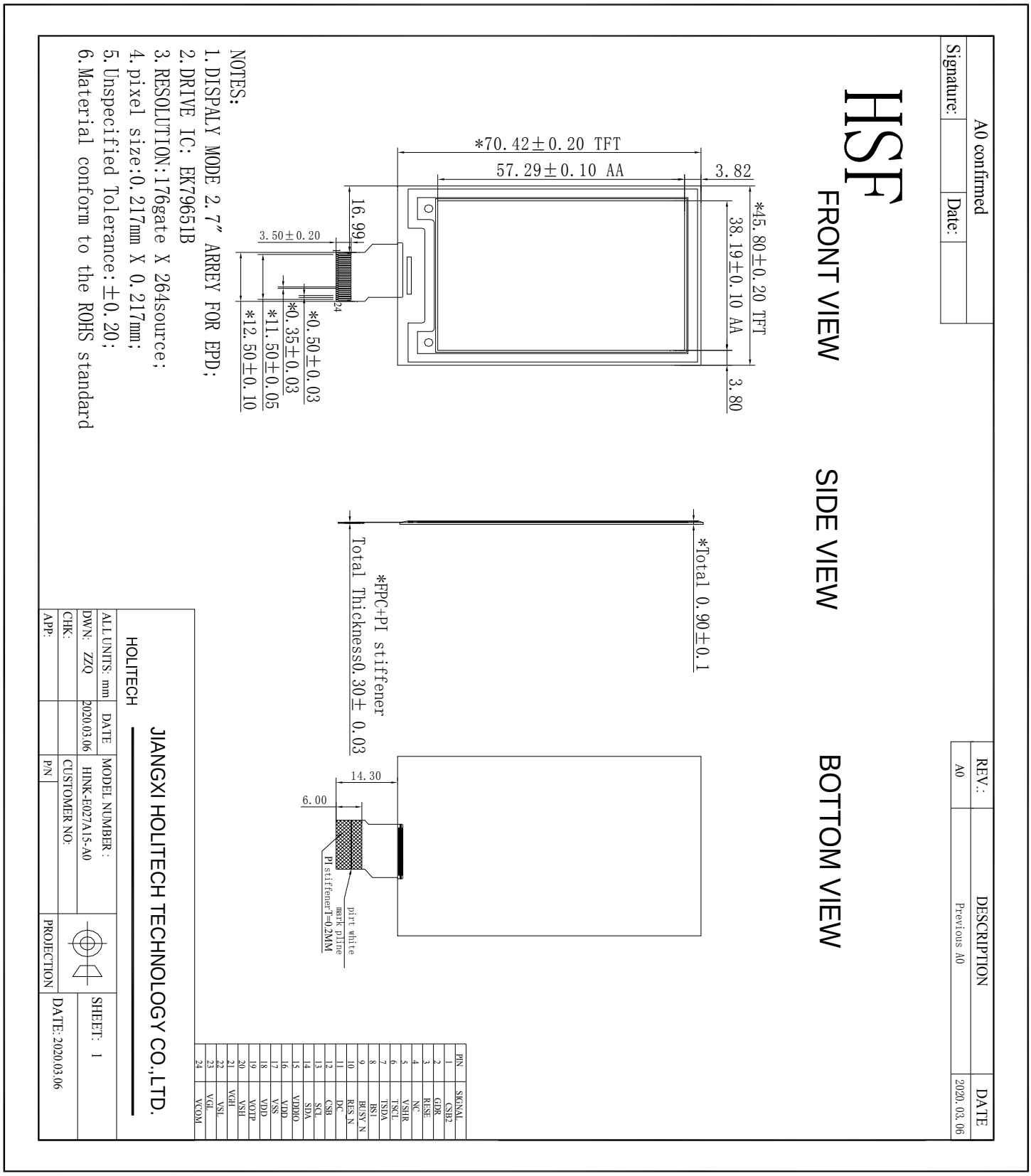
3. Application

Electronic Shelf Label System

4. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.7	Inch	
Display Resolution	176(H)×264(V)	Pixel	Dpi:117
Active Area	38.19(H)×57.29(V)	mm	
Pixel Pitch	0.217×0.217	mm	
Pixel Configuration	Rectangle		
Outline Dimension	45.8(H)×70.42(V) ×0.9(D)	mm	**Without masking film**
Weight	5.0±0.2	g	

5. Mechanical Drawing of EPD module



6. Input/Output Terminals

Pin #	Single	Description	Remark
1	NC	No connection and do not connect with other NC pins	Keep Open
2	GDR	N-Channel MOSFET Gate Drive Control	
3	RESE	Current Sense Input for the Control Loop	
4	NC	No connection and do not connect with other NC pins e	Keep Open
5	VSHR	Positive source voltage for Red	
6	TSCL	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I2C Interface to digital temperature sensor Date pin	
8	BS	Bus selection pin	Note 6-5
9	BUSY N	Busy state output pin	Note 6-4
10	RST N	Reset	Note 6-3
11	DC	Data /Command control pin	Note 6-2
12	CSB	Chip Select input pin	Note 6-1
13	SCL	serial clock pin (SPI)	
14	SDA	serial data pin (SPI)	
15	VDDIO	IO voltage supply	
16	VDD	Digital/Analog power.	
17	VSS	Digital ground	
18	VDD 1.8V	1.8V voltage input &output	
19	VOTP	OTP program power (7.5V)	
20	VSH	Positive Source driving voltage	
21	VGH	Power Supply pin for Positive Gate driving voltage and VSH	
22	VSL	Negative Source driving voltage	
23	VGL	Power Supply pin for Negative Gate driving voltage, VCOM and VSL	
24	VCOM	VCOM driving voltage	

Note 6-1: This pin (CSB) is the chip select input connecting to the MCU. The chip is enabled for MCU communication: only when CSB is pulled LOW.

Note 6-2: This pin (DC) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Note 6-3: This pin (RST_N) is reset signal input. The Reset is active low.

Note 6-4: This pin (BUSY_N) is Busy state output pin. When Busy_N is High the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy_N pin High when the driver IC is working such as:

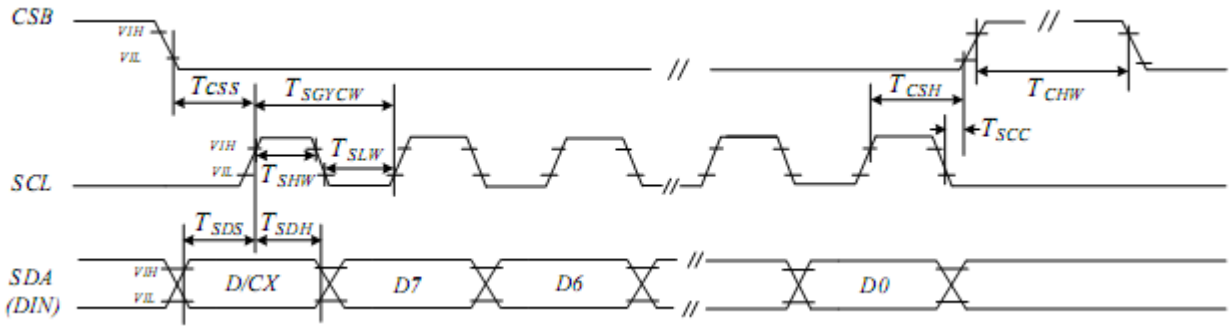
- Outputting display waveform; or
- Communicating with digital temperature sensor

Note 6-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is "Low", 4-line SPI is selected. When it is "High", 3-line SPI (9 bits SPI) is selected.

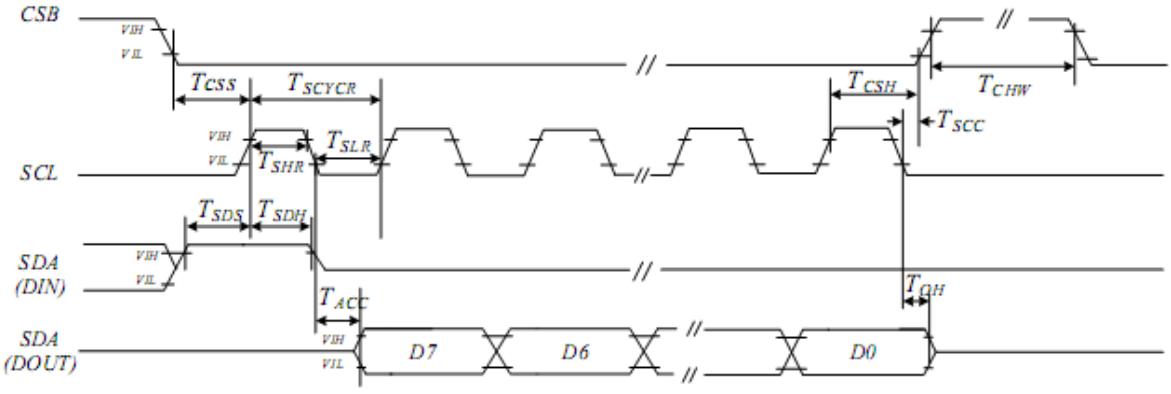
7.SPI COMMAND DESCRIPTION

7.1 "3-Wire" Serial Port Interface

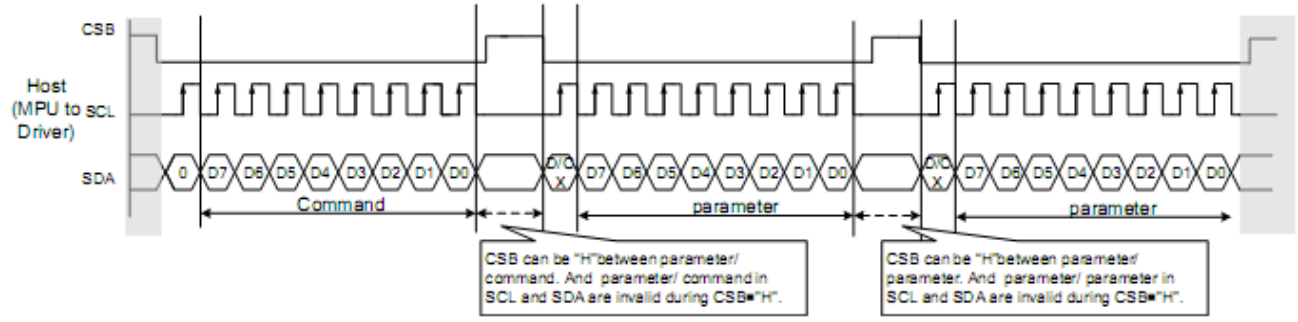
JD79651 use the 3-wire serial port as communication interface for all the function and command setting.
3-Wire communication can be bi-directional controlled by the "R/W" bit in address field. JD79651 3-Wire engine act as a "slave mode" for all the time, and will not issue any command to the 3-Wire bus itself.
Under read mode, 3-Wire engine will return the data during "Data phase". The returned data should be latched at the rising edge of SCL by external controller. Data in the "Hi-Z phase" will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under "Hi-Z phase" and "Data phase".



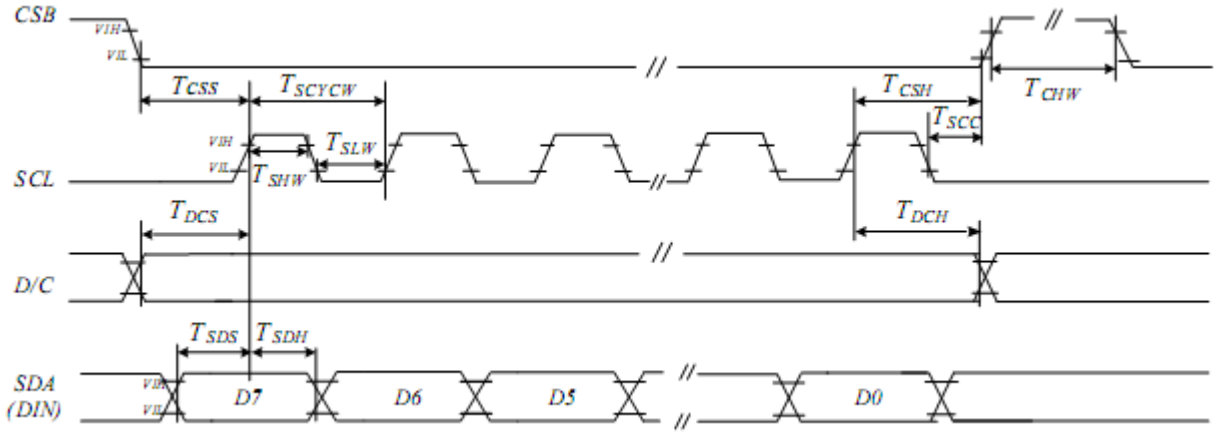
3 pin serial interface characteristics (write mode)



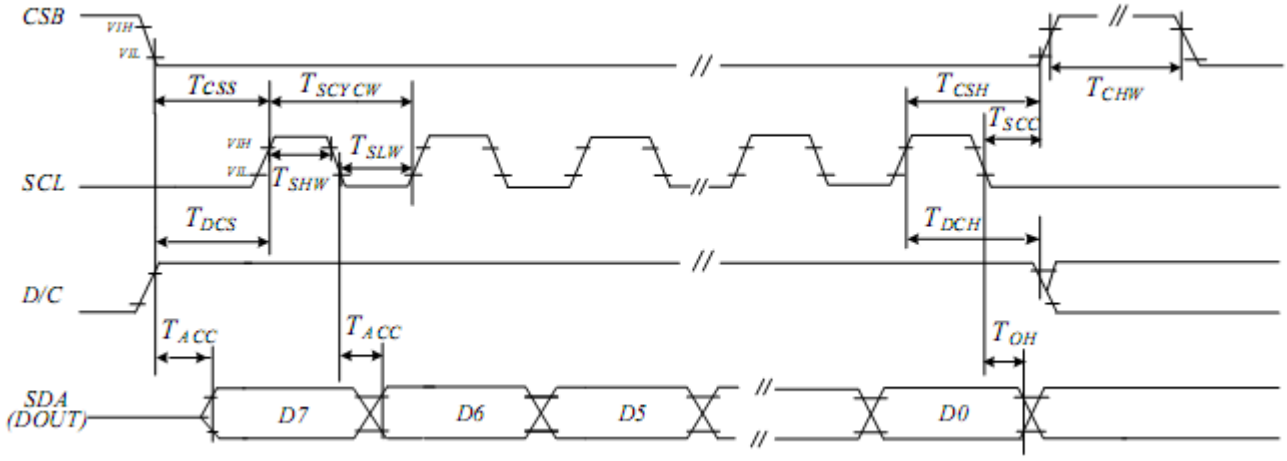
3 pin serial interface characteristics (read mode)



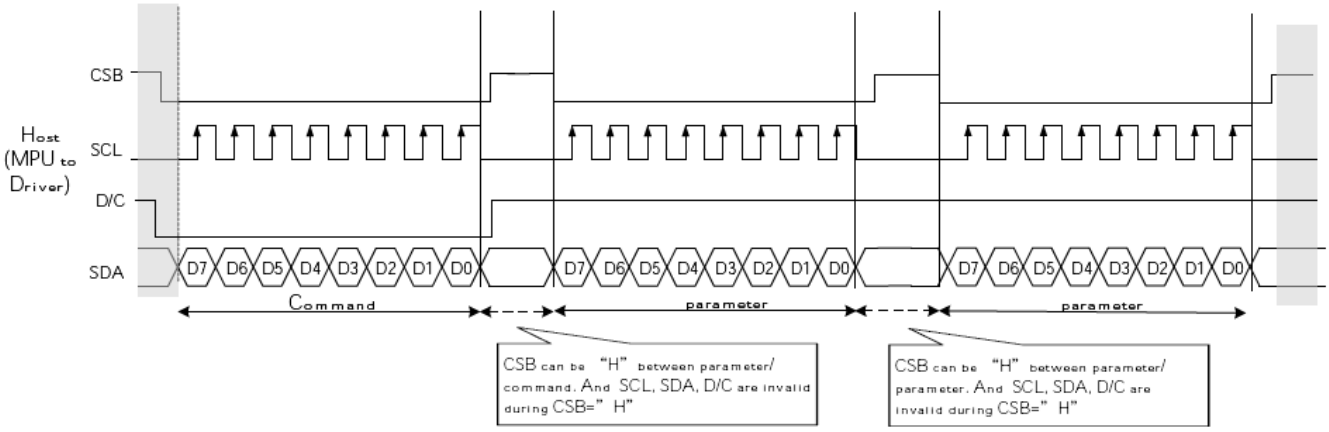
7.2 "4-Wire" Serial Port Interface



4 pin serial interface characteristics(write mode)



4 pin serial interface characteristics(read mode)


Host (MPU to Driver)
CSB
SCL
D/C
SDA
D7 D6 D5 D4 D3 D2 D1 D0
Command
parameter
parameter
CSB can be "H" between parameter/ command. And SCL, SDA, D/C are invalid during CSB=" H"
CSB can be "H" between parameter/ parameter. And SCL, SDA, D/C are invalid during CSB=" H"

8. COMMAND TABLE

8-1Register Table

Following table list all the SPI control registers and bit name definition for EK79686. Refer to the next section for detail register function description.

Address	command	Bit										
		R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
R00H	Panel setting (PSR)	W	0	0	0	0	0	0	0	0	0	00H
		W	1	RES[1]	RES[0]	REG_EN	BWR	UD	SHL	SHD_N	RST_N	8h
R01H	Power setting (PWR)	W	0	0	0	0	0	0	0	0	1	01H
		W	1	-	-	-	-	-	-	VDS_EN	VDG_EN	03H
		W	1			-	-	VCOM-HV	VCOM-LV[2]	VCOM-LV[1]	VCOM-LV[0]	00H
		W	1			VSH [5]	VSH [4]	VSH [3]	VSH [2]	VSH [1]	VSH [0]	26H
		W	1			VSL [5]	VSL [4]	VSL [3]	VSL [2]	VSL [1]	VSL [0]	26H
		W	1		VSHR [6]	VSHR [5]	VSHR [4]	VSHR [3]	VSHR [2]	VSHR [1]	VSHR [0]	06H
R02H	Power OFF(POF)	W	0	0	0	0	0	0	0	1	0	02H
R03H	Power off Sequence Setting(PFS)	W	0	0	0	0	0	0	0	1	0	03H
		W	1	-	-	T_VDS_OFF[1]	T_VDS_OFF [0]					00H
R04H	Power ON (PON)	W	0	0	0	0	0	0	1	0	0	04H
R05H	Power ON Measure (PMES)	W	0	0	0	0	0	0	1	0	1	05H
R06H	Booster Soft Start (BTST)	W	0	0	0	0	0	0	1	1	0	06H
		W	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0	17h
		W	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0	17h
		W	1	-		BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0	17h
R07H	Deep Sleep(DSLP)	W	0	0	0	0	0	0	1	1	1	07H
		W	1	1	0	1	0	0	1	0	1	A5h
R10H	Data Start transmission 1 (DTM1)	W	0	0	0	0	1	0	0	0	0	10H
		W	1	#	#	#	#	#	#	#	#	00H
R11H	Data Stop (DSP)	W	0	0	0	0	1	0	0	0	1	11H
		R	1	Data_flag	-	-	-	-	-	-	-	-
R12H	Display Refresh (DRF)	W	0	0	0	0	1	0	0	1	0	12H
R13H	Data Start transmission 2(DTM2)	W	0	0	0	0	1	0	0	1	1	13H
		W	1	#	#	#	#	#	#	#	#	00h
R14H	Partial Data Start transmission 1 (PDTM1)	W	0	0	0	0	1	0	1	0	0	14H
		W	1	#	#	#	#	#	#	#	#	00h
R15H	Partial Data Start transmission 2 (PDTM2)	W	0	0	0	0	1	0	1	0	1	15H
		W	1	#	#	#	#	#	#	#	#	00h
R16H	Partial Display Refresh(PDRF)	W	0	0	0	0	1	0	1	1	0	16H
		W	1	#	#	#	#	#	#	#	#	00h
R20H	LUT for VCOM (LUT1)	W	0	0	0	1	0	0	0	0	0	20H
		W	1	#	#	#	#	#	#	#	#	00h
R21H	White to	W	0	0	0	1	0	0	0	0	1	21H

	White LUT (LUTWW)	W	1	#	#	#	#	#	#	#	#	00h
R22H	Black to White LUT (LUTBW/LUTR)	W	0	0	0	1	0	0	0	1	0	22H
		W	1	#	#	#	#	#	#	#	#	00h
R23H	White to Black LUT (LUTWB/LUTW)	W	0	0	0	1	0	0	0	1	1	23H
		W	1	#	#	#	#	#	#	#	#	00h
R24H	Black to Black LUT(LUTBB/LUTB)	W	0	0	0	1	0	0	1	0	0	24H
		W	1	#	#	#	#	#	#	#	#	00h
R25H	LUTC option	W	0	0	0	1	0	0	1	0	1	25H
		W	1							XON [9:8]		00h
		W	1	XON [7:0]								00h
		W	1							VCOMH[9:8]		00h
		W	1	VCOMH[7:0]								00h
R26H	Set Vcom/Red states	W	0	0	0	1	0	0	1	1	0	26H
		W	1	0	0			vcom_stg_sel[1:0]		b2w_stg_sel[1:0]		00h
R30H	OSC control (OSC)	W	0	0	0	1	1	0	0	0	0	30H
		W	1	-		M[2:0]			N[2:0]			3Ah
R40H	Temperature Sensor Command (TSC)	W	0	0	1	0	0	0	0	0	0	40H
		R	1	D10/TS[7]	D9/TS[6]	D8/TS[8]	D7/TS[7]	D6/TS[9]	D5/TS[8]	D4/TS[10]	D3/TS[9]	--
		R	1	D2	D1	D0	-	-	-	-	-	--
R41H	Temperature Sensor Calibration (TSE)	W	0	0	1	0	0	0	0	0	1	41H
		W	1	TSE	-	-	-	TO[3]	TO[2]	TO[1]	TO[0]	00h
R42H	Temperature Sensor Write (TSW)	W	0	0	1	0	0	0	0	1	0	42H
		W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
		W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
		W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h
R43H	Temperature Sensor Read (TSR)	W	0	0	1	0	0	0	0	1	1	43H
		R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	-
		R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	-
R50H	VCOM and DATA interval setting (CDI)	W	0	0	1	0	1	0	0	0	0	50H
		W	1	VBD[1]	VBD[0]	DDX[1]	DDX[0]	CDI[3]	CDI[2]	CDI[1]	CDI[0]	D7h
R51H	Lower Power Detection (LPD)	W	0	0	1	0	1	0	0	0	1	51H
		R	1	-	-	-	-	-	-	-	LPD	-
R60H	TCON setting(TCON)	W	0	0	1	1	0	0	0	0	0	60H
		W	1	S2G[3]	S2G[2]	S2G[1]-	S2G[0]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	22h
R61H	Resolution setting (TRES)	W	0	0	1	1	0	0	0	0	1	61H
		W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	-	-	-	00H
		W	1	-	-	-	-	-	-	-	VRES(8)	00H
		W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00H
R62H	Source & gate start setting	W	0	0	1	1	0	0	0	1	0	62H
		W	1	S_start(7)	S_start(6)	S_start(5)	S_start(4)	S_start(3)	-	-	-	00H
		W	1				gscan				G_start [8]	00H
		W	1	G_start (7)	G_start (6)	G_start (5)	G_start (4)	G_start (3)	G_start (2)	G_start (1)	G_start (0)	00H
R70H	REVISION (REV)	W	0	0	1	1	1	0	0	0	0	70H
		R	1	REV[7]	REV[6]	REV[5]	REV[4]	REV[3]	REV[2]	REV[1]	REV[0]	-

		R	1	REV[15]	REV[14]	REV[13]	REV[12]	REV[11]	REV[10]	REV[9]	REV[8]	-
R71H	Status register(FLG)	W	0	0	1	1	1	0	0	0	1	71H
		R	1	-	PTL_flag	I2C_ERR	I2C_BUSYN	Data_flag	PON	POF	BUSY_N	-
R80H	Auto Measure VcomMeasure Vcom(AMV)	W	0	1	0	0	0	0	0	0	0	80H
		W	1	-	-	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMV	10H
R81H	Vcom Value (VV)	W	0	1	0	0		0	0	0	1	81H
		R	1	-	-	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	-
R82H	Vcom_DC Setting register(VDCS)	W	0	1	0	0	0	0	0	1	0	82H
		W	1	-	-	VCDS[5]	VCDS[4]	VCDS[3]	VCDS[2]	VCDS[1]	VCDS[0]	00H
RA0H	Program Mode(PGM)	W	0	1	0	1	0	0	0	0	0	A0H
		W	1	1	0	1	0	0	1	0	1	A5h
RA1H	Active program(APG)	W	0	1	0	1	0	0	0	1	0	A1H
RA2H	Read OTP Data(ROTP)	W	0	1	0	1	0	0	0	1	0	A2H
		R	1	#	#	#	#	#	#	#	#	-
RE0H	CASCADE setting(CCSET)	W	0	1	1	1	0	0	0	0	0	E0H
		W	1	-	-	-	-	Cce-sel	Cce-lr	TSFLX	CCEIN	00H
RE5H	Force Temperature	W	0	1	1	1	0	0	1	0	1	E5H
		W	1	TS_SET[7]	TS_SET[6]	TS_SET[5]	TS_SET[4]	TS_SET[3]	TS_SET[2]	TS_SET[1]	TS_SET[0]	00h
RE6H	LVD voltage Select	W	0	1	1	1	0	0	1	1	0	E6H
		W	1	-	-	-	-	-	-	LVD_SEL0]	LVD_SEL[0]	03h
RE7H	Panel Break Check	W	0	1	1	1	0	0	1	1	1	E7H
		R	1	-	-	-	-	-	-	-	PSTA	-
RE8H	Power saving	W	0	1	1	1	0	1	0	0	0	E8H
		W	1	VCOM_W[3]	VCOM_W[2]	VCOM_W[1]	VCOM_W[0]	SD_W[3]	SD_W[2]	SD_W[1]	SD_W[0]	00h
RE9H	AUTO sequence	W	0	1	1	1	0	1	0	0	1	E9H
		W	1	1	0	1	0	0	1	0	1	00h
REFH	Checksum program toOTP	W	0	1	1	1	0	1	1	1	11	EFH
RF0H	Remap LUT	W	0	1	1	1	1	0	0	0	0	F0H
		W	1	-	-	-	Bkup-lut-2-en	Rmp2-table-sel[3]	Rmp2-table-sel[2]	Rmp2-table-sel[1]	Rmp2-table-sel[0]	1Fh
		W	1	-	-	-	Bkup-lut-1-en	Rmp1-table-sel[3]	Rmp1-table-sel[2]	Rmp1-table-sel[1]	Rmp1-table-sel[0]	1Fh
RF1H	Set OTP program	W	0	1	1	1	1	0	0	0	1	F1H
		W	1	-	-	-	-	-	-	LUT_bank	reg_bank	03h
RF2H	Read checksum	W	0	1	1	1	1	0	0	1	0	F2H
		R	1	#	#	#	#	#	#	#	#	-
RF3H	Calculate Checksum	W	0	1	1	1	1	0	0	1	1	F3H

8-2 Register Description

8-2.1R00H (PSR): Panel setting Register

R00H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PSR	W	0	0	0	0	0	0	0	0	0	00H
1st Parameter	W	1	RES[1]	RES[0]	REG_EN	BWR	UD	SHL	SHD_N	RST_N	8Fh

NOTE: "-" Don't care, can be set to VDD or GND level

Description -The command defines as :

Bit	Name	Description
0	RST_N	RST_N function 1 : no effect. (default) 0: Booster OFF, Register data are set to their default values, and SEG/BG/VCOM:floating
1	SHD_N	SHD_N function 0 : Booster OFF, register data are kept, and SEG/BG/VCOM are kept floating. 1 : Booster on. (default)
2	SHL	SHL function 0: Shift left; First data=Sn →Sn-1 → ⋯→S2 →Last data=S1. 1: Shift right: First data=S1→ S2 → ⋯→Sn-1 → Last data=Sn. (default)
3	UD	UD function 0:Scan down; First line=Gn→Gn-1 →⋯→ G2 → Last line=G1. 1:Scan up; First line=G1 →G2 →⋯→Gn-1 →Last line=Gn. (default)
4	BWR	Color selection setting 0: Pixel with B/W/Red. Run both LU1 and LU2. (default) 1: Pixel with B/W. Run LU1 only
5	REG_EN	LUT selection setting 0 : Using LUT from OTP(default) 1 : Using LUT from register
7-6	RES[1,0]	Resolution setting 00: Display resolution is 96x230 01: Display resolution is 96x252 10: Display resolution is 128x296 (default) 11: Display resolution is 160x296

Notes

1. When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD turn off. SD output and VCOM will base on previous condition and keep floating.
2. When RST_N become low, driver will reset. All register will reset to default value. All of the driver's functions will disable. SD output and VCOM will base on previous condition and keep floating.

8-2-2 R01H (PWR): Power setting Register

R01H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWR	W	0	0	0	0	0	0	0	0	1	01h
1st Parameter	W	1	-	-	-	-	-	-	VDS_EN	VDS_EN	03h
2nd Parameter	W	1	-	-	-	-	VCOM_HV	VGHL_LV [2]	VGHL_LV [1]	VGHL_LV [0]	00h
3rd Parameter	W	1	-	-	VSH [5]	VSH [4]	VSH [3]	VSH [2]	VSH [1]	VSH [0]	26h
4th Parameter	W	1	-	-	VSL [5]	VSL [4]	VSL [3]	VSL [2]	VSL [1]	VSL [0]	26h
5th Parameter	W	1	-	VSHR [6]	VSHR [5]	VSHR [4]	VSHR [3]	VSHR [2]	VSHR [1]	VSHR [0]	06h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :E4

1st Parameter:

Bit	Name	Description
0	VDG_EN	Source power selection. 0 : External source power from VSH/VSL/VSHR pins. 1 : Internal DC/DC function for generate VSH/VSL/VSHR (default)
1	VDS_EN	Source power selection. 0 : External source power from VSH/VSL/VSHR pins. 1 : Internal DC/DC function for generate VSH/VSL/VSHR (default)

2nd Parameter:

Bit	Name	Description
2-0	VGHL_LV	VGHL_LV Voltage Level. 000: VGH=20 v, VGL=-20v 001: VGH=19 v, VGL=-19v 010: VGH=18 v, VGL=-18v 011: VGH=17 v, VGL=-17v 100: VGH=16 v, VGL=-16v 101: VGH=15 v, VGL=-15v 110: VGH=14 v, VGL=-14v 111: VGH=13 v, VGL=-13v
3	VCOM_HV	VCOM Voltage Level 0: VCOMH=VSH+VCOMDC,VCOML=VSL+VCOMDC(default) 1: VCOMH=VGH, VCOML=VGL

3rd Parameter: Internal VSH power selection for B/W LUT.

Bit	Name	Description
5-0	VSH	Internal VSH power selection.

VSH[5:0]		Voltage(V)	VSH[5:0]		Voltage(V)
000000	00h	2.4	100000	20h	8.8
000001	01h	2.6	100001	21h	9
000010	02h	2.8	100010	22h	9.2
000011	03h	3	100011	23h	9.4
000100	04h	3.2	100100	24h	9.6
000101	05h	3.4	100101	25h	9.8
000110	06h	3.6	100110	26h	10
000111	07h	3.8	100111	27h	10.2
001000	08h	4	101000	28h	10.4
001001	09h	4.2	101001	29h	10.6
001010	0Ah	4.4	101010	2Ah	10.8
001011	0Bh	4.6	101011	2Bh	11
001100	0Ch	4.8	101100	2Ch	11.2
001101	0Dh	5	101101	2Dh	11.4
001110	0Eh	5.2	101110	2Eh	11.6
001111	0Fh	5.4	101111	2Fh	11.8
010000	10h	5.6	110000	30h	12
010001	11h	5.8	110001	31h	12.2
010010	12h	6	110010	32h	12.4
010011	13h	6.2	110011	33h	12.6
010100	14h	6.4	110100	34h	12.8
010101	15h	6.6	110101	35h	13
010110	16h	6.8	110110	36h	13.2
010111	17h	7	110111	37h	13.4
011000	18h	7.2	111000	38h	13.6
011001	19h	7.4	111001	39h	13.8
011010	1Ah	7.6	111010	3Ah	14
011011	1Bh	7.8	111011	3Bh	14.2
011100	1Ch	8	111100	3Ch	14.4
011101	1Dh	8.2	111101	3Dh	14.6
011110	1Eh	8.4	111110	3Eh	14.8
011111	1Fh	8.6	111111	3Fh	15

4th Parameter: Internal VSL power selection for B/W LUT.

Bit	Name	Description
5-0	VSL	Internal VSH power selection.

VSH[5:0]		Voltage(V)	VSH[5:0]		Voltage(V)
000000	00h	-2.4	100000	20h	-8.8
000001	01h	-2.6	100001	21h	-9
000010	02h	-2.8	100010	22h	-9.2
000011	03h	-3	100011	23h	-9.4
000100	04h	-3.2	100100	24h	-9.6
000101	05h	-3.4	100101	25h	-9.8
000110	06h	-3.6	100110	26h	-10
000111	07h	-3.8	100111	27h	-10.2
001000	08h	-4	101000	28h	-10.4
001001	09h	-4.2	101001	29h	-10.6
001010	0Ah	-4.4	101010	2Ah	-10.8
001011	0Bh	-4.6	101011	2Bh	-11
001100	0Ch	-4.8	101100	2Ch	-11.2
001101	0Dh	-5	101101	2Dh	-11.4
001110	0Eh	-5.2	101110	2Eh	-11.6
001111	0Fh	-5.4	101111	2Fh	-11.8
010000	10h	-5.6	110000	30h	-12
010001	11h	-5.8	110001	31h	-12.2
010010	12h	-6	110010	32h	-12.4
010011	13h	-6.2	110011	33h	-12.6
010100	14h	-6.4	110100	34h	-12.8
010101	15h	-6.6	110101	35h	-13
010110	16h	-6.8	110110	36h	-13.2
010111	17h	-7	110111	37h	-13.4
011000	18h	-7.2	111000	38h	-13.6
011001	19h	-7.4	111001	39h	-13.8
011010	1Ah	-7.6	111010	3Ah	-14
011011	1Bh	-7.8	111011	3Bh	-14.2
011100	1Ch	-8	111100	3Ch	-14.4
011101	1Dh	-8.2	111101	3Dh	-14.6
011110	1Eh	-8.4	111110	3Eh	-14.8
011111	1Fh	-8.6	111111	3Fh	-15

5th Parameter: Internal VSHR power selection for Red LUT.

Bit	Name	Description
6-0	VSHR	Internal VSH power selection.

VSH[5:0]		Voltage(V)	VSH[5:0]		Voltage(V)	VSHR[6:0]		Voltage(V)
0000000	00h	2.4	0011101	1Dh	5.3	0111010	3Ah	8.2
0000001	01h	2.5	0011110	1Eh	5.4	0111011	3Bh	8.3
0000010	02h	2.6	0011111	1Fh	5.5	0111100	3Bh	8.4
0000011	03h	2.7	0100000	20h	5.6	0111101	3Dh	8.5
0000100	04h	2.8	0100001	21h	5.7	0111110	3Eh	8.6
0000101	05h	2.9	0100010	22h	5.8	0111111	3Fh	8.7
0000110	06h	3.	0100011	23h	5.9	0111111	40h	8.8
0000111	07h	3.1	0100100	24h	6.0	1000001	41h	8.9
0001000	08h	3.2	0100101	25h	6.1	1000010	42h	9
0001001	09h	3.3	0100110	26h	6.2	1000011	43h	9.1
0001010	0Ah	3.4	0100111	27h	6.3	1000100	44h	9.2
0001011	0Bh	3.5	0101000	28h	6.4	1000101	45h	9.3
0001100	0Ch	3.6	0101001	29h	6.5	1000110	46h	9.4
0001101	0Dh	3.7	0101010	2Ah	6.6	1000111	47h	9.5
0001110	0Eh	3.8	0101011	2Bh	6.7	1001000	48h	9.6
0001111	0Fh	3.9	0101100	2Ch	6.8	1001001	49h	9.7
0010000	10h	4	0101101	2Dh	6.9	1001010	4Ah	9.8
0010001	11h	4.1	0101110	2Eh	7	1001011	4Ah	9.9
0010010	12h	4.2	0101111	2Fh	7.1	1001100	4Ch	10
0010011	13h	4.3	0110000	30h	7.2	1001101	4Dh	10.1
0010100	14h	4.4	0110001	31h	7.3	1001110	4Eh	10.2
0010101	15h	4.5	0110010	32h	7.4	1001110	4Eh	10.3
0010110	16h	4.6	0110011	33h	7.5	1010000	50h	10.4
0010111	17h	4.7	0110100	34h	7.6	1010001	51h	10.5
0011000	18h	4.8	0110101	35h	7.7	1010010	52h	10.6
0011001	19h	4.9	0110110	36h	7.8	1010010	53h	10.7
0011010	1Ah	5	0110111	37h	7.9	1010100	53h	10.8
0011011	1Bh	5.1	0111000	38h	8	1010101	55h	10.9
0011100	1Ch	5.2	0111001	39h	8.1	1010110	56h	11

Note:
1.VSH>VSHR

Restriction	

8.2.3 R02H (POF): Power OFF Command

R02H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
POF	W	0	0	0	0	0	0	0	1	0	02H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ●After power off command, driver will power off base on power off sequence. ●After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N singal will rise from low to high. ●Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. ●SD output and VCOM will keep floating.
Restriction	

8.2.4 R03H (PFS): Power off Sequence Setting Register

R03H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PFS	W	0	0	0	0	0	0	0	1	1	03H
1st Parameter	W	1	-	-	Vsh_off[1]	Vsh_off [0]	Vsl_off[1]	vsl_off[0]	vshr_off[1]	vshr_off [0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : 1st Parameter:		
	Bit	Name	Description
	1-0	vshr_off	00: 5ms. (default) 01: 10ms 10: 20ms 11: 40ms
	3-2	vsl_off	00: 5ms. (default) 01: 10ms 10: 20ms 11: 40ms
	5-4	vsh_off	00: 5ms. (default) 01: 10ms 10: 20ms 11: 40ms
Restriction			

8.2.5 R04H (PON): Power ON Command

R04H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PON	W	0	0	0	0	0	0	1	0	0	04H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ●After power on command, driver will power on base on power on sequence. ●After power on command, BUSY_N signal will drop from high to low. When finishing the power off sequence, BUSY_N signal will rise from low to high.

8.2.6 R05H (PMES): Power ON Measure Command

R05H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PMES	W	0	0	0	0	0	0	1	0	1	05H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■If user wants to read temperature sensor or detect low power in power off mode, user has to send this command. After power on measure command, driver will switch on relevant commend with Low Power detection (R51H) and temperature measurement. (R40H).
Restriction	

8.2.7 R06H (BTST): Booster Soft Start Command

R06H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
BTST	W	0	0	0	0	0	0	1	1	0	06H
1st Parameter	W	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0	17h
2nd Parameter	W	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0	17h
3rd Parameter	W	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0	17h

Description

-The command define as follows:

1st Parameter:

Bit	Name	Description
2-0	Driving strength of phase A	000: period 1
		001: period 2
		010: period 3
		011: period 4
		100: period 5
		101: period 6
		110: period 7
		111: period 8 (default)
5-3		000: Strength 1
		001: Strength 2
		010: Strength 3 (default)
		011: Strength 4
		100: Strength 5
		101: Strength 6
		110: Strength 7
		111: Strength 8
7-6	Soft start period of phase A	00: 10mS (default)
		01: 20mS
		10: 30mS

				11: 40mS	

Description

2nd Parameter:

Bit	Name	Description
2-0	Driving strength of phase B	000: period 1
		001: period 2
		010: period 3
		011: period 4
		100: period 5
		101: period 6
		110: period 7
		111: period 8 (default)
5-3		000: Strength 1
		001: Strength 2
		010: Strength 3 (default)
		011: Strength 4
		100: Strength 5
		101: Strength 6
		110: Strength 7
		111: Strength 8
7-6	Soft start period of phase B	00: 10mS (default)
		01: 20mS
		10: 30mS
		11: 40mS

3rd Parameter:

Bit	Name	Description
2-0	Minimum OFF time setting of GDR in phase C	000: period 1
		001: period 2
		010: period 3
		011: period 4
		100: period 5
		101: period 6
		110: period 7
		111: period 8 (default)
5-3	Driving strength of phase C	000: Strength 1
		001: Strength 2
		010: Strength 3 (default)
		011: Strength 4
		100: Strength 5
		101: Strength 6
		110: Strength 7
		111: Strength 8

Restriction	

8.2.8 R07H (DSLP): Deep Sleep

R07H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSLP	W	0	0	0	0	0	0	1	1	1	07H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset. The only one parameter is a check code, the command would be excited if check code = 0xA5.
Restriction	

8.2.9 R10H (DTM1): Data Start transmission 1 Register

R10H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM1	W	0	0	0	0	1	0	0	0	0	10H
1st Parameter	W	1	KPixel 1	KPixel2	KPixel3	KPixel 4	KPixel5	KPixel6	KPixel 7	KPixel 8	00H
2nd Parameter	W	1									00H
…	W	1									00H
Mth Parameter	W	1	KPixel (n-7)	KPixel(n -6)	KPixel(n -5)	KPixel (n-4)	KPixel(n -3)	KPixel(n-2)	KPixel (n-1)	KPixel (n)	00H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "OLD" data to SRAM. In B/W/Red mode, this command writes "B/W" data to SRAM. In Program mode, this command writes "OTP" data to SRAM for programming.
Restriction	

8.2.10 R11H (DSP): Data Stop Command

R11H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSP	W	0	0	0	0	1	0	0	0	1	11H
1st Parameter	R	1	Data_flag	-	-	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■ While finished the data transmitting, user must send this command to driver and read Data_flag information. 1st Parameter:

	Bit	Name	Description
	7	-	0: Driver didn't receive all the data. 1: Driver has already received all of the one frame data.
	After "Data Start" (10h) or "Data Stop" (11h) commands and when data_flag=1, BUSY_N signal will become "0" and the refreshing of panel starts.		
Restriction	This command only actives when BUSY_N = "1".		

8.2.11 R12H (DRF): Display Refresh Command

R12H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DRF	W	0	0	0	0	1	0	0	1	0	12H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■ While users send this command, driver will refresh display (data/VCOM) base on SRAM data and LUT. After display refresh command, BUSY_N signal will become "0".
Restriction	This command only actives when BUSY_N = "1".

8.2.12 R13H (DTM2): Data Start transmission 2 Register

R13H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM2	W	0	0	0	0	1	0	0	1	1	13H
1st Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00H
2nd Parameter	W	1									00H
……	W	1									00H
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00H

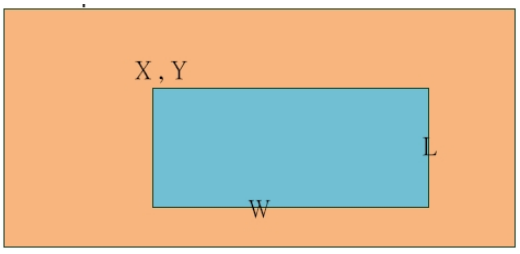
NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "NEW" data to SRAM. In B/W/Red mode, this command writes "RED" data to SRAM.
Restriction	

8.2.13 R14H (PDTM1): Partial Data Start transmission 1 Register

R14H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PDTM1	W	0	0	0	0	1	0	1	0	0	14H
1st Parameter	W	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0	00h
2nd Parameter										Y[8]	00h
3rd Parameter	W	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]	00h
4th Parameter	W	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0	00h
5th Parameter										L[8]	00h
6th Parameter	W	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]	00h
7th Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

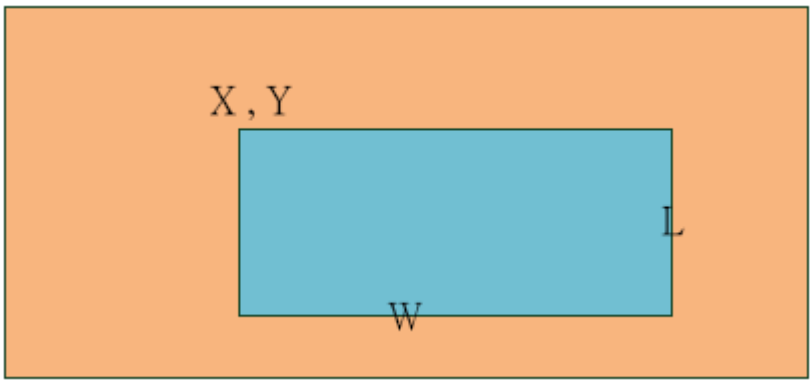
NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows:
	The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "OLD" data to SRAM. In B/W/Red mode, this command writes "B/W" data to SRAM. Partial update location and area  Note: X and W should be the multiple of 8.
Restriction	

8.2.14 R15H (PDTM2): Partial Data Start transmission 2 Register

R15H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PDTM2	W	0	0	0	0	1	0	1	0	0	15H
1st Parameter	W	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0	00h
2nd Parameter										Y[8]	00h
3rd Parameter	W		Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]	00h
4th Parameter	W	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0	00h
5th Parameter										L[8]	00h
6th Parameter	W	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0	00h
7th Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

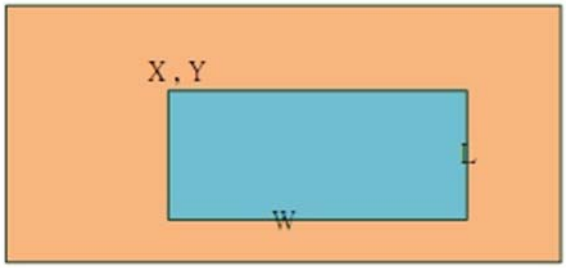
NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "NEW" data to SRAM. In B/W/Red mode, this command writes "RED" data to SRAM. Partial update location and area  Note: X and W should be the multiple of 8.
Restriction	

8.2.15 R16H (PDRF): Partial Display Refresh Command

R16H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PDRF	W	0	0	0	0	1	0	1	1	0	16H
1st Parameter	W	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0	00h
			DFV_EN							Y[8]	00h
3rd Parameter	W	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]	00h
4th Parameter	W	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0	00h
										L[8]	00h
6th Parameter	W	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: While user sent this command, driver will refresh display (data/VCOM) base on SRAM data and LUT. Only the area (X,Y, W, L) would update, the others pixel output would follow VCOM LUT  Note: X and W should be the multiple of 8. DFV_EN: data follow VCOM function on display area. DFV_EN=1: Only effective in B/W mode, if pixel from "New data" SRAM equal to "Old data" SRAM on display area, this pixel output would follow VCOM LUT. DFV_EN=0: Data doesn't follow VCOM LUT.
Restriction	this command only active when BUSY_N = "1".

8.2.16 R20H (LUTC): LUT for Vcom

R20H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTC	W	0	0	0	1	0	0	0	0	0	20H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number [7:0]								00h
5th Parameter	W	1	4th Frame number [7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~13th Parameter …..	W	1	2nd state								00h
	W	1	3rd ~9th state								00h
55th ~60h Parameter	W	1	10th state								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This register is set for VCOM LUT. This command stores VCOM Look-Up Table with 10 states of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat. If BWR=0 (BWR mode), User could choose 7~10 groups by R26H (SET_STG) If BWR=1 (BW mode), only 7 groups are used.	
	define	description
	Level selection [1:0]	00: -VCM_DC 01: VSH+VCM_DC. 10: VSL+VCM_DC. 11: Floating.
	Frame number [7:0]	00000000 :0 frame 00000001: 1 frame … 11111110: 254 frame 11111111: 255 frame
	Repeat numbers [7:0]	00000000 : 0 00000001: 1 … 11111110: 254 11111111: 255
Restriction	- This command only actives when BUSY_N = "1".	

8.2.17 R21H (LUTWW): White to White LUT Register

R21H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTWW	W	0	0	0	1	0	0	0	0	0	21H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number [7:0]								00h
5th Parameter	W	1	4th Frame number [7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~12th Parameter	W	1	2nd state								00h
…..	W	1	3rd ~6th state								00h
37th ~42th Parameter	W	1	7th state								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat.	
	define	description
	Level selection [1:0]	00: GND 01: VSH 10: VSL 11: VSHR
	Frame number [7:0]	00000000 :0 frame 00000001: 1 frame . 11111110: 254 frame 11111111: 255 frame
	Repeat numbers [7:0]	00000000 : 0 time 00000001: 1 time . 11111110: 254 times 11111111: 255 times
Restriction	- This command only actives when BUSY_N = "1".	

8.2.18 R22H (LUTBW/LUTR): Black to White LUT or Red LUT Register

R22H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTBW/LUTR	W	0	0	0	1	0	0	0	1	0	22H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number [7:0]								00h
5th Parameter	W	1	4th Frame number [7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~12th Parameter …..	W	1	2nd state								00h
	W	1	3rd ~9th state								00h
55th ~60th Parameter	W	1	10th state								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command stores White-to-White Look-Up Table with 10 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat. If BWR=0 (BWR mode), User could choose 7~10 groups by R26H (SET_STG) If BWR=1 (BW mode), only 7 groups are used.	
	define	description
	Level selection [1:0]	00: GND 01: VSH 10: VSL 11: VSHR
	Frame number [7:0]	00000000 :0 frame 00000001: 1 frame . 11111110: 254 frame 11111111: 255 frame
	Repeat numbers [7:0]	00000000 : 0 time 00000001: 1 time . 11111110: 254 times 11111111: 255 times
Restriction	- This command only actives when BUSY_N = "1".	

8.2.19 R23H (LUTWB/LUTW): White to Black LUT or White LUT Register

R23H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTBW/LUTR	W	0	0	0	1	0	0	0	1	1	23H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number [7:0]								00h
5th Parameter	W	1	4th Frame number [7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~12th Parameter …..	W	1	2nd state								00h
	W	1	3rd ~6th state								00h
37th ~42th Parameter	W	1	7th state								00h

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	-The command defines as: This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat.	
	define	description
	Level selection [1:0]	00: GND 01: VSH 10: VSL 11: VSHR
	Frame number [7:0]	00000000 :0 frame 00000001: 1 frame . 11111110: 254 frame 11111111: 255 frame
	Repeat numbers [7:0]	00000000 : 0 time 00000001: 1 time . 11111110: 254 times 11111111: 255 times
Restriction	- This command only actives when BUSY_N = “1”.	

8.2.20 R24H (LUTBB/LUTB): Black to Black LUT or Black LUT Register

R24H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTBB/LUTB	W	0	0	0	1	0	0	1	0	0	24H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number [7:0]								00h
5th Parameter	W	1	4th Frame number [7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~12th Parameter …..	W	1	2nd state								00h
	W	1	3rd ~6th state								00h
37th ~42th Parameter	W	1	7th state								00h

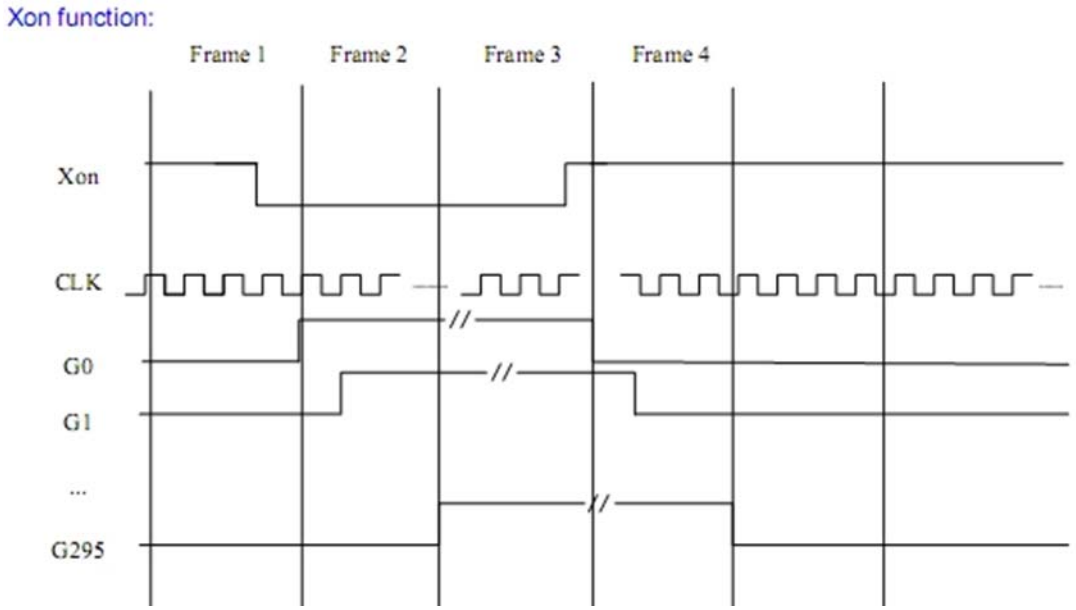
NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat.	
	define	description
	Level selection [1:0]	00: GND 01: VSH 10: VSL 11: VSHR
	Frame number [7:0]	00000000 :0 frame 00000001: 1 frame . 11111110: 254 frame 11111111: 255 frame
	Repeat numbers [7:0]	00000000 : 0 time 00000001: 1 time . 11111110: 254 times 11111111: 255 times
Restriction	- This command only actives when BUSY_N = "1".	

8.2.21 R25H (LUTC Option): LUTC option

R25H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTC option	W	0	0	0	1	0	0	0	0	0	25H
1st Parameter	W	1	XON [9:8]								00h
2nd Parameter	W	1	XON [7:0]								00h
3rd Parameter	W	1	ST_CHV [9:8]								00h
4th Parameter	W	1	ST_CHV [7:0]								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This register is set for VCOM LUT.	
	XON[9:0]	All Gate ON 0000000000: No all gate on. 0000000001: State1 gate power on 1111111111: State1~10 all gate power on
	ST_CHV[9:0]	Control VCOM Power as High 0000000000: No VCOM High voltage 0000000001: State1 VCOM High voltage …. 1111111111: State1~10 VCOM High voltage
		
Restriction	- This command only actives when BUSY_N = "1".	

8.2.22 R26H (SET_STG): Set VCOM/Red States

R26H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
SET_STG	W	0	0	0	1	0	0	1	1	0	26H
1st Parameter	W	1			-	-	vcom_stg_sel[1:0]		b2w_stg_sel[1:0]		00h

Description	This command is used to set VCOM/Red LUT states Function of vcom_stg_sel [1:0]/ b2w_stg_sel[1:0] are shown below Value / Stages 00 / 7 01 / 8 10 / 9 11 / 10 Default is set as 7 stages.
Restriction	These settings are valid for BWR mode.

8.2.23 R30H (OSC): OSC control Register

R30H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
OSC	W	0	0	0	1	1	0	0	0	0	30H
1st Parameter	W	1	-	-	M[2:0]			N[2:0]			3Ah

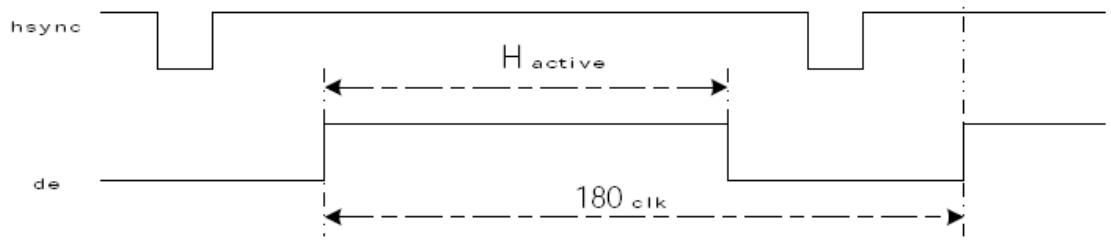
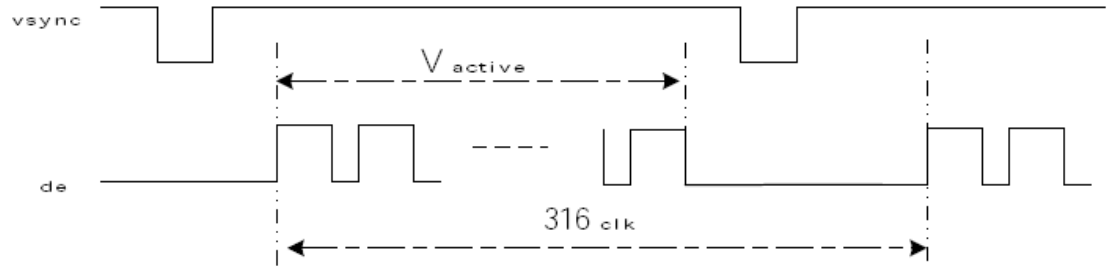
NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

The command controls the OSC clock frequency. The OSC structure must support the following frame rates:

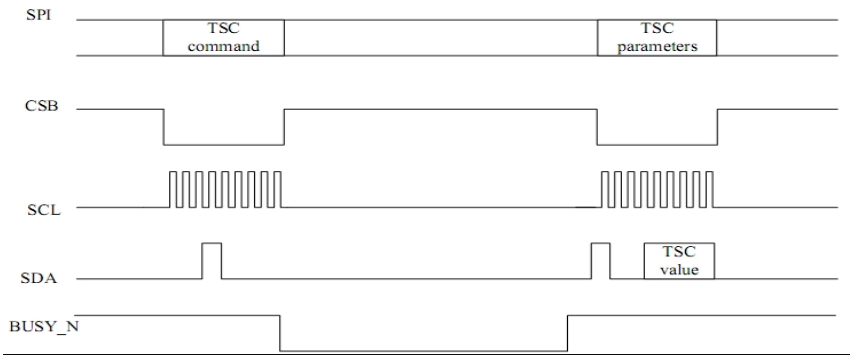
M	N	Frame rate	M	N	Frame rate	M	N	Frame rate	M	N	Frame rate
1	1	29HZ	3	1	86HZ	5	1	150HZ	7	1	200HZ
	2	14HZ		2	43HZ		2	72HZ		2	100HZ
	3	10HZ		3	29HZ		3	48HZ		3	67HZ
	4	7HZ		4	21HZ		4	36HZ		4	50HZ (default)
	5	6HZ		5	17HZ		5	29HZ		5	40HZ
	6	5HZ		6	14HZ		6	24HZ		6	33HZ
	7	4HZ		7	12HZ		7	20HZ		7	29HZ
2	1	57HZ	4	1	114HZ	6	1	171HZ			
	2	29HZ		2	57HZ		2	86HZ			
	3	19HZ		3	38HZ		3	57HZ			
	4	14HZ		4	29HZ		4	43HZ			
	5	11HZ		5	23HZ		5	34HZ			
	6	10HZ		6	19HZ		6	29HZ			
	7	8HZ		7	16HZ		7	24HZ			

remark	 -Vertical 
Restriction	

8.2.24 R40H (TSC): Temperature Sensor Command

R40H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	0	0	40H
1st Parameter	R	1	D10/TS[9]	D9/TS[8]	D8/TS[7]	D7/TS[6]	D6/TS[5]	D5/TS[4]	D4/TS[3]	D3/TS[2]	-
2nd Parameter	R	1	D2/TS[1]	D1/TS[0]	D0	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: This command indicates the temperature value. If R41H(TSE) bit7 set to 0, this command reads internal temperature sensor value. If R41H(TSE) bit7 set to 1, this command reads external (LM75) temperature sensor value 

TS[9:2]/D[10:3]	T (° C)	TS[9:2]/D[10:3]	T (° C)	TS[9:2]/D[10:3]	T (° C)
11100111	-25	00000000	0	00011001	25
11101000	-24	00000001	1	00011010	26
11101001	-23	00000010	2	00011011	27

	11101010	-22	00000011	3	00011100	28
	11101011	-21	00000100	4	00011101	29
	11101100	-20	00000101	5	00011110	30
	11101101	-19	00000110	6	00011111	31
	11101110	-18	00000111	7	00100000	32
	11101111	-17	00001000	8	00100001	33
	11110000	-16	00001001	9	00100010	34
	11110001	-15	00001010	10	00100011	35
	11110010	-14	00001011	11	00100100	36
	11110011	-13	00001100	12	00100101	37
	11110100	-12	00001101	13	00100110	38
	11110101	-11	00001110	14	00100111	39
	11110110	-10	00001111	15	00101000	40
	11110111	-9	00010000	16	00101001	41
	11111000	-8	00010001	17	00101010	42
	11111001	-7	00010010	18	00101011	43
	11111010	-6	00010011	19	00101100	44
	11111011	-5	00010100	20	00101101	45
	11111100	-4	00010101	21	00101110	46
	11111101	-3	00010110	22	00101111	47
	11111110	-2	00010111	23	00110000	48
	11111111	-1	00011000	24	00110001	49

TS[1:0]	T (° C)
00	+0
01	+0.25
10	+0.5
11	+0.75

Restriction	This command only actives after R04H(PON) or R05H(PMES)

8.2.25 R41H (TSE): Temperature Sensor Calibration Register

R41H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSE	W	0	0	1	0	0	0	0	0	1	41H
1st Parameter	W	1	TSE	-	-	-	TO[3]	TO[2]	TO[1]	TO[0]	00h

NOTE: “-” Don’t care, can be set to VDD or GND level

Description

-The command defines as:

This command indicates the driver IC temperature sensor enable and calibration function.

Bit	temperature
2-0	mean temperature offset value
	000:0℃
	001:1℃
	010:2℃
	….
	111:7℃
3	Positive and negative value
	0:”+”
	1:”-“

	7	Internal temperature sensor enable
		0: Internal temperature sensor enable.(default)
		1: Internal temperature sensor disable, using externaltemperature sensor.
	For example: 1100: - 4 degree c 0111: + 7 degree c	
Restriction	This command only actives after R04H(PON) or R05H(PMES)	

8.2.26 R42H (TSW): Temperature Sensor Write Register

R42H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSW	W	0	0	1	0	0	0	0	1	0	42H
1st Parameter	W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
2nd Parameter	W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
3rd Parameter	W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	-The command defines as: This command writes the temperature. 1st Parameter:	
	Bit	temperature
	2-0	Pointer setting
	5-3	User-defined address bits (A2, A1, A0)
	7-6	I2C Write Byte Number 00: 1 byte (head byte only) 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1st parameter) 11: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)
	2nd Parameter:	
	Bit	temperature
	7-0	MSByte of write-data to external temperature sensor
	3nd Parameter:	
	Bit	temperature
	7-0	LSByte of write-data to external temperature sensor
Restriction	This command only actives after R04H(PON) or R05H(PMES)	

8.2.27 R43H (TSR): Temperature Sensor Read Register

R43H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	0	1	43H
1st Parameter	R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	-
2nd Parameter	R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	-

NOTE: “-” Don’t care, can be set to VDD or GND level

Description

-The command defines as:

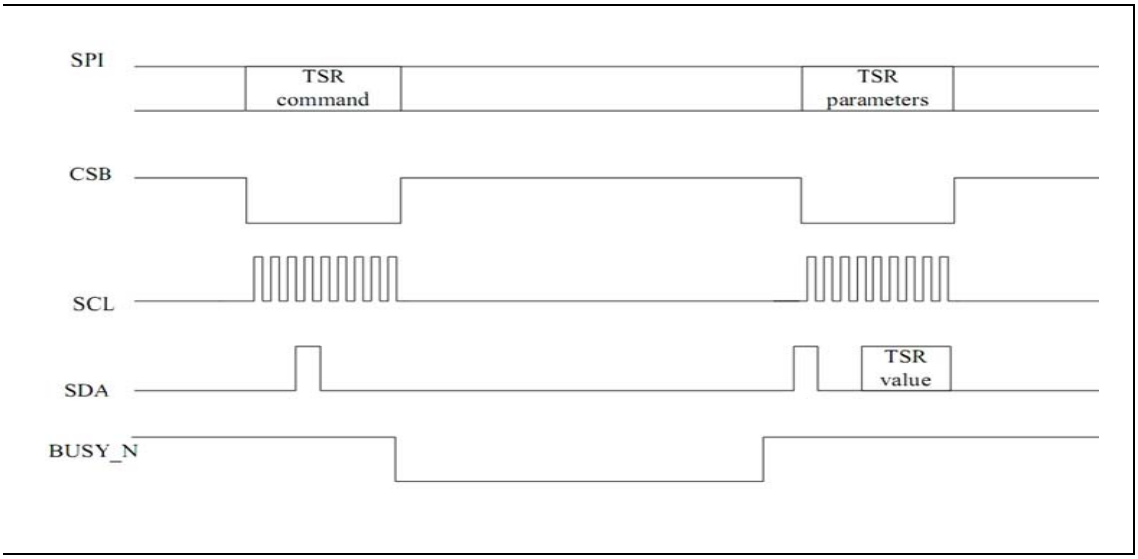
This command reads the temperature sensed by the temperature sensor.

1st Parameter:

Bit	temperature
7-0	MSByte of read-data from external temperature sensor

2nd Parameter:

Bit	temperature
7-0	LSByte of write-data from external temperature sensor



Restriction: This command only actives after R04H(PON) or R05H(PMES)

8.2.28 R50H (CDI): VCOM and DATA interval setting Register

R50H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CDI	W	0	0	1	0	1	0	0	0	0	50H
1st Parameter	W	1	VBD[1]	VBD[0]	DDX[1]	DDX[0]	CDI[3]	CDI[2]	CDI[1]	CDI[0]	D7h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

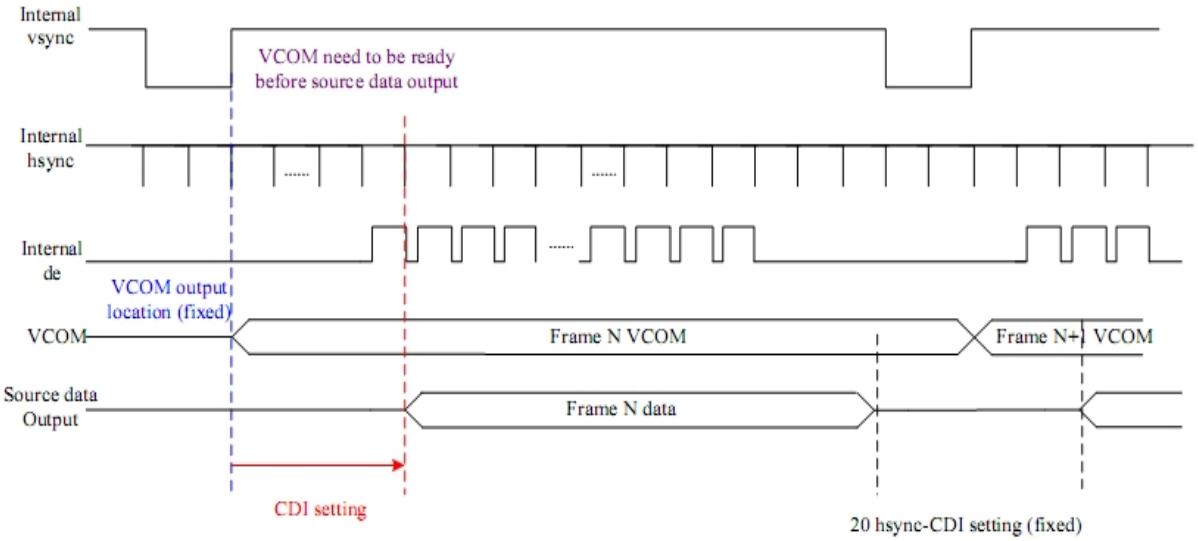
-The command defines as:

1st Parameter:

CDI[1:0]: This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be keep (20hsync).

Bit

3-0	Vcom and data interval 0000: 17 hsync 0001:16 hsync 0010:15 hsync 0011:14 hsync 0100:13 hsync 0101:12 hsync 0110:11 hsync 0111:10 hsync 1000:9 hsync 1001:8 hsync 1010:7 hsync 1011:6 hsync 1100:5 hsync 1101:4 hsync 1110:3 hsync 1111:2 hsync



VBD[1:0] Border data selection.

B/W/Red mode(BWR=0)		
Bit 5-4	Bit7-6	Description
DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTR
	10	LUTW
	11	LUTB
1 (default)	00	LUTB
	01	LUTW
	10	LUTR
	11 (default)	Floating
B/W mode (BWR=1)		

Bit 5-4	Bit7-6	description
DDX[0]	VBD[1:0]	LUT
00	00	Floating
	01	LUTBW (1->0)
	10	LUTWB (0->1)
	11	Floating
01 (default)	00	Floating
	01	LUTWB (1->0)
	10	LUTBW (0->1)
	11	Floating

DDX[1:0]: Data polarity
1. DDX[1] for RED data, DDX[0] for BW data in the B/W/Red mode
2. DDX[0] for B/W mode

B/W/Red mode(BWR=0)

Bit 5-4	Description	
DDX[1:0]	Data (Red/B/W)	LUT
00	00	LUTW
	01	LUTB
	10	LUTR
	11	LUTR
01(default)	00	LUTB
	01	LUTW
	10	LUTR
	11	LUTR
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTB
11	00	LUTR
	01	LUTR
	10	LUTB
	11	LUTW

B/W mode (BWR=1)

Bit 5-4	Description	
DDX[0]	Data (B/W)	LUT
00	00	LUTWW (0->0)
	01	LUTBW(1->0)
	10	LUTWB(0->1)
	11	LUTBB(1->1)
1 (default)	00	LUTBB(0->0)
	01	LUTWB(1->0)
	10	LUTBW(0->1)
	11	LUTWW(1->1)

8.2.29 R51H (LPD): Lower Power Detection Register

R51H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LPD	W	0	0	1	0	1	0	0	0	1	51H
1st Parameter	R	1	-	-	-	-	-	-	-	LPD	-

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	-The command defines as: This command indicates the input power condition. Host can read this data to understand the battery’s condition. When LPD=”1”, system input power is normal. When LPD=”0”, system input power is lower (VDD<2.5v, which could be select in RE6H (LVSEL)). 1st Parameter:

Bit 0	LPD
0	Low power input.
1	Normal status

Restriction	

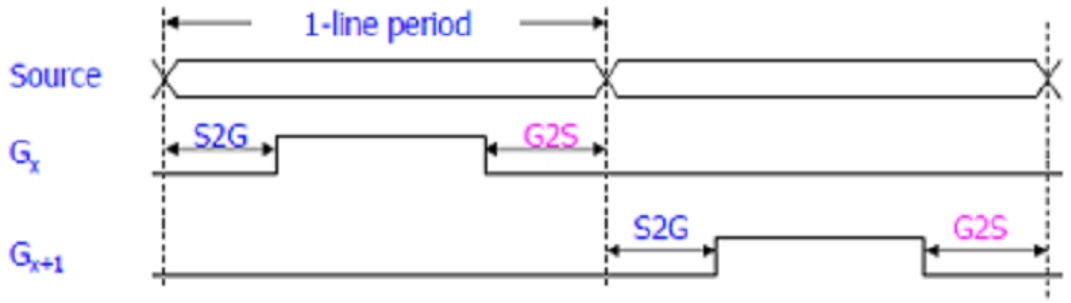
8.2.30 R60H (TCON): TCON setting

R60H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TCON	W	0	0	1	1	0	0	0	0	0	60H
1st Parameter	W	1	S2G[3]	S2G[2]	S2G[1]	S2G[0]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	00h

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	- The command define Non-overlap period of gate and source as below: 1st Parameter:

Bit	Period
S2G[3:0]/G2S[3:0]	0000: 4 clock(default) 0001: 8 clock 0010: 12 clock 0011:16 clock 0100: 20 clock 0101: 24 clock 0110: 28 clock 0111: 32 clock 1000: 36 clock 1001: 40 clock 1010: 44 clock 1011: 48 clock 1100: 52 clock 1101: 56 clock 1110: 60 clock 1111: 64 clock
Period=660ns	

	Period=660ns 
Restriction	

8.2.31 R61H (TRES): Resolution setting

R61H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TRES	W	0	0	1	1	0	0	0	0	1	61H
1st Parameter	W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	-	-	-	00h
2nd Parameter	W	1								-VRES(8)	00h
3rd Parameter	W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	-The command define as follows: When using register: Horizontal display resolution = HRES Vertical display resolution = VRES Channel disable calculation: GD : First G active = G0; LAST active GD= first active +VRES[8:0] -1 SD : First active channel: =S0 ; LAST active SD= first active +HRES[7:3]*8-1 EX :128X272 GD: First G active = G0 LAST active GD= 0+272-1= 271; (G271) SD : First active channel: =S0
Restriction	

8.2.32 R62H (TSGS): Source & gate start setting

R62H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSGS	W	0	0	1	1	0	0	0	1	0	62H
1st Parameter	W	1	S_Start (7)	S_Start (6)	S_Start (5)	S_Start (4)	S_Start (3)				00h
2nd Parameter	W	1				gscan		-	-	-G_start [8]	00h
3rd Parameter	W	1	G_Start (7)	G_Start (6)	G_Start (5)	G_Start (4)	G_Start (3)	G_Start (2)	G_Start (1)	G_Start (0)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: 1.S_Start [8:0] describe which source output line is the first date line 2.G_Start[8:0] describe which gate line is the first scan line 3. gscan :Gate scan select 0: Normal scan 1: Cascade type 2 scan
Restriction	S_Start should be the multiple of 8

8.2.33 R70H (REV): REVISION register

R70H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
REV	W	0	0	1	1	1	0	0	0	0	70H
1st Parameter	R	1	REV[7]	REV[6]	REV[5]	REV[4]	REV[3]	REV[2]	REV[1]	REV[0]	-
2nd Parameter	R	1	REV[15]	REV[14]	REV[13]	REV[12]	REV[11]	REV[10]	REV[9]	REV[8]	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: The LUT_REV is read from OTP address = 0x001.& 0x002
Restriction	- This command only actives when BUSY_N = "1".

8.2.34 R71H (FLG): Status register

R71H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
FLG	W	0	0	1	1	1	0	0	0	1	71H
1st Parameter	R	1			I2C_ERR	II2C_ BUSYN	Data_flag	PON	POF	BUSY_N	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command indicates the IC status. Host can read this data to understand the IC status. 1st Parameter:

Bit	Function
5	I2C master error status
4	I2C master busy status (low active)

	3	Driver has already received one frame data
	2	PON 0: Not in PON mode 1: In PON mode
	1	POF 0: Not in POF mode(default) 1: In POF mode
	0	Driver busy status(low active)
Restriction	User can send this command in any time. It doesn’t have restriction of BUSY_N.	

8.2.35 R80H (AMV): Auto Measure VCOM register

R80H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
AMV	W	0	1	0	0	0	0	0	0	0	80H
1st Parameter	W	1	-	-	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	10H

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	-The command define as follows: This command indicates the IC status. Host can read this data to understand the IC status. 1st Parameter:	
	Bit	Function
	0	AMVE: Auto Measure Vcom Setting 0:Auto measure VCOM disable (default) 1: Auto measure VCOM enable
	1	AMV: Analog signal 0:Get Vcom value from R81h(default) 1:Get Vcom value in analog signal
	2	AMVS: setting for Source output of AMV 0: Source output 0V during Auto Measure VCOM period. (default) 1: Source output VSHR during Auto Measure VCOM period.
	3	XON: setting for all Gate ON of AMVB 0: Gate normally scan during Auto Measure VCOM period. (default) 1: All Gate ON during Auto Measure VCOM period.
	5-4	The sensing time of VCOM detection 00: 3s 01: 5s (default) 10: 8s 11: 10s
Restriction	This command only actives when BUSY_N = “1”.	

8.2.36 R81H (VV): Vcom Value register

R81H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VV	W	0	1	0	0	0	0	0	0	1	81H
1st Parameter	R	1	-	-	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command could get the Vcom value
1st Parameter:

Bit	Function
5-0	Vcom value

VCOM[5:0]		Voltage(V)	VCOM[5:0]		Voltage(V)	VCOM[5:0]		Voltage(V)
000000	00h	-0.1	010100	14h	-1.1	101000	28h	-2.1
000001	01h	-0.15	010101	15h	-1.15	101001	28h	-2.15
000010	02h	-0.2	010110	16h	-1.2	101001	2Ah	-2.2
000011	03h	-0.25	010111	17h	-1.25	101011	2Bh	-2.25
000100	04h	-0.3	011000	18h	-1.3	101100	2Ch	-2.3
000100	05h	-0.35	011001	19h	-1.35	101101	2Dh	-2.35
000110	06h	-0.4	011010	1Ah	-1.4	101110	2Eh	-2.4
000111	07h	-0.45	011011	1Bh	-1.45	101111	2Fh	-2.45
001000	08h	-0.5	011100	1Ch	-1.5	101111	30h	-2.5
001001	09h	-0.55	011101	1Dh	-1.55	110001	31h	-2.55
001010	0Ah	-0.6	011110	1Eh	-1.6	110010	32h	-2.6
001010	0Bh	-0.65	011111	1Fh	-1.65	110011	33h	-2.65
001100	0Ch	-0.7	011111	20h	-1.7	110100	34h	-2.7
001101	0Dh	-0.75	100001	21h	-1.75	110101	35h	-2.75
001110	0Eh	-0.8	100010	22h	-1.8	110110	36h	-2.8
001111	0Fh	-0.85	100011	23h	-1.85	110110	37h	-2.85
010000	10h	-0.9	100100	24h	-1.9	111000	38h	-2.9
010001	10h	-0.95	100100	25h	-1.95	111001	39h	-2.95
010010	12h	-1	100110	26h	-2	111010	3Ah	-3
010010	13h	-1.05	100111	27h	-2.05			

Restriction: This command only actives when BUSY_N = "1".

8.2.37 R82H (VDCS): Vcom_DC Setting register

Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VDCS	W	0	1	0	0	0	0	0	1	0	82H
1st Parameter	W	1	-	-	VCDS[5]	VCDS [4]	VCDS [3]	VCDS [2]	VCDS [1]	VCDS [0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command set the VCOM DC value. Driver will base on this value for VCM_DC.
1st Parameter:

Bit	Function
5-0	VCOM value

VCOM[5:0]		Voltage(V)	VCOM[5:0]		Voltage(V)	VCOM[5:0]		Voltage(V)
000000	00h	-0.1	010100	14h	-1.1	101000	28h	-2.1
000001	01h	-0.15	010101	15h	-1.15	101001	28h	-2.15
000010	02h	-0.2	010110	16h	-1.2	101001	2Ah	-2.2
000011	03h	-0.25	010111	17h	-1.25	101011	2Bh	-2.25
000100	04h	-0.3	011000	18h	-1.3	101100	2Ch	-2.3
000100	05h	-0.35	011001	19h	-1.35	101101	2Dh	-2.35
000110	06h	-0.4	011010	1Ah	-1.4	101110	2Eh	-2.4
000111	07h	-0.45	011011	1Bh	-1.45	101111	2Fh	-2.45
001000	08h	-0.5	011100	1Ch	-1.5	101111	30h	-2.5
001001	09h	-0.55	011101	1Dh	-1.55	110001	31h	-2.55
001010	0Ah	-0.6	011110	1Eh	-1.6	110010	32h	-2.6
001010	0Bh	-0.65	011111	1Fh	-1.65	110011	33h	-2.65
001100	0Ch	-0.7	011111	20h	-1.7	110100	34h	-2.7
001101	0Dh	-0.75	100001	21h	-1.75	110101	35h	-2.75
001110	0Eh	-0.8	100010	22h	-1.8	110110	36h	-2.8
001111	0Fh	-0.85	100011	23h	-1.85	110110	37h	-2.85
010000	10h	-0.9	100100	24h	-1.9	111000	38h	-2.9
010001	10h	-0.95	100100	25h	-1.95	111001	39h	-2.95
010010	12h	-1	100110	26h	-2	111010	3Ah	-3
010010	13h	-1.05	100111	27h	-2.05			

Restriction: This command only actives when BUSY_N = "1".

8.2.38RA0H (PGM): Program Mode

RA0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTIN	W	0	1	0	1	0	0	0	0	0	A0H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is issued, the chip would enter the program mode. The mode would return to standby by hardware reset. The only one parameter is a check code, the command would be executed if check code = 0xA5.
Restriction	This command only actives when BUSY_N = "1".

8.2.39 RA1H (APG): Active Program

RA1H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
APG	W	0	1	0	1	0	0	0	0	1	A1H

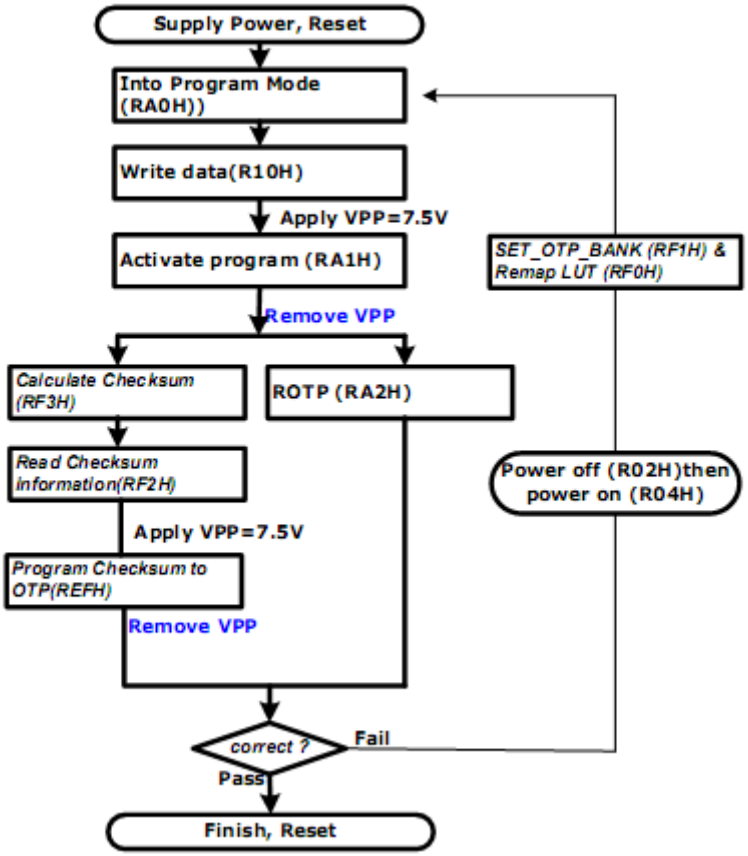
NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is transmitted, the programming state machine would be activated.
Restriction	-- The BUSY flag would fall to 0 while the programming is completed.

8.2.40 RA2H (ROTP): Read OTP Data

RA2H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
ROTP	W	0	1	0	1	0	0	0	1	0	A2H
1st Parameter	R	1	Dummy								-
2nd Parameter	R	1	The data of address 0x000 in the OTP								-
3rd Parameter	R	1	The data of address 0x001 in the OTP								-
4th Parameter	R	1	:								-
5th Parameter	R	1	The data of address (n-1) in the OTP								-
6th~ (m-1)th Parameter	R	1	…								-
mth Parameter	R	1	The data of address (n) in the OTP								-

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	-The command define as follows: The command is used for reading the content of OTP for checking the data of programming. The value of (n) is depending on the amount of programmed data, the max address = 0xFFF.  The sequence of programming OTP
Restriction	This command only actives when BUSY_N = “1”.

8.2.41 RE0H (CCSET): Cascade Setting

RE0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CCSET	W	0	1	1	1	0	0	0	0	0	E0H
1st Parameter	W	1	-	-	-	-	-	-	TSFIX	CCEIN	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	This command is used for cascade.	
	1st Parameter:	
	Bit	
	0	Output clock enable/disable. 0: Output 0V at CL pin. (default) 1: Output clock at CL pin for slave chip.
	1	Let the value of slave's temperature is same as the master's. 0: Temperature value is defined by internal temperature sensor / external LM75. (default) 1: Temperature value is defined by TS_SET [7:0] registers.
Restriction	This command only actives when BUSY_N = "1".	

8.2.42 RE5H (TSSET): Force Temperature

RE5H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSSET	W	0	1	1	1	0	0	1	0	1	E5H
1st Parameter	W	1	TS_SET[7]	TS_SET[6]	TS_SET[5]	TS_SET[4]	TS_SET[3]	TS_SET[2]	TS_SET[1]	TS_SET[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows:
	This command is used to fix the temperature value of master and salve
Restriction	

8.2.43 RE6H (LVSEL): LVD voltage Select

RE6H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Select LVD Voltage	W	0	1	1	1	0	0	1	1	0	E6H
1st Parameter	W	1							LVD_SEL[1]	LVD_SEL[0]	03h

Description	LVD_SEL[1:0]: Low power Voltage selection	
	LVD_SEL[1:0]	LVD value
	00	< 2.2 V
	01	< 2.3 V
	10	< 2.4 V
	11(default)	< 2.5 V
Restriction		

8.2.44 RE7H (PBC): Panel Break Check

RE7H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Select LVD Voltage	W	0	1	1	1	0	0	1	1	1	E7H
1st Parameter	R	1								PSTA	-

Description`	This command is used to enable panel check, and to disable after reading result. 1st Parameter:

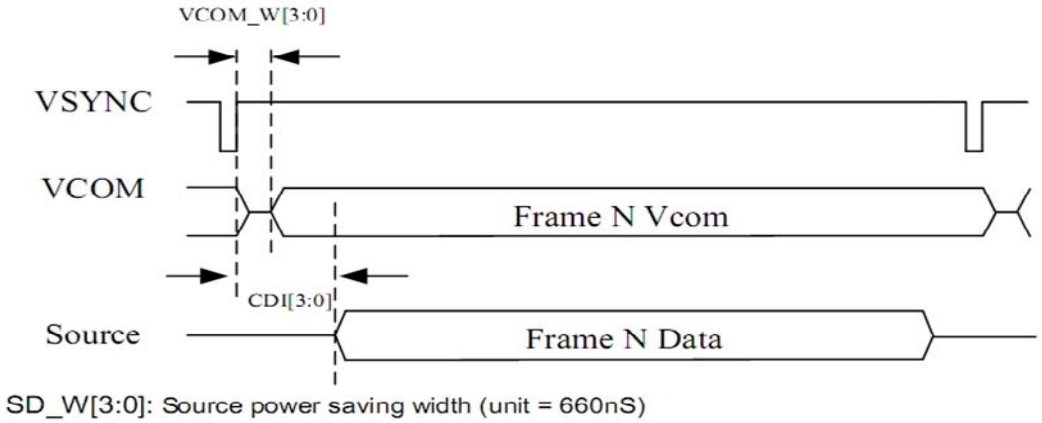
Bit	PSTA
0	Panel check fail (panel broken).
1	Panel check pass

Restriction	

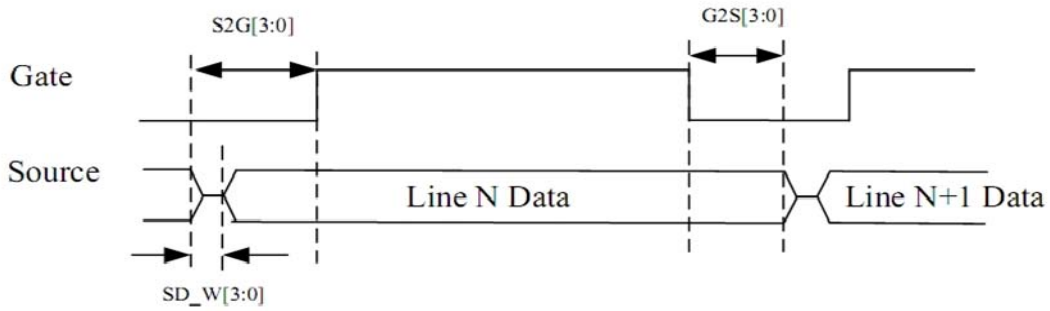
8.2.45 RE8H (PWS): Power Saving

RE8H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Power Saving	W	0	1	1	1	0	1	0	0	0	E8H
1st Parameter	W	1	VCOM_W[3]	VCOM_W[2]	VCOM_W[1]	VCOM_W[0]	SD_W[3]	SD_W[2]	SD_W[1]	SD_W[0]	00H

Description	This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.1st Parameter: Vcom_W[3:0]: VCOM power saving width (unit = line period)



SD_W[3:0]: Source power saving width (unit = 660nS)



Restriction	

8.2.46 RE9H (AUTO): AUTO Sequence

RE9H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
AUTO Sequence	W	0	1	1	1	0	1	0	0	1	E9H
1st Parameter	W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	00H

Description	The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP. AUTO (0xE9) + Code(0xA5) = (PON->DRF->POF) AUTO (0xE9) + Code(0xA7) = (PON->DRF->POF->DSLP)
Restriction	

8.2.47 REBH (LUT_BACKUP1_PG): OTP LUT backup1 program

REBH	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CHKSUM_PG	W	1	1	1	1	0	1	0	1	1	EFH

Description	This command is used to Program Checksum of LUT Table
Restriction	Apply VPP to OTP before use this command

8.2.48 RE0H (LUT_BACKUP1_RD): Read OTP LUT backup1

RFOH	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
RM_LUT_CMD	W	0	1	1	1	1	0	0	0	0	F0H
1st Parameter	W	1	-	-	-	tr10_lut_en	rmp2_table_sel[3]	rmp2_table_sel[2]	rmp2_table_sel[1]	rmp2_table_sel[0]	1FH
2nd Parameter	W	1	-	-	-	tr9_lut_en	rmp1_table_sel[3]	rmp1_table_sel[2]	rmp1_table_sel[1]	rmp1_table_sel[0]	1FH

NOTE: “-” Don’t care, can be set to VDD or GND level

Description

The command is used for indicating backup OTP blocks to remap for LUTs

Addr (hex)	OTP Bank 0 (3K Bytes)	Addr (hex)	OTP Bank 1 (3K Bytes)
00h~0Fh	Temp. segment	C00h~C0Fh	Temp. segment
20h~60h	Default setting	C20h~C60h	Default setting
100h	TR0 WF	D00h	TR0 WF
200h	TR1 WF	E00h	TR1 WF
300h	TR2 WF	F00h	TR2 WF
400h	TR3 WF	1000h	TR3 WF
500h	TR4 WF	1100h	TR4 WF
600h	TR5 WF	1200h	TR5 WF
700h	TR6 WF	1300h	TR6 WF
800h	TR7 WF	1400h	TR7 WF
900h	TR8 WF	1500h	TR8 WF
A00h	TR9 WF / Backup 1	1600h	TR9 WF / Backup 1
B00h	TR10 WF / Backup 2	1700h	TR10 WF / Backup 2

1st Parameter:
tr10_lut_en :

Value	Function
1	OTP Address B00h~BFFh is used as “TR10 WF”
0	OTP Address B00h~BFFh is used as “Backup 2”, And you can replace one of TR0 ~TR9.

rmp2_tab_sel [3:0] :
Only be functional when tr10_lut_en is set “0”, target LUTs to be replaced is shown below

Value	Target LUTs
0001	TR0
0010	TR1
0011	TR2
0100	TR3
0101	TR4
0110	TR5
0111	TR6
1000	TR7
1001	TR8
1010	TR9
1011~1111	None

2nd Parameter
tr9_lut_en :

Value	Function
1	OTP Address B00h~BFFh is used as “TR9 WF”
0	OTP Address B00h~BFFh is used as “Backup 1”, And you can replace one of TR0 ~TR8.

rmp1_tab_sel[3:0]
Only be functional when tr9_lut_en is set “0”, target LUTs to be replaced is shown below

Value	Target LUTs
0001	TR0
0010	TR1
0011	TR2
0100	TR3
0101	TR4
0110	TR5
0111	TR6
1000	TR7
1001	TR8
1010	TR9
1011~1111	None

Notice :
If rmp1_tab_sel = rmp2_tab_sel , the control hardware will reload “backup 1” block to replace target LUT.

Restriction	This command only actives when BUSY_N = “1”.

8.2.49 RF1H (SET_OTP_BANK): Set OTP program bank

RF1H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
SET_OTP_BANK	W	0	1	1	1	1	0	0	0	1	F1H
1st Parameter	W	1			-	-	-	-	LUT_bank0	reg_bank0	03H

Description	This command is used to set program bank for registers and LUTs

Addr (hex)	OTP Bank 0 (3K Bytes)	Addr (hex)	OTP Bank 1 (3K Bytes)
00h~0Fh	Temp. segment	C00h~C0Fh	Temp. segment
20h~60h	Default setting	C20h~C60h	Default setting
100h~BFFh	LUTs	D00h~17FFh	LUTs

reg_bank :

Value	Function
1	Program “Temp. segment” and “Default Setting” in bank 0
0	Program “Temp. segment” and “Default Setting” in bank 1

LUT_bank :

Value	Function
1	Program “LUTs” in bank 0
0	Program “LUTs” in bank 1

Restriction	

8.2.50 RF2H (RD_CHKSUM): Read checksum information

RF2H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
RD_CHKSUM	W	0	1	1	1	1	0	0	1	0	F2H
1st ~9th Parameter	R	1	Checksum from “TR0 WF” to “TR8 WF”								-
10th Parameter	R	1	Checksum of “TR9 WF / backup 1”								-
11th Parameter	R	1	Checksum of “TR10 WF / backup 2”								-
12th Parameter	R	1	Checksum comparison result from “TR0 WF” to “TR7 WF”								-
13th Parameter	R	1	Checksum comparison result from “TR8” and “TR10 WF / backup 2”								-

Description

This command is to read checksum information from OTP.
1st to 11th Parameter : Checksum from “TR0 WF” to “TR10 WF / backup 2”
12th Parametercommand is to read checksum information from OTP.
1st to 11th Parameter : Checksum from “TR0 WF” to “TR10 WF / backup 2”
12th Parameter

D7	D6	D5	D4	D3	D2	D1	D0
fault_TR7	fault_TR6	fault_TR5	fault_TR4	fault_TR3	fault_TR2	fault_TR1	fault_TR0

13th Parameter

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	-	fault_TR10 / fault_backup2	fault_TR9 / fault_backup1	fault_TR9

definition of fault_TRx / fault_backup_x

Value	Function
0	Checksum comparison : Equal
1	Checksum comparison : Not Equal

Restriction

8.2.51 RF3H (CAL_CHKSUM): Calculate Checksum

RF3H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CAL_CHKSUM	W	0	1	1	1	0	1	0	1	1	F3H

Description	This command is used to Calculate Checksum of LUT Table
Restriction	

9.Reference Circuit

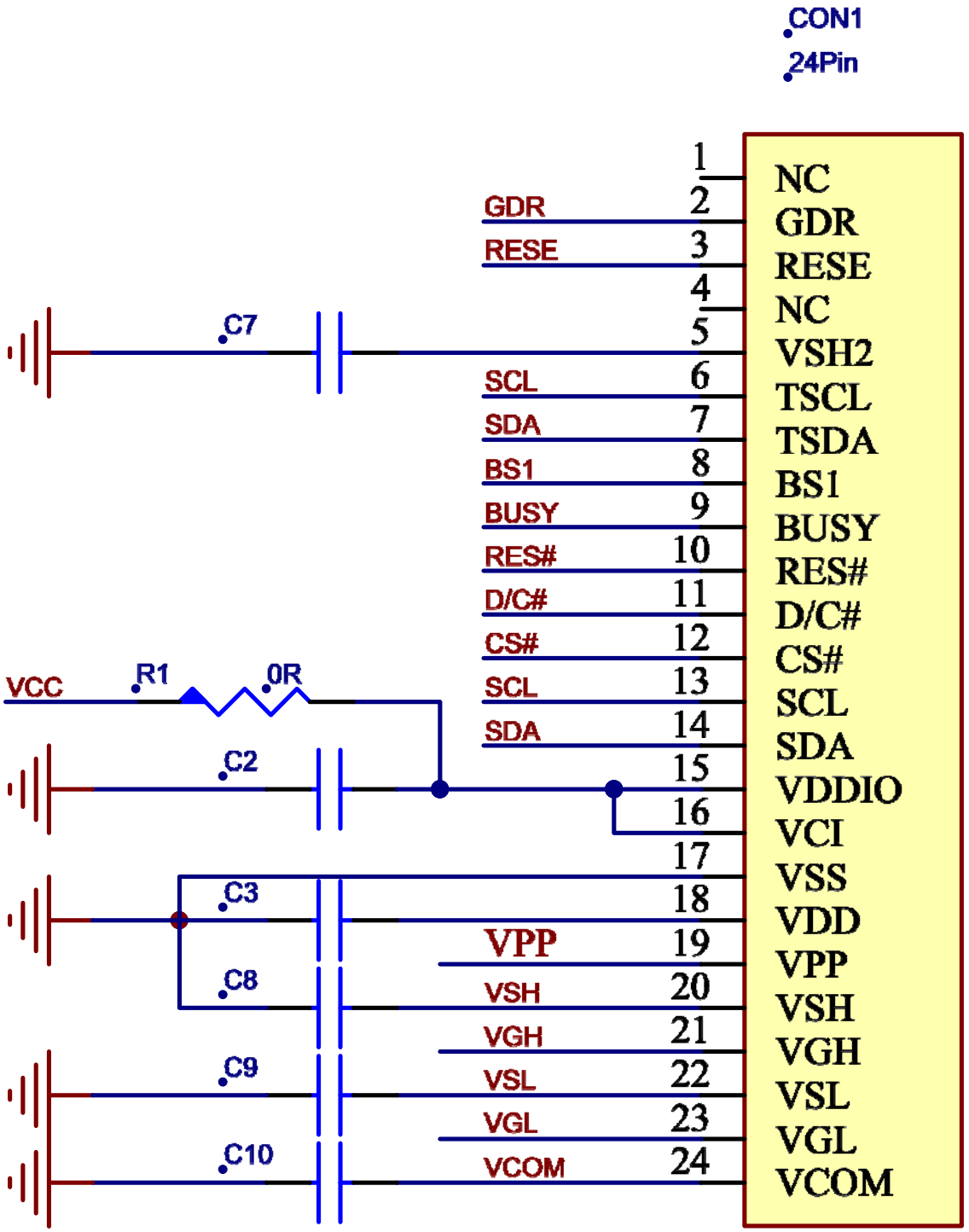


Figure. 9-1

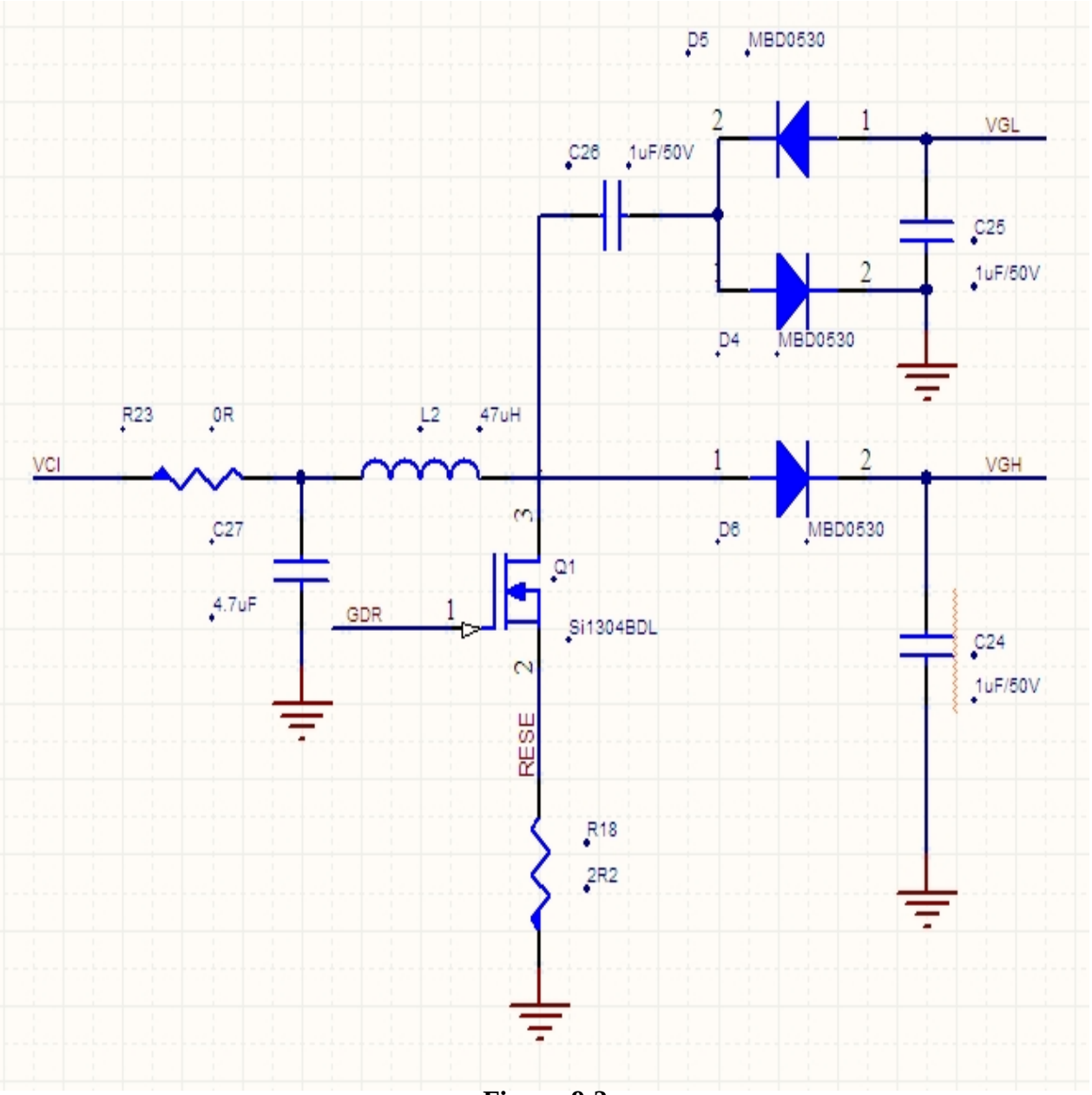

D5
MBD0530
2
1
VGL
C26
1uF/50V
C25
1uF/50V
2
D4
MBD0530
R23
0R
L2
47uH
VCI
1
2
VGH
C27
3
D6
MBD0530
Q1
4.7uF
GDR
1
Si1304BDL
C24
1uF/50V
2
RESE
R18
2R2

Figure. 9-2

10. ABSOLUTE MAXIMUM RATING

Table 10-1: Maximum Ratings

Symbol	Parameter	Rating	Unit	Humidity	Unit	Note
V_{CI}	Logic supply voltage	-0.5 to +6.0	V	-	-	
T_{OPR}	Operation temperature range	0 to 40	°C	45 to70	%	Note 10-1
Tttg	Transportation temperature range	-25 to 60	°C	-	-	Note 10-2
Tstg	Storage condition	0 to 40	°C	45 to70	%	Maximum storage time: 5 years
-	After opening the package	0 to 40	°C	45 to70	%	

Note 10-1： We guarantee the single pixel display quality for 0-35℃, but we only guarantee the barcode readable for 35-40℃. Normal use is recommended to refresh every 24 hours.

Note10-2: Tttg is the transportation condition, the transport time is within 10 days for -25℃~0℃ or 40℃~60℃.

Note 10-3： When the three-color product is stored. The display screen should be kept white and face up. In addition, please be sure to refresh the e-paper every three months.

11. DC CHARACTERISTICS

The following specifications apply for: VSS=0V, VCI=3.3V, TOPR=25℃.

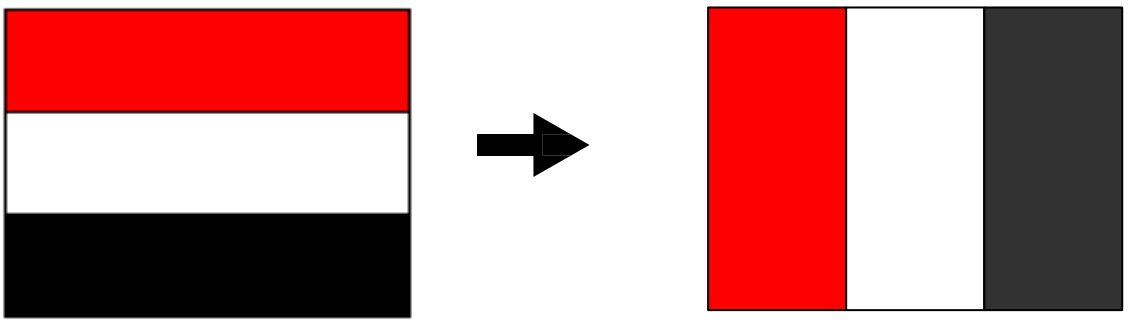
Table 13-1: DC Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	
VCI	VCI operation voltage	-	VCI	2.3	3.3	3.6	
VIH	High level input voltage	-	SDA, SCL, CS#, D/C#, RES#, BS1	0.8VDDIO	-	-	
VIL	Low level input voltage	-		-	-	0.2VDDIO	
VOH	High level output voltage	IOH = -100uA	BUSY,	0.9VDDIO	-	-	
VOL	Low level output voltage	IOL = 100uA		-	-	0.1VDDIO	
Iupdate	Module ~~operating~~ current	-	-	-	3	-	
Isleep	Deep sleep mode	VCI=3.3V	-	-	-	3	

- The Typical power consumption is measured using associated 25℃ waveform with following pattern transition: from horizontal scan pattern to vertical scan pattern. (Note 11-1)
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by XingTai.
- Vcom value will be OTP before in factory or present on the label sticker.

Note 11-1

The Typical power consumption



12. Serial Peripheral Interface Timing

The following specifications apply for: VSS=0V, VCI=2.3V to 3.6V, T_{OPR}=25℃

Write mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Write Mode)			20	MHz
tCSSU	Time CSB has to be low before the first rising edge of SCLK	20			ns
tCSHLD	Time CSB has to remain low after the last falling edge of SCLK	20			ns
tCSHIGH	Time CSB has to remain high between two transfers	100			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	25			ns
tSCLLOW	Part of the clock period where SCL has to remain low	25			ns
tSISU	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
tSIHLD	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Read Mode)			2.5	MHz
tCSSU	Time CSB has to be low before the first rising edge of SCLK	100			ns
tCSHLD	Time CSB has to remain low after the last falling edge of SCLK	50			ns
tCSHIGH	Time CSB has to remain high between two transfers	250			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	180			ns
tSCLLOW	Part of the clock period where SCL has to remain low	180			ns
tSOSU	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
tSOHLD	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

Note: All timings are based on 20% to 80% of VDDIO-VSS

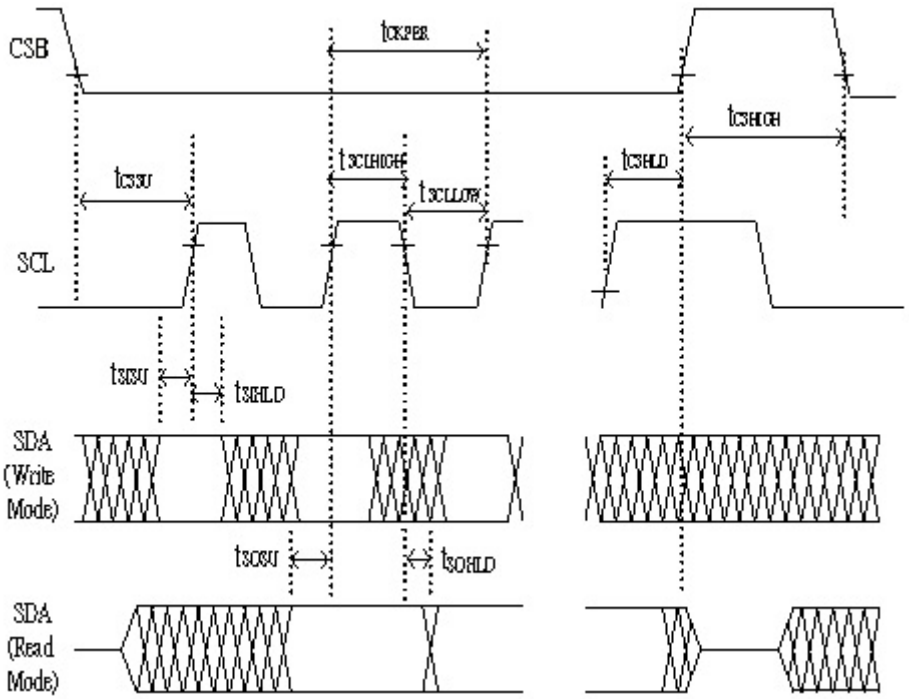


Figure 12-1: Serial peripheral interface characteristics

13. Power ON /OFF Sequence

In order to prevent IC fail in power on resetting, the power sequence must be followed as below.

Power ON Sequence

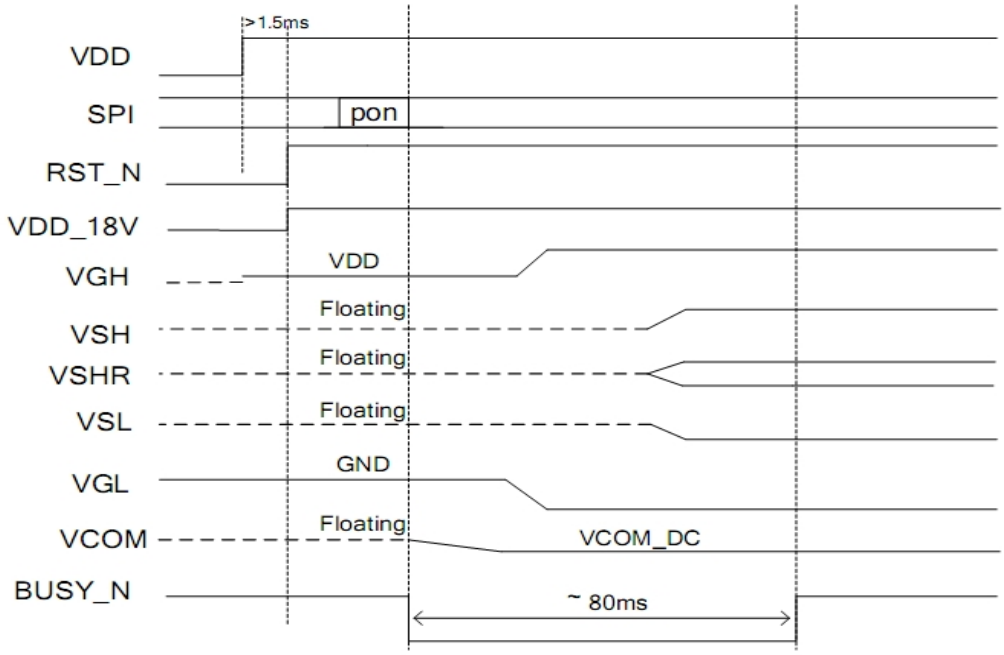


Figure 1: Power on sequence

Power OFF Sequence

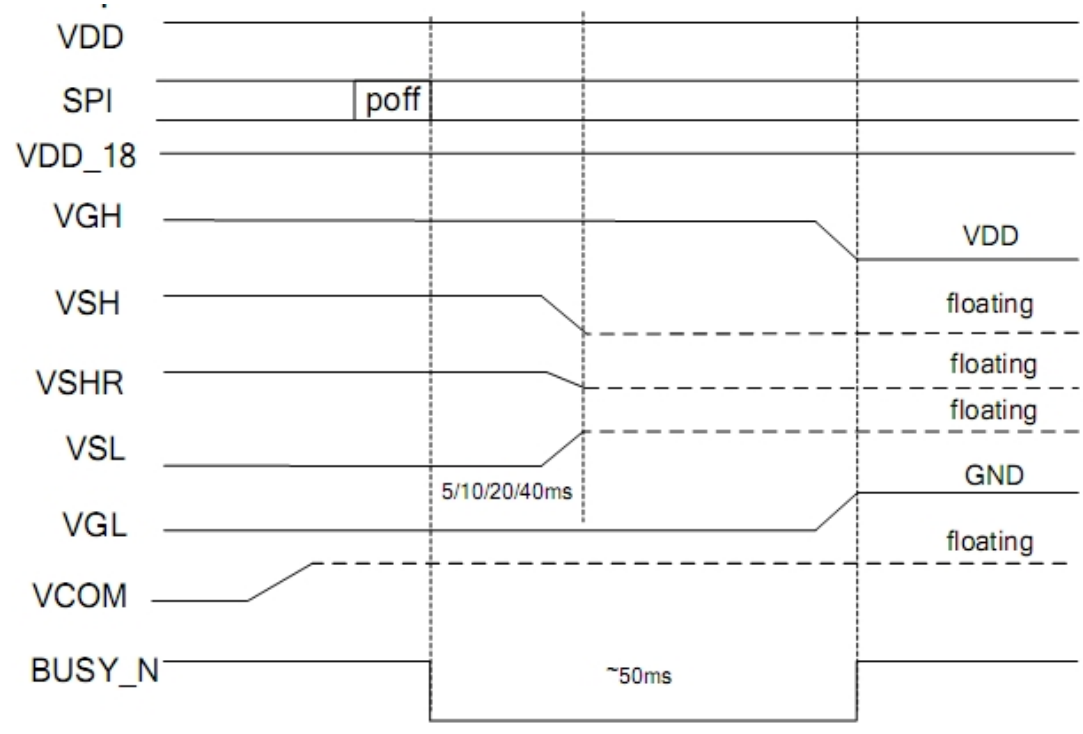


Figure 2: Power off sequence

DSLP sequence

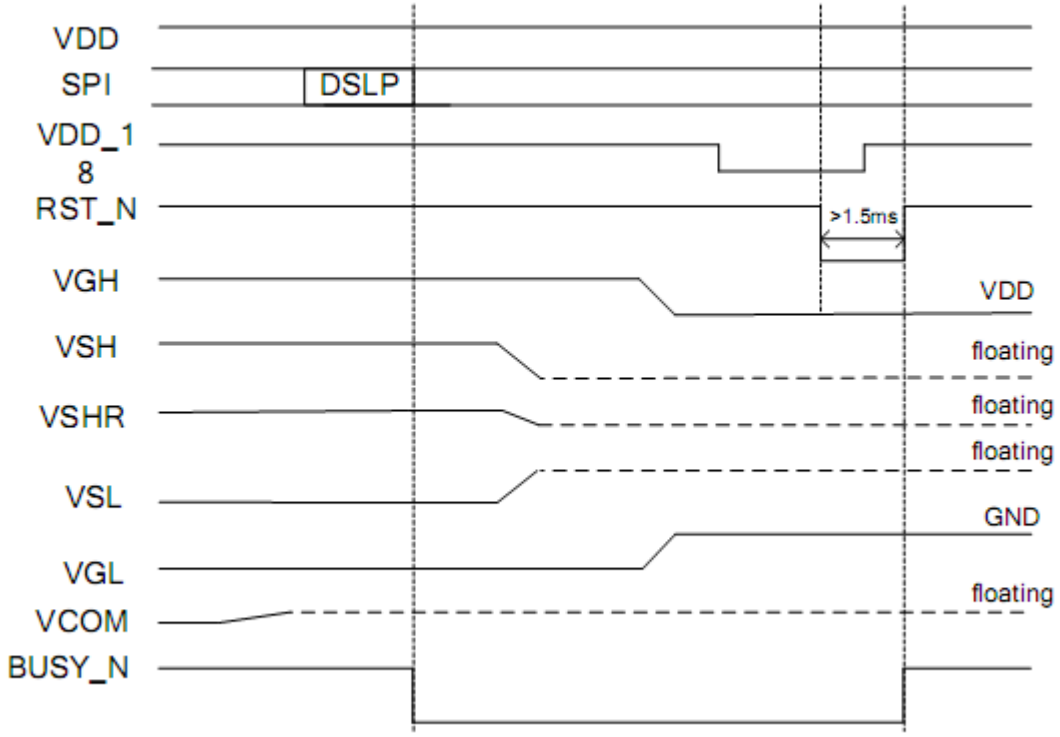


Figure 3: DSLP sequence

14. Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25℃	40	-	mAs	-
Deep sleep mode	-	25℃	-	3	uA	-

mAs=update average current×update time

15.Optical characteristics

15.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless
otherwise specified.

T=25℃

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 15-1
Gn	2Grey Level	-	-	DS+(WS-DS)×n(m-1)	-	L*	-
CR	Contrast Ratio	-	10	15	-		-
DS	Dark State L* value		-	13	14		Note 15-1
	Dark State a* value		-	3	5		Note 15-1
WS	White State L* value		63	65	-		Note 15-1
RS	Red State L* value	Red	25	28	-		Note 15-1
	Red State a* value	Red	36	40	-		Note 15-1
Panel's life	-	0℃～40℃		5years	-	-	Note 15-2
Panel	Image Update	Storage and transportation	-	Update the white screen	-	-	-
	Update Time	Operation	-	Suggest Updated once a day	-	-	-

WS: White state, DS : Dark state

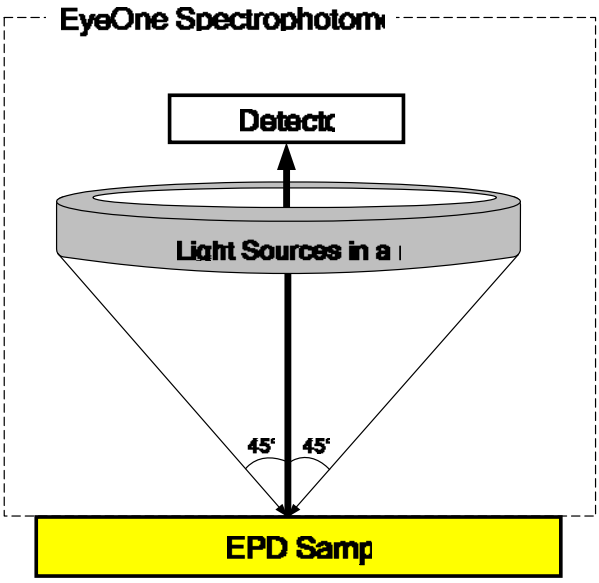
Note 15-1: Luminance meter : Eye - One Pro Spectrophotometer

Note 15-2: We don't guarantee 5 years pixels display quality for humidity below 45%RH or above 70%RH; at least update 1 time per day.

15.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd):

CR = Rl/Rd

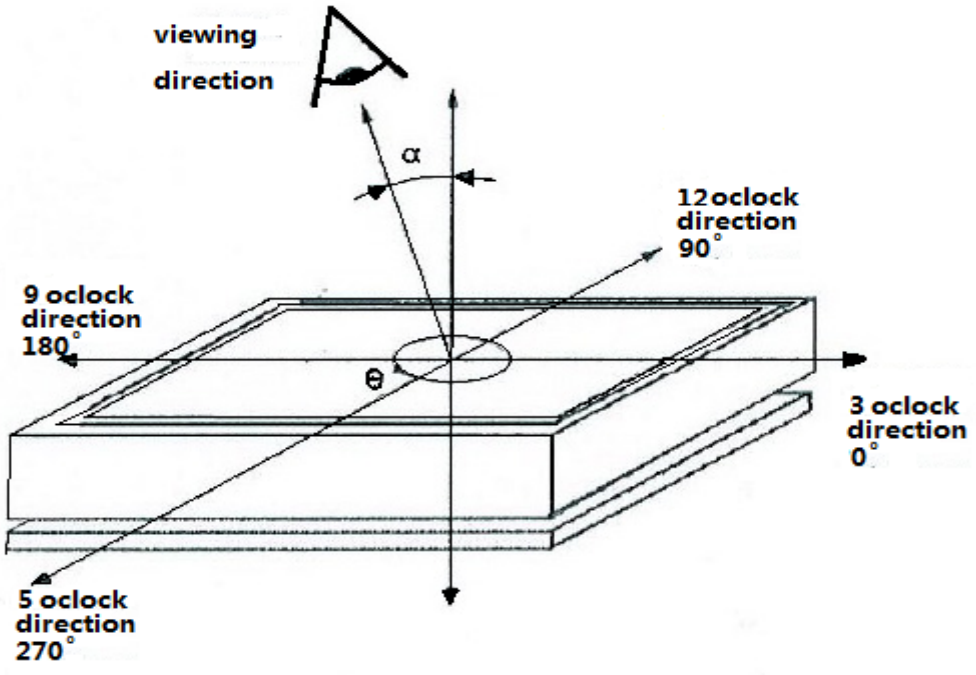


15.3 Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factor $_{\text{white board}}$ x (L_{center} / $L_{\text{white board}}$)

L_{center} is the luminance measured at center in a white area (R=G =B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



16. HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display module should be kept flat or fixed to a rigid, curved support with limited bending along the long axis. It should not be used for continual flexing and bending. Handle with care. Should the display break do not touch any material that leaks out. In case of contact with the leaked material then wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.
Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status	
Product specification	The data sheet contains final product specifications.

Limiting values
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.
Application information
Where application information is given, it is advisory and dose not form part of the specification.

Product Environmental certification
ROHS
REMARK
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

17. Reliability test

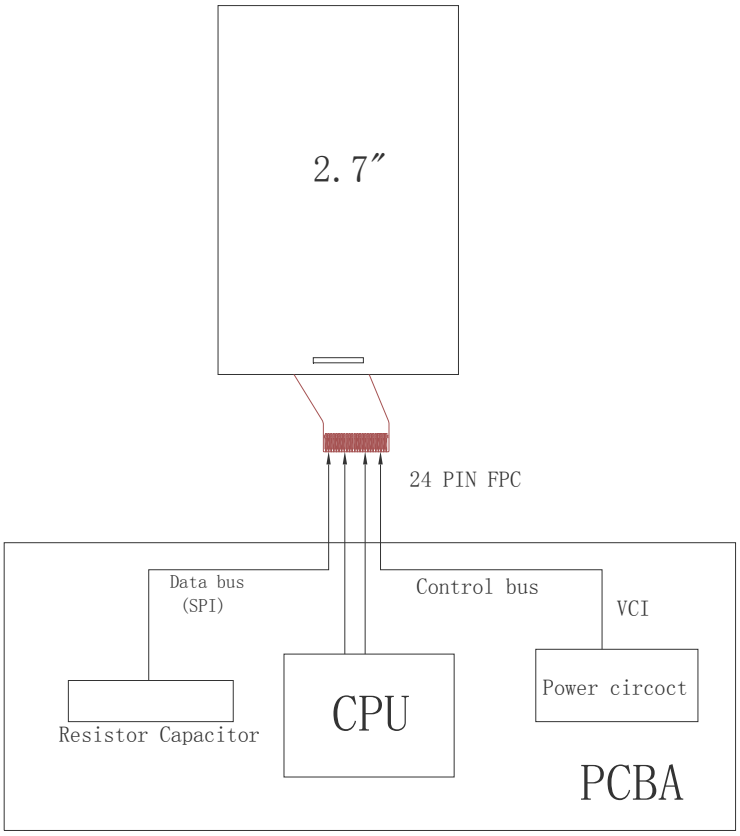
	TEST	CONDITION	REMARK
1	High-Temperature Operation	T=40℃, RH=35%RH, For 240Hr	
2	Low-Temperature Operation	T = 0℃ for 240 hrs	
3	High-Temperature Storage	T=50℃ RH=35%RH For 240Hr	Test in white pattern
4	Low-Temperature Storage	T = -25℃ for 240 hrs Test in white pattern	Test in white pattern
5	High Temperature, High-Humidity Operation	T=40℃,RH=90%RH, For 168Hr	
6	High Temperature, High-Humidity Storage	T=50℃,RH=80%RH,For 240Hr	Test in white pattern
7	Temperature Cycle	-25℃(30min)~60℃(30min),50 Cycle	Test in white pattern
8	Package Vibration	1.04G,Frequency : 20~200Hz Direction : X,Y,Z Duration: 30 minutes in each direction	Full packed for shipment
9	Package Drop Impact	Drop from height of 100 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment
10	UV exposure Resistance	765 W/㎡ for 168hrs,40℃	
11	Electrostatic discharge	Machine model: +/-250V,0Ω,200pF	

Actual EMC level to be measured on customer application.

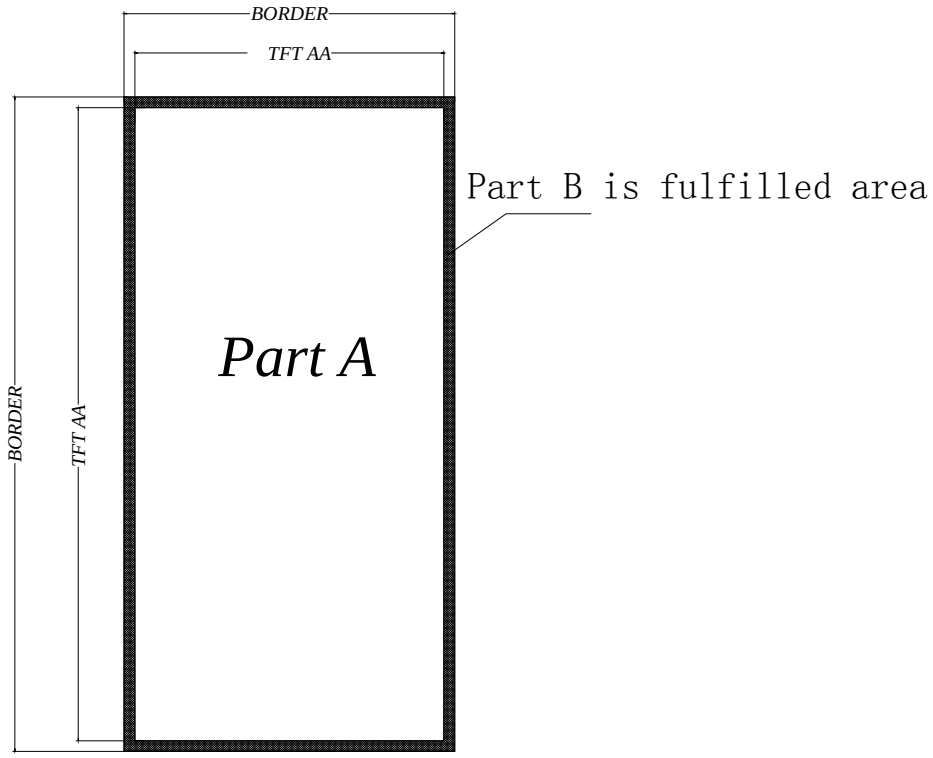
Note1: The protective film must be removed before temperature test.

Note2： Stay white pattern for storage and non-operation test.

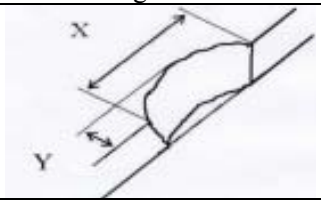
18. Block Diagram

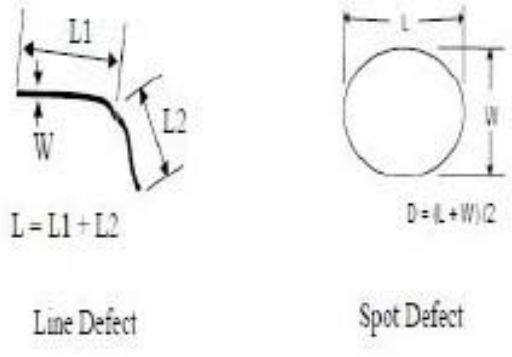


19. PartA/PartB specification



20. Point and line standard

Shipment Inspection Standard						
Equipment：Electrical test fixture, Point gauge						
Outline dimension	45.8(H)×70.42(V) ×0.9(D)	Unit：㎜	Part-A	Active area	Part-B	Border area
Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle
	19℃～25℃	55%±5%RH	800～1300Lux	300 ㎜	35Sec	
Defect type	Inspection method	Standard		Part-A		Part-B
Spot	Electric Display	D≤0.25 ㎜		Ignore		Ignore
		0.25 ㎜＜D≤0.4 ㎜		N≤4		Ignore
		D＞0.4 ㎜		Not Allow		Ignore
Display unwork	Electric Display	Not Allow		Not Allow		Ignore
Display error	Electric Display	Not Allow		Not Allow		Ignore
Scratch or line defect(include dirt)	Visual/Film card	L≤2 ㎜，W≤0.2 ㎜		Ignore		Ignore
		2.0mm＜L≤5.0mm，0.2＜W≤0.3mm,		N≤2		Ignore
		L＞5 ㎜，W＞0.3 ㎜		Not Allow		Ignore
PS Bubble	Visual/Film card	D≤0.2mm		Ignore		Ignore
		0.2mm≤D≤0.35mm & N≤4		N≤4		Ignore
		D＞0.35 mm		Not Allow		Ignore
Side Fragment	Visual/Film card	X≤6mm，Y≤0.4mm, Do not affect the electrode circuit (Edge chipping) X≤1mm，Y≤1mm, Do not affect the electrode circuit((Corner chipping) Ignore				
						
Remark	1.Cannot be defect & failure cause by appearance defect;					
	2.Cannot be larger size cause by appearance defect;					
	L=long W=wide D=point size N=Defects NO					



L=long W=wide D=point size

21.Barcode

21.1 Babel appearance

ABBBBBBBCC
DDDEEEFGGG

21.2 QR scanned information（Total 28 code number+ 2 blank spaces）

A BBBBBBB CC □ DDD EEE F GGG □ H III J KKK
① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑪

① A——The factory code
② BBBBBBB———Module name of EPD
③ CC———FPL model name
④ DDD———Date of production
⑤ EEE———Production lot
⑥ F———Separator
⑦ GGG———FPL Lot
⑧ H———Normal Lot
⑨ III———TFT、PS、EC.
⑩ J———IC
⑪ KKK———Serial NO.
□ blank spaces

22. Packing

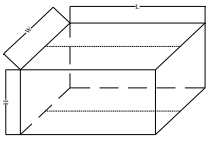
Packing Spec

Sheet No:

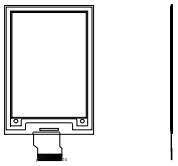
HOLITECH	Part No	HINK-E027A15-A0	DATE	2020.03.06	VER	A0	Page	2-1

一, Package Type: Box

Box No	HINK-E029A01-ZX-A0
Box size	515*322*170
Containment	252PCS



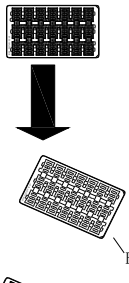
PRODUCT DRAWING



二,Inside package type:Plastic Tray unit: mm

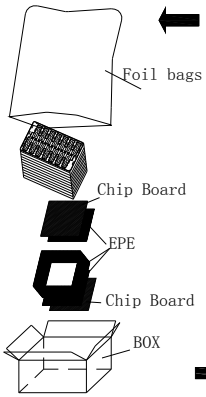
Plastic Tray	465*280*15	13 pcs
Anti-static foil bags	700*530*0.1	1 pcs
EPE(inside)	405.5*250.4*2	12 pcs
EPE(Up-Down)	485*145*10	2 pcs
EPE(Left-Right)	285*480*10	2 pcs
EPE(Front-back)	310*145*10	2 pcs
Chip board	500*306*5	2 pcs
Quantity/tray	21 pcs	
Tray number/sheet	12+1 Sheets	
Box	1	

Step 1:
Material: Tray, EPE
Put the product in to the tray and keep the dispaly side up. Then put anti-static EPE in to each holes.

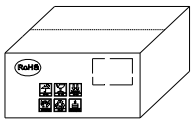


Step 2:
1) Must keep the angle 180 degree placed between the neighboring Plastic trays.
2) There are 12 layers product, total14*12=168pcs。
3) An empty Plastic tray intersects put on the top of the plastic trays.

Step 3:
1) In each case, put 2 bags of desiccant. then seal the trays with adhesive tapes.
2) Put the trays into foil bags.
3) heat seal the foil bags.



Step 4:
1)First put a chip board on the buttom of the box, then placed the down EPE, the left - right and front -back EPE.
2) Placed the sealed products into the box.
3) The last placed the up EPE on the top of the trays, and place a chip board on it.



Step 5:
1) Seal the box with adhensive tapes 。
2) Paste the lable onto the exterior box, and the lable can't cover the safety , transfer and RoSH sign。

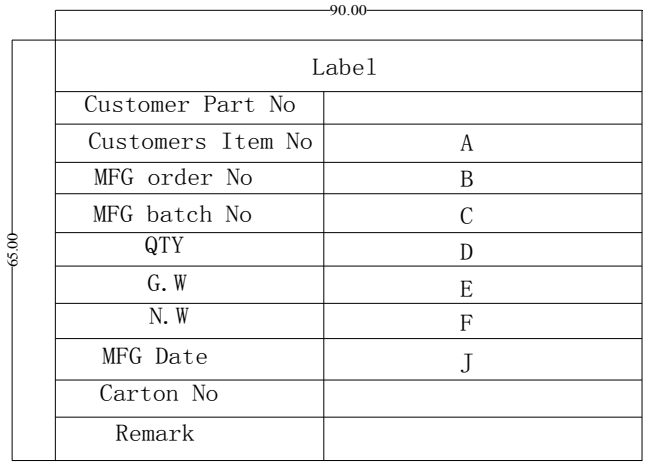
Design	Z.Z.Q	Approve	H.Z.P	Confirm	X.X.M
Date	2020.03.06	Date	2020.03.06	Date	2020.03.06

Packing Spec

Sheet No

HOLITECH	Part No	HINK-E027A15-A0	Date	2020.03.06	VER	A0	Page	2-2

The label outside the carton print as below



Label	
Customer Part No	
Customers Item No	A
MFG order No	B
MFG batch No	C
QTY	D
G.W	E
N.W	F
MFG Date	J
Carton No	
Remark	

NOTE:

1."A" Print customer Item No

2."B" Print customer Order No

3."C" Print MFG Batch No(Separate packing for different batch products. Mixed packing available for the odd number of different batch print all the batch NO&QTY accordingly if happened.

4."D"Print product qty

5."E"Print the G.W

6."F"Print the N.W

7."J"Print the MFG date

8.Before packing make sure the FPL batch ,item and qty are the same as which on the Final passed card.

Design	Z.Z.Q	Approve	H.Z.P	Confirm	X.X.M
Date	2020.03.06	Date	2020.03.06	Date	2020.03.06