Specification For HINK 2.7''EPD

Model NO.: HINK-E027A22

Product VER:A0

Customer Approval

Customer	
Approval By	
Date Of Approval	

It will be agreed by the receiver,if not sign back the Specification within 15days.

Prepared By	Checked By	Approval By
Daisy Zhu	Yufeng Zhou	Ziping Hu

CONTENTS

Version	Content	Date	Producer
A0	New release	20120/11/20	Daisy Zhu

1. General Description

HINK-E027A22 is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design. The 2.7" active area contains 176×264 pixels, and has 1-bit B/W full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC. SRAM.LUT, VCOM and border are supplied with each panel.

2. Features

- 176×264 pixels display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C signal master interface to read external temperature sensor/built-in temperature sensor

3. Application

Electronic Shelf Label System

4. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.7	Inch	
Display Resolution	176(H)×264(V)	Pixel	Dpi:117
Active Area	38.19(H)×57.29(V)	mm	
Pixel Pitch	0.217×0.217	mm	
Pixel Configuration	Rectangle		
Outline Dimension	45.8(H)×70.42(V) ×0.9(D)	mm	**Without masking film**
Weight	5.0±0.5	g	

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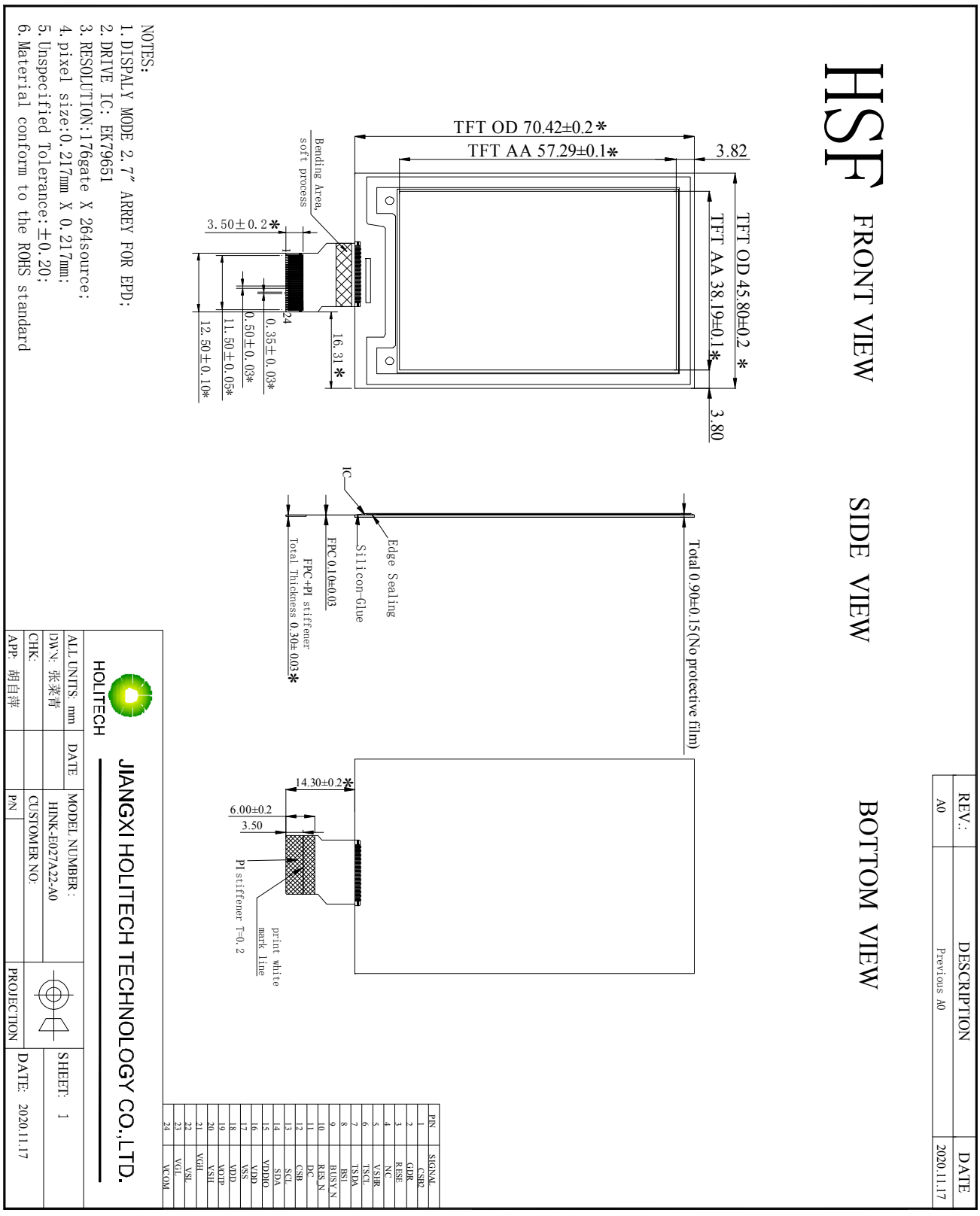
5. Mechanical Drawing of EPD module



6. Input/Output Terminals

Pin #	Single	Description	Remark
1	NC	No connection and do not connect with other NC pins	Keep Open
2	GDR	N-Channel MOSFET Gate Drive Control	
3	RESE	Current Sense Input for the Control Loop	
4	NC	No connection and do not connect with other NC pins e	Keep Open
5	VSHR	Positive source voltage for Red	
6	TSCL	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I2C Interface to digital temperature sensor Date pin	
8	BS	Bus selection pin	Note 6-5
9	BUSY _N	Busy state output pin	Note 6-4
10	RST _ N	Reset	Note 6-3
11	DC	Data /Command control pin	Note 6-2
12	CSB	Chip Select input pin	Note 6-1
13	SCL	serial clock pin (SPI)	
14	SDA	serial data pin (SPI)	
15	VDDIO	IO voltage supply	
16	VDD	Digital/Analog power.	
17	VSS	Digital ground	
18	VDD _1.8V	1.8V voltage input &output	
19	VOTP	OTP program power (7.5V)	
20	VSH	Positive Source driving voltage	
21	VGH	Positive gate voltage	
22	VSL	Negative Source driving voltage	
23	VGL	Negative gate voltage.	
24	VCOM	VCOM driving voltage	

Note 6-1: This pin (CSB) is the chip select input connecting to the MCU. The chip is enabled for MCU communication: only when CSB is pulled LOW.

Note 6-2: This pin (DC) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Note 6-3: This pin (RST_N) is reset signal input. The Reset is active low.

Note 6-4: This pin (BUSY_N) is Busy state output pin. When Busy_N is High the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy_N pin High when the driver IC is working such as:

- Outputting display waveform;
- Communicating with digital temperature sensor

Note 6-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is "Low", 4-line SPI is selected. When it is "High", 3-line SPI (9 bits SPI) is selected.

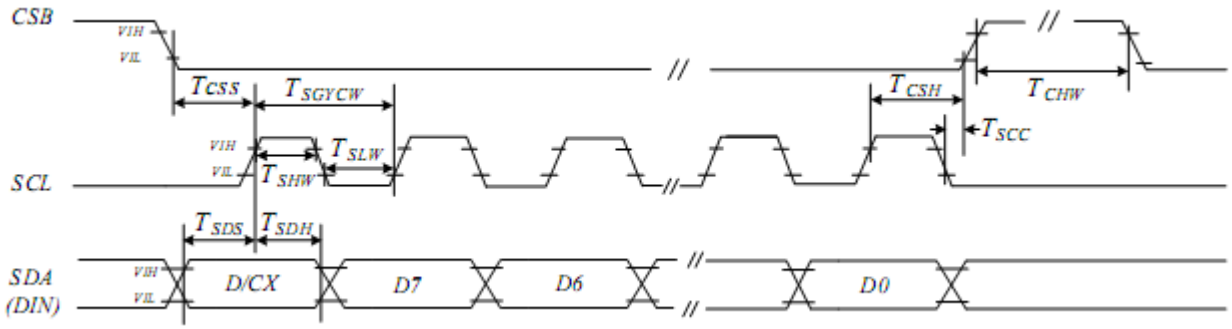
7.SPI COMMAND DESCRIPTION

7.1 "3-Wire" Serial Port Interface

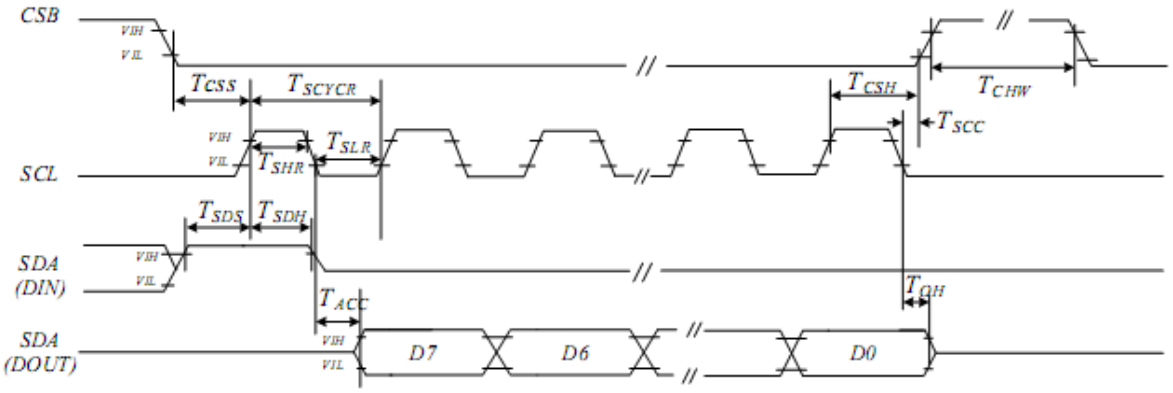
E027A22 use the 3-wire serial port as communication interface for all the function and command setting.

E027A22 3-wire/4-wire engine act as a "slave mode" for all the time, and will not issue any command to the 3-wire/4-wire bus itself.

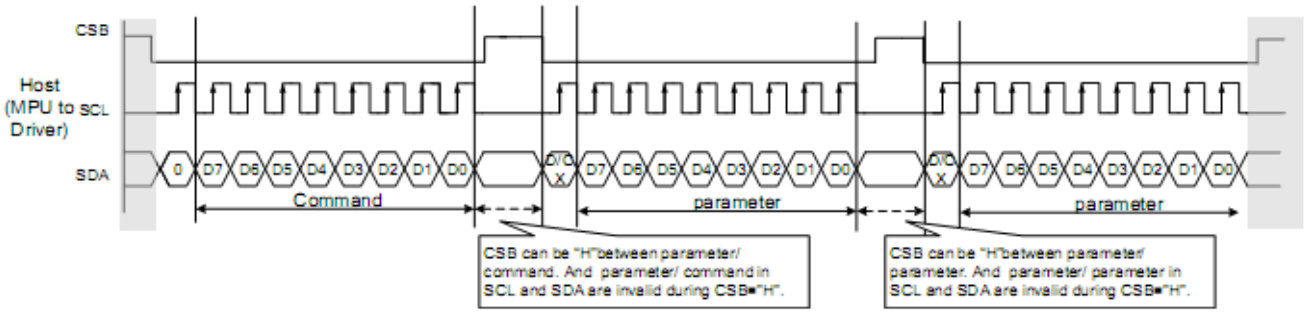
Under read mode, 3-Wire engine will return the data during "Data phase". The returned data should be latched at the rising edge of SCL by external controller. Data in the "Hi-Z phase" will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under "Hi-Z phase" and "Data phase".



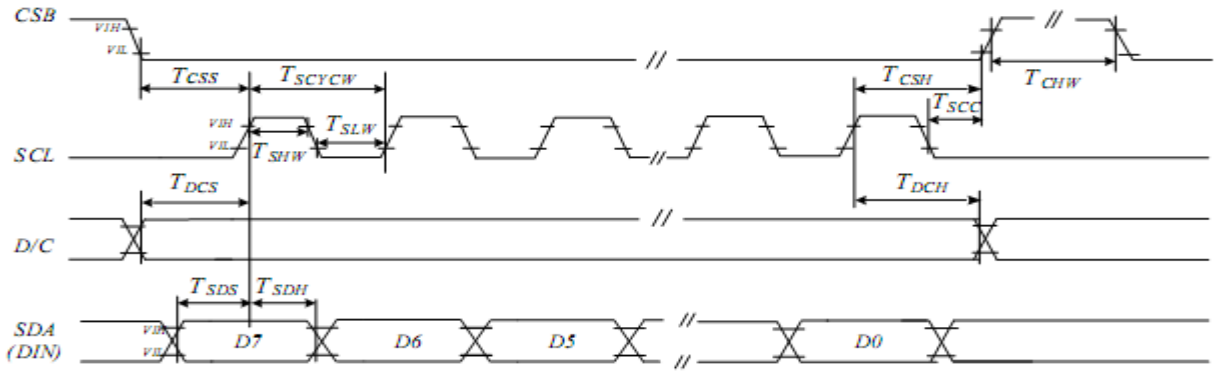
3 pin serial interface characteristics (write mode)



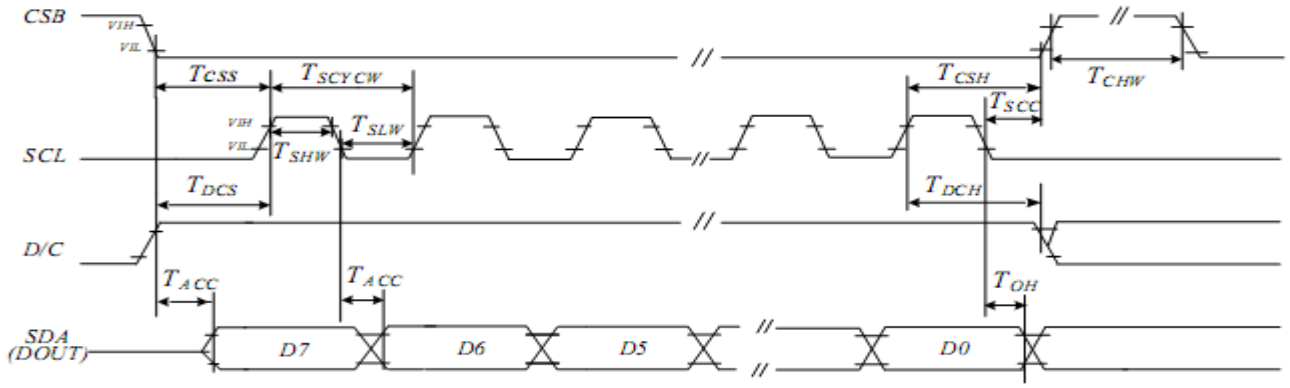
3 pin serial interface characteristics (read mode)



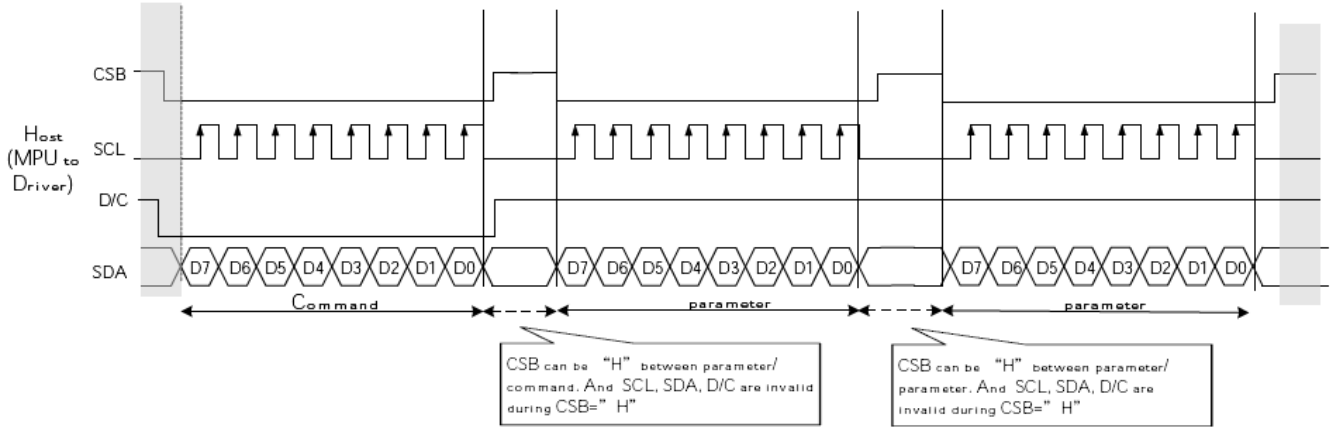
7.2 "4-Wire" Serial Port Interface



4 pin serial interface characteristics(write mode)



4 pin serial interface characteristics(read mode)



8. COMMAND TABLE

8.1.1R00H (PSR): Panel setting Register

R00H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PSR	W	0	0	0	0	0	0	0	0	0	00H
1st Parameter	W	1	RES[1]	RES[0]	REG_EN	BWR	UD	SHL	SHD_N	RST_N	0Fh
2nd Parameter	W	1	-	-	-	VCMZ	TS_AUTO	VGLTIEG	NORG	VC_LUTZ	09h

NOTE: "-" Don't care, can be set to VDD or GND level

Description -The command defines as :

1st Parameter

Bit	Name	Description
0	RST_N	RST_N function 1 : no effect. (default) 0: Booster OFF, Register data are set to their default values, and SEG/BG/VCOM:floating
1	SHD_N	SHD_N function 0 : Booster OFF, register data are kept, and SEG/BG/VCOM are kept floating. 1 : Booster on. (default)
2	SHL	SHL function 0: Shift left; First data=Sn →Sn-1 → …→S2 →Last data=S1. 1: Shift right: First data=S1→ S2 → …→Sn-1 → Last data=Sn. (default)
3	UD	UD function 0:Scan down; First line=Gn→Gn-1 →…→ G2 → Last line=G1. 1:Scan up; First line=G1 →G2 →…→Gn-1 →Last line=Gn. (default)
4	BWR	Color selection setting 0: Pixel with B/W/Red. Run both LU1 and LU2. (default) 1: Pixel with B/W. Run LU1 only
5	REG_EN	LUT selection setting 0 : Using LUT from OTP(default) 1 : Using LUT from register
7-6	RES[1,0]	Resolution setting 00: Display resolution is 96x230 01: Display resolution is 96x252 10: Display resolution is 128x296 (default) 11: Display resolution is 160x296

Notes

1. When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD turn off. SD output and VCOM will base on previous condition and keep floating.
2. When RST_N become low, driver will reset. All register will reset to default value. All of the driver's functions will disable. SD output and VCOM will base on previous condition and keep floating.

Description -The command defines as :
2nd Parameter

Bit	Name	Description
0	VC_LUTZ	RST_N function 0 : Display off, VCOM keep to power off
1	NORG	VCOM status function 0 : No effect (default) 1 : Expect refreshing display, VCOM is tied to GND
2	VGLTIEG	VGL power off status function 0 : Power off, VGL will be floating (default) 1 : Power off, VGL will be tied to GND
3	TS_AUTO	Temperature sensing will be activated automatically one time 0 : Before enabling refresh, temperature sensing on 1 : Before enabling booster, temperature sensing on (default)
4	VCMZ	VCOM status function 0 : No effect (default) 1 : VCOM is always floating
Priority of VCOM setting: VCMZ > NORG > VC_LUTZ		

8.1.2 R01H (PWR): Power setting Register

R01H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWR	W	0	0	0	0	0	0	0	0	1	01h
1st Parameter	W	1	-	-	-	-	-	-	VDS_EN	VDG_EN	03h
2nd Parameter	W	1	VGHL_LV [2]	-	-	-	-	VCOM_HV	VGHL_LV [1]	VGHL_LV [0]	00h
3rd Parameter	W	1	-	-	VSH [5]	VSH [4]	VSH [3]	VSH [2]	VSH [1]	VSH [0]	26h
4th Parameter	W	1	-	-	VSL [5]	VSL [4]	VSL [3]	VSL [2]	VSL [1]	VSL [0]	26h
5th Parameter	W	1	OPTEN	VSHR [6]	VSHR [5]	VSHR [4]	VSHR [3]	VSHR [2]	VSHR [1]	VSHR [0]	06h

NOTE: "-" Don't care, can be set to VDD or GND level

Description -The command defines as :E4
1st Parameter:

Bit	Name	Description
0	VDG_EN	Source power selection. 0 : External source power from VSH/VSL/VSHR pins. 1 : Internal DC/DC function for generate VSH/VSL/VSHR (default)
1	VDS_EN	Source power selection. 0 : External source power from VSH/VSL/VSHR pins. 1 : Internal DC/DC function for generate VSH/VSL/VSHR (default)

2nd Parameter:

Bit	Name	Description
1-0	VGHL_LV	VGHL_LV Voltage Level. 00: VGH=20 v, VGL=-20v (default) 01: VGH=19 v, VGL=-19v 10: VGH=18 v, VGL=-18v 11: VGH=17 v, VGL=-17v
2	VCOM_HV	VCOM Voltage Level 0: VCOMH=VSH-VCOMDC (default) VCOML=VSL-VCOMDC 1: VCOMH=VGH VCOML=VGL
7	VGHL_LV[2]	VGHL_LV Voltage Level. 000: VGH=20 v, VGL=-20v 001: VGH=19 v, VGL=-19v 010: VGH=18 v, VGL=-18v 011: VGH=17 v, VGL=-17v 100: VGH=16 v, VGL=-16v 101: VGH=15 v, VGL=-15v

3rd Parameter: Internal VSH power selection for B/W LUT.

Bit	Name	Description								
		Internal VSH power selection.								
		VSH[5:0]		Voltage (V)	VSH[5:0]		Voltage (V)	VSH[5:0]		Voltage (V)
5-0	VSH	000000	00h	6.4	010000	10h	9.6	100000	20h	12.8
		000001	01h	6.6	010001	11h	9.8	100001	21h	13
		000010	02h	6.8	010010	12h	10	100010	22h	13.2
		000011	03h	7	010011	13h	10.2	100011	23h	13.4
		000100	04h	7.2	010100	14h	10.4	100100	24h	13.6
		000101	05h	7.4	010101	15h	10.6	100101	25h	13.8
		000110	06h	7.6	010110	16h	10.8	100110	26h	14
		000111	07h	7.8	010111	17h	11	100111	27h	14.2
		001000	08h	8	011000	18h	11.2	101000	28h	14.4
		001001	09h	8.2	011001	19h	11.4	101001	29h	14.6
		001010	0Ah	8.4	011010	1Ah	11.6	101010	2Ah	14.8
		001011	0Bh	8.6	011011	1Bh	11.8	101011	2Bh	15
		001100	0Ch	8.8	011100	1Ch	12			
		001101	0Dh	9	011101	1Dh	12.2			
		001110	0Eh	9.2	011110	1Eh	12.4			
		001111	0Fh	9.4	011111	1Fh	12.6			

4th Parameter: Internal VSL power selection for B/W LUT.

Bit	Name	Description											
		Internal VSL power selection.											
		VSL[5:0]		Voltage(V)	VSL[5:0]		Voltage(V)	VSL[5:0]		Voltage(V)			
		000000	00h	-6.4	010000	10h	-9.6	100000	20h	-12.8			
		000001	01h	-6.6	010001	11h	-9.8	100001	21h	-13			
		000010	02h	-6.8	010010	12h	-10	100010	22h	-13.2			
		000011	03h	-7	010011	13h	-10.2	100011	23h	-13.4			
		000100	04h	-7.2	010100	14h	-10.4	100100	24h	-13.6			
		000101	05h	-7.4	010101	15h	-10.6	100101	25h	-13.8			
		000110	06h	-7.6	010110	16h	-10.8	100110	26h	-14			
		000111	07h	-7.8	010111	17h	-11	100111	27h	-14.2			
5-0	VSL	001000	08h	-8	011000	18h	-11.2	101000	28h	-14.4			
		001001	09h	-8.2	011001	19h	-11.4	101001	29h	-14.6			
		001010	0Ah	-8.4	011010	1Ah	-11.6	101010	2Ah	-14.8			
		001011	0Bh	-8.6	011011	1Bh	-11.8	101011	2Bh	-15			
		001100	0Ch	-8.8	011100	1Ch	-12						
		001101	0Dh	-9	011101	1Dh	-12.2						
		001110	0Eh	-9.2	011110	1Eh	-12.4						
		001111	0Fh	-9.4	011111	1Fh	-12.6						

5th Parameter:

Bit	Name	Description											
		Internal VSHR power selection.											
		VSH[5:0]		Voltage(V)	VSH[5:0]		Voltage(V)	VSH[5:0]		Voltage(V)			
		000000	00h	2.4	010110	16h	6.8	101100	2Ch	11.2			
		000001	01h	2.6	010111	17h	7	101101	2Dh	11.4			
		000010	02h	2.8	011000	18h	7.2	101110	2Eh	11.6			
		000011	03h	3.0	011001	19h	7.4	101111	2Fh	11.8			
		000100	04h	3.2	011010	1Ah	7.6	110000	30h	12			
		000101	05h	3.4	011011	1Bh	7.8	110001	31h	12.2			
		000110	06h	3.6	011100	1Ch	8	110010	32h	12.4			
		000111	07h	3.8	011101	1Dh	8.2	110011	33h	12.6			
		001000	08h	4	011110	1Eh	8.4	110100	34h	12.8			
		001001	09h	4.2	011111	1Fh	8.6	110101	35h	13			
		001010	0Ah	4.4	100000	20h	8.8	110110	36h	13.2			
		001011	0Bh	4.6	100001	21h	9	110111	37h	13.4			
5-0	VSHR	001100	0Ch	4.8	100010	22h	9.2	111000	38h	13.6			
		001101	0Dh	5	100011	23h	9.4	111001	39h	13.8			
		001110	0Eh	5.2	100100	24h	9.6	111010	3Ah	14			
		001111	0Fh	5.4	100101	25h	9.8	111011	3Bh	14.2			
		010000	10h	5.6	100110	26h	10	111100	3Ch	14.4			
		010001	11h	5.8	100111	27h	10.2	111101	3Dh	14.6			
		010010	12h	6	101000	28h	10.4	111110	3Eh	14.8			
		010011	13h	6.2	101001	29h	10.6	111111	3Fh	15			
		010100	14h	6.4	101010	2Ah	10.8						
		010101	15h	6.6	101011	2Bh	11						

OPTEN=1:enable step -0.1 voltage selection(2.4~15V) Internal VSHR power selection for Red LUT.

Bit	Name	Description							
		Internal VSHR power selection.							
		VSHR[7:0]		Voltage(V)	VSHR[7:0]		Voltage(V)	VSHR[7:0]		Voltage(V)
6-0	VSHR	10000000	80h	2.4	10101011	ABh	6.7	11010110	D6h	11
		10000001	81h	2.5	10101100	ACh	6.8	11010111	D7h	11.1
		10000010	82h	2.6	10101101	ADh	6.9	11011000	D8h	11.2
		10000011	83h	2.7	10101110	AEh	7	11011001	D9h	11.3
		10000100	84h	2.8	10101111	AFh	7.1	11011010	DAh	11.4
		10000101	85h	2.9	10110000	B0h	7.2	11011011	DBh	11.5
		10000110	86h	3	10110001	B1h	7.3	11011100	DCh	11.6
		10000111	87h	3.1	10110010	B2h	7.4	11011101	DDh	11.7
		10001000	88h	3.2	10110011	B3h	7.5	11011110	DEh	11.8
		10001001	89h	3.3	10110100	B4h	7.6	11011111	DFh	11.9
		10001010	8Ah	3.4	10110101	B5h	7.7	11100000	E0h	12
		10001011	8Bh	3.5	10110110	B6h	7.8	11100001	E1h	12.1
		10001100	8Ch	3.6	10110111	B7h	7.9	11100010	E2h	12.2
		10001101	8Dh	3.7	10111000	B8h	8	11100011	E3h	12.3
		10001110	8Eh	3.8	10111001	B9h	8.1	11100100	E4h	12.4
		10001111	8Fh	3.9	10111010	BAh	8.2	11100101	E5h	12.5
		10010000	90h	4	10111011	BBh	8.3	11100110	E6h	12.6
		10010001	91h	4.1	10111100	BCh	8.4	11100111	E7h	12.7
		10010010	92h	4.2	10111101	BDh	8.5	11101000	E8h	12.8
		10010011	93h	4.3	10111110	BEh	8.6	11101001	E9h	12.9
		10010100	94h	4.4	10111111	BFh	8.7	11101010	EAh	13
		10010101	95h	4.5	11000000	C0h	8.8	11101011	EBh	13.1
		10010110	96h	4.6	11000001	C1h	8.9	11101100	ECh	13.2
		10010111	97h	4.7	11000010	C2h	9	11101101	EDh	13.3
		10011000	98h	4.8	11000011	C3h	9.1	11101110	EEh	13.4
		10011001	99h	4.9	11000100	C4h	9.2	11101111	EFh	13.5
		10011010	9Ah	5	11000101	C5h	9.3	11110000	F0h	13.6
		10011011	9Bh	5.1	11000110	C6h	9.4	11110001	F1h	13.7
		10011100	9Ch	5.2	11000111	C7h	9.5	11110010	F2h	13.8
		10011101	9Dh	5.3	11001000	C8h	9.6	11110011	F3h	13.9
		10011110	9Eh	5.4	11001001	C9h	9.7	11110100	F4h	14
		10011111	9Fh	5.5	11001010	CAh	9.8	11110101	F5h	14.1
		10100000	A0h	5.6	11001011	CBh	9.9	11110110	F6h	14.2
		10100001	A1h	5.7	11001100	CCh	10	11110111	F7h	14.3
		10100010	A2h	5.8	11001101	CDh	10.1	11111000	F8h	14.4
		10100011	A3h	5.9	11001110	CEh	10.2	11111001	F9h	14.5
		10100100	A4h	6	11001111	CFh	10.3	11111010	FAh	14.6
		10100101	A5h	6.1	11010000	D0h	10.4	11111011	FBh	14.7
		10100110	A6h	6.2	11010001	D1h	10.5	11111100	FCh	14.8
		10100111	A7h	6.3	11010010	D2h	10.6	11111101	FDh	14.9
		10101000	A8h	6.4	11010011	D3h	10.7	11111110	FEh	15
		10101001	A9h	6.5	11010100	D4h	10.8			
		10101010	AAh	6.6	11010101	D5h	10.9			

Note: VSH>VSHR

Restriction

8.1.3 R02H (POF): Power OFF Command

R02H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
POF	W	0	0	0	0	0	0	0	1	0	02H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ● After power off command, driver will power off base on power off sequence. ● After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N singal will rise from low to high. ● Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. ● SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.
Restriction	This command only active when BUSY_N = "1".

8.1.4R04H (PON): Power ON Command

R04H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PON	W	0	0	0	0	0	0	1	0	0	04H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ● After power on command, driver will power on base on power on sequence. ● After power on command, BUSY_N signal will drop from high to low. When finishing the power on sequence, BUSY_N signal will rise from low to high.
Restriction	This command only active when BUSY_N = "1".

8.1.5R06H (BTST): Booster Soft Start Command

R06H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
BTST	W	0	0	0	0	0	0	1	1	0	06H
1st Parameter	W	1	BT_PHA[7]	BT_PHA[6]	BT_PHA[5]	BT_PHA[4]	BT_PHA[3]	BT_PHA[2]	BT_PHA[1]	BT_PHA[0]	17h
2nd Parameter	W	1	BT_PHB[7]	BT_PHB[6]	BT_PHB[5]	BT_PHB[4]	BT_PHB[3]	BT_PHB[2]	BT_PHB[1]	BT_PHB[0]	17h
3rd Parameter	W	1	-	-	BT_PHC[5]	BT_PHC[4]	BT_PHC[3]	BT_PHC[2]	BT_PHC[1]	BT_PHC[0]	17h

Description	-The command define as follows: 1st Parameter:

Bit	Name	Description
2-0	Driving strength of phase A	000: period 1 001: period 2 010: period 3 011: period 4 100: period 5 101: period 6 110: period 7 111: period 8 (default)

5-3		000: Strength 1 001: Strength 2 010: Strength 3 (default) 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8
7-6	Soft start period of phase A	00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS

2nd Parameter:

Bit	Name	Description
2-0	Driving strength of phase B	000: period 1 001: period 2 010: period 3 011: period 4 100: period 5 101: period 6 110: period 7 111: period 8 (default)
5-3		000: Strength 1 001: Strength 2 010: Strength 3 (default) 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8
7-6	Soft start period of phase B	00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS

3rd Parameter:

Bit	Name	Description
2-0	Minimum OFF time setting of GDR in phase C	000: period 1 001: period 2 010: period 3 011: period 4 100: period 5 101: period 6 110: period 7 111: period 8 (default)
5-3	Driving strength of phase C	000: Strength 1 001: Strength 2 010: Strength 3 (default) 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8

Restriction	

8.1.6 R07H (DSLP): Deep Sleep Command

R07H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSLP	W	0	0	0	0	0	0	1	1	1	07H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset. The only one parameter is a check code, the command would be excited if check code = 0xA5.
Restriction	This command only active when BUSY_N = "1".

8.1.7 R10H (DTM1): Data Start transmission 1 Register

R10H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM1	W	0	0	0	0	1	0	0	0	0	10H
1st Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
2nd Parameter	W	1									00h
…	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "OLD" data to SRAM. In B/W/Red mode, this command writes "B/W" data to SRAM. In Program mode, this command writes "OTP" data to SRAM for programming.
Restriction	

8.1.8 R11H (DSP): Data Stop Command

R11H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSP	W	0	0	0	0	1	0	0	0	1	11H
1st Parameter	R	1	Data_flag	-	-	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■ While finished the data transmitting, user must send this command to driver and read Data_flag information. 1st Parameter: Bit / Name / Description 7 / Data_flag / 0: Driver didn't receive all the data. 1: Driver has already received all of the one frame data. After "Data Start" (10h) or "Data Stop" (11h) commands and when data_flag=1, BUSY_N signal will become "0" and the refreshing of panel starts.
Restriction	This command only actives when BUSY_N = "1".

8.1.9 R12H (DRF): Display Refresh Command

R12H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DRF	W	0	0	0	0	1	0	0	1	0	12H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■ While users send this command, driver will refresh display (data/VCOM) base on SRAM data and LUT. After display refresh command, BUSY_N signal will become "0".
Restriction	This command only actives when BUSY_N = "1"

8.1.10 R13H (DTM2): Data Start transmission 2 Register

R13H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM2	W	0	0	0	0	1	0	0	1	1	13H
1st Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
2nd Parameter	W	1									00h
…	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "NEW" data to SRAM. In B/W/Red mode, this command writes "RED" data to SRAM.
Restriction	

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8.1.11 R20H (LUTC): LUT for Vcom

R20H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTC	W	0	0	0	1	0	0	0	0	0	20H
1st Parameter	W	1	Group repeat times[7:0]								00h
2nd Parameter	W	1	level selection1-1 [1:0]		Frame Number1-1 [5:0]						00h
3rd Parameter	W	1	level selection1-2 [1:0]		Frame Number1-2 [5:0]						00h
4th Parameter	W	1	level selection2-1 [1:0]		Frame Number2-1 [5:0]						00h
5th Parameter	W	1	level selection2-2 [1:0]		Frame Number2-2 [5:0]						00h
6th Parameter	W	1	State 1 repeat times[7:0]								00h
7th Parameter	W	1	State 2 repeat times[7:0]								00h
8th~14th Parameter	W	1	2nd group								00h
15th~21th Parameter	W	1	3rd group								00h
…	W	1	4th~7th group								00h
50th~56th Parameter	W	1	8th group								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-This command builds up VCOM Look-Up Table (LUT). This LUT includes 8 kinds of groups; each group is of 7 bytes, as above. Each Group is divided to 2 states and "Group Repeat Number". Each state made up 2 phases. And each phase is combined with "Repeat Number", "Level selection", and "Frame Number". Byte 2: Group repeat times. Byte 3-6: [D7:D6]: Level selection of each phase. [D5:D0]: Frame number of each phase (state1 & state 2) Bytes 7~8: state repeat times (state1 & state 2) Bytes 2,9,16,23,30,…: Group repeat times 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 times Bytes 3~6,10~13,17~20, 24~27, 31~ 34 Level Selection. [D7:D6]: Level Selection. 00b:-VCM_DC 01b:VSH-VCM_DC(VCOMH) 10b:VSL -VCM_DC(VCOML) 11b:Floating [D5:D0]: Number of frames (state1 & state 2) 00 0000b~11 1111b: 0~63 times Bytes 7~8,14~15,21~22,28~29,35~36,…: :repeat times (state1 & state 2) 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 frames If BWR=0(BWR mode),all 8 groups are used. If BWR=1(BW mode),only 6 groups are used.
Restriction	

8.1.12 R22H (LUTBW/LUTR): Black to White LUT or Red LUT Register

R22H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTBW/LUTR	W	0	0	0	1	0	0	0	1	0	22H
1st Parameter	W	1	Group repeat times[7:0]								00h
2nd Parameter	W	1	level selection1-1 [1:0]		Frame Number1-1 [5:0]						00h
3rd Parameter	W	1	level selection1-2 [1:0]		Frame Number1-2 [5:0]						00h
4th Parameter	W	1	level selection2-1 [1:0]		Frame Number2-1 [5:0]						00h
5th Parameter	W	1	level selection2-2 [1:0]		Frame Number2-2 [5:0]						00h
6th Parameter	W	1	State 1 repeat times[7:0]								00h
7th Parameter	W	1	State 2 repeat times[7:0]								00h
8th~14th Parameter	W	1	2nd group								00h
15th~21th Parameter	W	1	3rd group								00h
…	W	1	4th~7th group								00h
50th~56th Parameter	W	1	8th group								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	This command builds Look-up Table for LUTBW / LUTR. This LUT includes 8 kinds of groups; each group is of 7 bytes, as above. Each Group is divided to 2 states and "Group Repeat Number". Each state made up 2 phases. And each phase is combined with "Repeat Number", "Level selection", and "Frame Number". Byte 2:Group repeat times. Byte 3-6: [D7:D6]: Level selection of each phase. [D5:D0]: Frame number of each phase (state1 & state 2) Bytes 7~8: state repeat times (state1 & state 2) Bytes 2,9,16,23,30,…: Group repeat times 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 times Bytes 3~6,10~13,17~20, 24~27, 31~ 34 Level Selection. [D7:D6]: Level Selection. 00b: GND 01b: VSH 10b: VSL 11b: VSHR [D5:D0]: Number of frames (state1 & state 2) 00 0000b~11 1111b: 0~63 times Bytes 7~8,14~15,21~22,28~29,35~36,…: :repeat times (state1 & state 2) 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 frames If BWR=0(BWR mode),all 8 groups are used. If BWR=1(BW mode),only 6 groups are used.
Restriction	

8.1.13 R23H (LUTWB/LUTW): White to Black LUT or White LUT Register

R23H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTWB/LUTW	W	0	0	0	1	0	0	0	1	1	23H
1st Parameter	W	1	Group repeat times[7:0]								00h
2nd Parameter	W	1	level selection1-1 [1:0]		Frame Number1-1 [5:0]						00h
3rd Parameter	W	1	level selection1-2 [1:0]		Frame Number1-2 [5:0]						00h
4th Parameter	W	1	level selection2-1 [1:0]		Frame Number2-1 [5:0]						00h
5th Parameter	W	1	level selection2-2 [1:0]		Frame Number2-2 [5:0]						00h
6th Parameter	W	1	State 1 repeat times[7:0]								00h
7th Parameter	W	1	State 2 repeat times[7:0]								00h
8th~14th Parameter	W	1	2nd group								00h
15th~21th Parameter	W	1	3rd group								00h
…	W	1	4th~7th group								00h
50th~56th Parameter	W	1	8th group								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	- This command builds Look-up Table for LUTWB/LUTW. This LUT includes 8 kinds of groups; each group is of 7 bytes, as above. Each Group is divided to 2 states and "Group Repeat Number". Each state made up 2 phases. And each phase is combined with "Repeat Number", "Level selection", and "Frame Number". Byte 2:Group repeat times. Byte 3-6: [D7:D6]: Level selection of each phase. [D5:D0]: Frame number of each phase (state1 & state 2) Bytes 7~8: state repeat times (state1 & state 2) Bytes 2,9,16,23,30,…: Group repeat times 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 times Bytes 3~6,10~13,17~20, 24~27, 31~ 34 Level Selection. [D7:D6]: Level Selection. 00b: GND 01b: VSH 10b: VSL 11b: VSHR [D5:D0]: Number of frames (state1 & state 2) 00 0000b~11 1111b: 0~63 times Bytes 7~8,14~15,21~22,28~29,35~36,…: :repeat times (state1 & state 2) 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 frames If BWR=0(BWR mode),all 8 groups are used. If BWR=1(BW mode),only 6 groups are used.
Restriction	-

8.1.14 R24H (LUTBB/LUTB): Black to Black LUT or Black LUT Register

R24H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTBB/LUTB	W	0	0	0	1	0	0	1	0	0	24H
1st Parameter	W	1	Group repeat times[7:0]								00h
2nd Parameter	W	1	level selection1-1 [1:0]		Frame Number1-1 [5:0]						00h
3rd Parameter	W	1	level selection1-2 [1:0]		Frame Number1-2 [5:0]						00h
4th Parameter	W	1	level selection2-1 [1:0]		Frame Number2-1 [5:0]						00h
5th Parameter	W	1	level selection2-2 [1:0]		Frame Number2-2 [5:0]						00h
6th Parameter	W	1	State 1 repeat times[7:0]								00h
7th Parameter	W	1	State 2 repeat times[7:0]								00h
8th~14th Parameter	W	1	2nd group								00h
15th~21th Parameter	W	1	3rd group								00h
…	W	1	4th~7th group								00h
50th~56th Parameter	W	1	8th group								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	- This command builds Look-up Table for LUTBB/LUTB. This LUT includes 8 kinds of groups; each group is of 7 bytes, as above. Each Group is divided to 2 states and "Group Repeat Number". Each state made up 2 phases. And each phase is combined with "Repeat Number", "Level selection", and "Frame Number". Byte 2: Group repeat times. Byte 3-6: [D7:D6]: Level selection of each phase. [D5:D0]: Frame number of each phase (state1 & state 2) Bytes 7~8: state repeat times (state1 & state 2) Bytes 2,9,16,23,30,…: Group repeat times 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 times Bytes 3~6,10~13,17~20, 24~27, 31~ 34 Level Selection. [D7:D6]: Level Selection. 00b: GND 01b: VSH 10b: VSL 11b: VSHR [D5:D0]: Number of frames (state1 & state 2) 00 0000b~11 1111b: 0~63 times Bytes 7~8,14~15,21~22,28~29,35~36,…: :repeat times (state1 & state 2) 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 frames If BWR=0(BWR mode),all 8 groups are used. If BWR=1(BW mode),only 6 groups are used.
Restriction	

Note: All LUTs are independent of each other and could be deal with separately. If waveform time is different for each LUT, IC would select longest LUT as refresh time and fill 0 (GND) to remaining refresh time for other LUT.

8.1.15 R30H (PLL): PLL Control Register

R30H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PLL	W	0	0	0	1	1	0	0	0	0	30H
1st Parameter	W	1	-	-	M[2:0]			N[2:0]			3Ch

NOTE: "-" Don't care, can be set to VDD or GND level

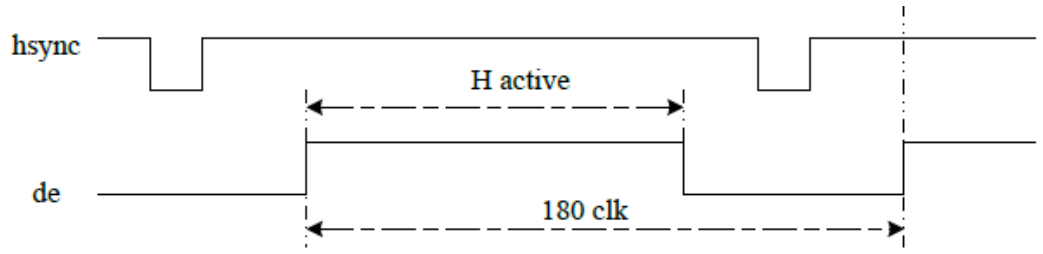
Description

-The command defines as:
The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

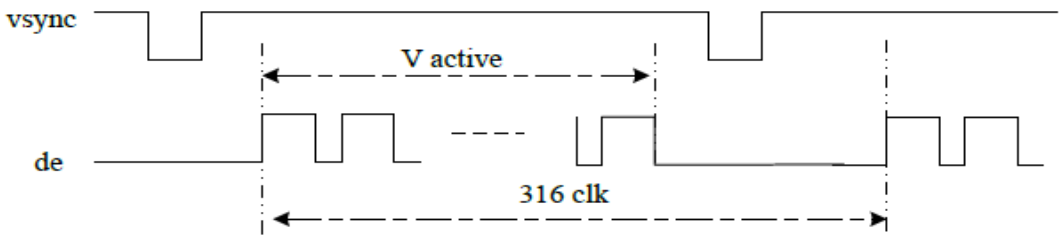
M	N	Frame rate	M	N	Frame rate	M	N	Frame rate	M	N	Frame rate
1	1	29HZ	3	1	86HZ	5	1	150HZ	7	1	200HZ
	2	14HZ		2	43HZ		2	72HZ		2	100HZ
	3	10HZ		3	29HZ		3	48HZ		3	67HZ
	4	7HZ		4	21HZ		4	36HZ		4	50HZ
	5	6HZ		5	17HZ		5	29HZ		5	40HZ
	6	5HZ		6	14HZ		6	24HZ		6	33HZ
	7	4HZ		7	12HZ		7	20HZ		7	29HZ
2	1	57HZ	4	1	114HZ	6	1	171HZ			
	2	29HZ		2	57HZ		2	86HZ			
	3	19HZ		3	38HZ		3	57HZ			
	4	14HZ		4	29HZ		4	43HZ			
	5	11HZ		5	23HZ		5	34HZ			
	6	10HZ		6	19HZ		6	29HZ			
	7	8HZ		7	16HZ		7	24HZ			

Remark

-Horizental



-Vertical



Restriction

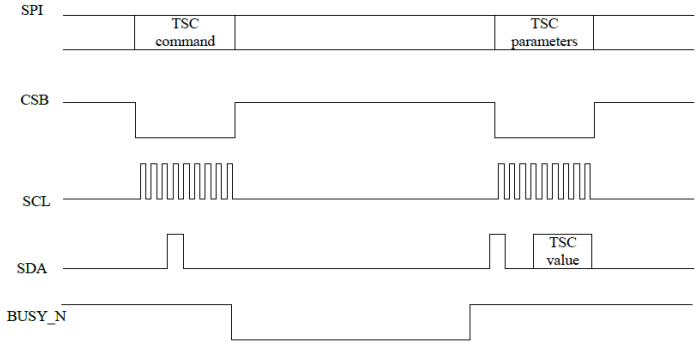
8.1.16 R40H (TSC): Temperature Sensor Command

R40H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	0	0	40H
1st Parameter	R	1	D10/TS[9]	D9/TS[8]	D8/TS[7]	D7/TS[6]	D6/TS[5]	D5/TS[4]	D4/TS[3]	D3/TS[2]	-
2nd Parameter	R	1	D2/TS[1]	D1/ TS[0]	D0	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command define as follows:
This command indicates the temperature value.
If R41H(TSE) bit7 set to 0, this command reads internal temperature sensor value.
If R41H(TSE) bit7 set to 1, this command reads external (LM75) temperature sensor value



TS[9:2]/D[10:3]	T(°C)	TS[9:2]/D[10:3]	T(°C)	TS[9:2]/D[10:3]	T(°C)
11100111	-25	00000000	0	00011001	25
11101000	-24	00000001	1	00011010	26
11101001	-23	00000010	2	00011011	27
11101010	-22	00000011	3	00011100	28
11101011	-21	00000100	4	00011101	29
11101100	-20	00000101	5	00011110	30
11101101	-19	00000110	6	00011111	31
11101110	-18	00000111	7	00100000	32
11101111	-17	00001000	8	00100001	33
11110000	-16	00001001	9	00100010	34
11110001	-15	00001010	10	00100011	35
11110010	-14	00001011	11	00100100	36
11110011	-13	00001100	12	00100101	37
11110100	-12	00001101	13	00100110	38
11110101	-11	00001110	14	00100111	39
11110110	-10	00001111	15	00101000	40
11110111	-9	00010000	16	00101001	41
11111000	-8	00010001	17	00101010	42
11111001	-7	00010010	18	00101011	43
11111010	-6	00010011	19	00101100	44
11111011	-5	00010100	20	00101101	45
11111100	-4	00010101	21	00101110	46
11111101	-3	00010110	22	00101111	47
11111110	-2	00010111	23	00110000	48
11111111	-1	00011000	24	00110001	49

TS[1:0]	T(° C)
00	+0
01	+0.25
10	+0.5
11	+0.75

Restricti	This command only actives when BUSY_N = "1".

8.1.17 R41H (TSE): Temperature Sensor Calibration Register

R41H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSE	W	0	0	1	0	0	0	0	0	1	41H
1st Parameter	W	1	TSE	-	TO[5]	TO[4]	TO[3]	TO[2]	TO[1]	TO[0]	**00h**

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the driver IC temperature sensor enable and calibration function.
Reserve one temperature offset TO[3:0] for calibration
1. TO[3]: mean '+' or '-' , while 0 is '+' ; 1 is '-'
2. TO[2:0]: mean temperature offset value

Bit	Name	Description
3-0	TO[3:0]	Temperature level: 0000: +0℃ (default) 0001: +1℃ 0010: +2℃ 0011: +3℃ 0100: +4℃ 0101: +5℃ 0110: +6℃ 0111: +7℃ 1000: -8℃ 1001: -7℃ 1010: -6℃ 1011: -5℃ 1100: -4℃ 1101: -3℃ 1110: -2℃ 1111: -1℃
5-4	TO[5:4]	00: +0.0℃ (default) 01: +0.25℃ 10: +0.5℃ 11: +0.75℃
7	TSE	Internal temperature sensor enable 0: Internal temperature sensor enable.(default) 1: Internal temperature

Restriction: This command only actives after R04H(PON) or R05H(PMES)

8.1.18 R42H (TSW): Temperature Sensor Write Register

R42H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSW	W	0	0	1	0	0	0	0	1	0	42H
1st Parameter	W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
2nd Parameter	W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
3rd Parameter	W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command writes the temperature.

1st Parameter:

Bit	Name	Description
2-0	WATTR[2:0]	Pointer setting
5-3	WATTR[5:3]	User-defined address bits (A2, A1, A0)
7-6	WATTR[7:6]	I2C Write Byte Number 00: 1 byte (head byte only) 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1st parameter) 11: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

2nd Parameter:

Bit	Name	Description
7-0	WMSB[7:0]	MSByte of write-data to external temperature sensor

3nd Parameter:

Bit	Name	Description
7-0	WMSB[7:0]	LSByte of write-data to external temperature sensor

Restriction

This command only actives after R04H(PON) or R05H(PMES)

8.1.19 R43H (TSR): Temperature Sensor Read Register

R43H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	1	1	43H
1st Parameter	R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	-
2nd Parameter	R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description

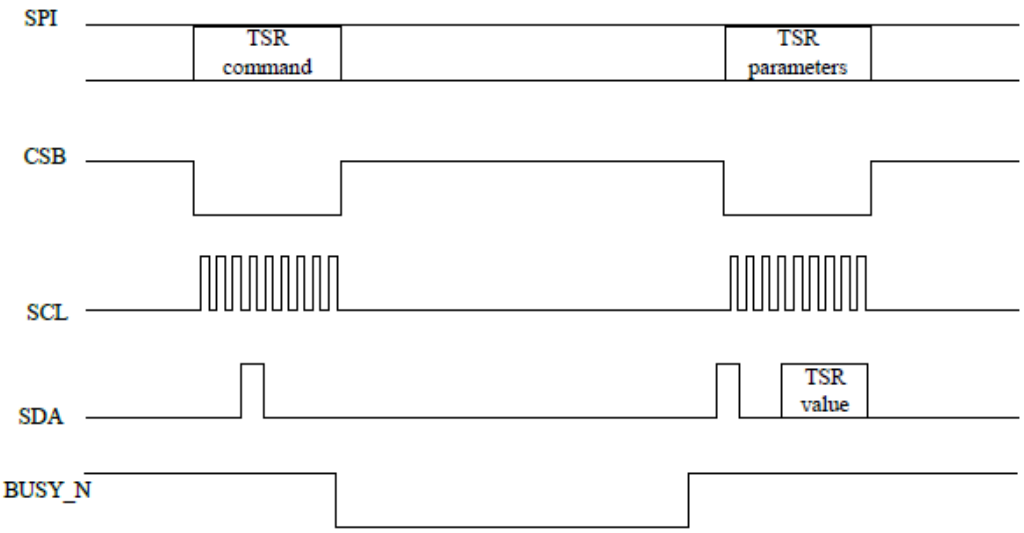
-The command defines as:
This command reads the temperature sensed by the temperature sensor.

1st Parameter:

Bit	Name	Description
7-0	RMSB[7:0]	MSByte of read-data from external temperature sensor

2nd Parameter:

Bit	Name	Description
7-0	RLSB[7:0]	LSByte of write-data from external temperature sensor



Restriction

This command only actives after R04H(PON) or R05H(PMES)

8.1.20 R50H (CDI): VCOM and DATA interval setting Register

R50H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CDI	W	0	0	1	0	1	0	0	0	0	50H
1st Parameter	W	1	VBD[1]	VBD[0]	DDX[1]	DDX[0]	CDI[3]	CDI[2]	CDI[1]	CDI[0]	D7h

NOTE: "-" Don't care, can be set to VDD or GND level

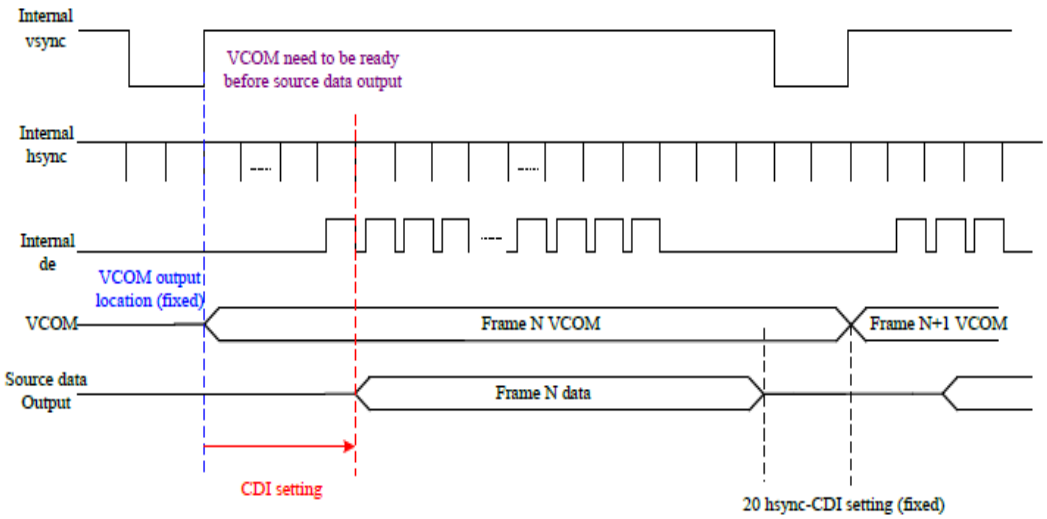
Description

-The command defines as:

1st Parameter:

CDI[1:0]: This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be keep (20hsync).

Bit	Name	Description
3-0	CDI[3:0]	Vcom and data interval 0000: 17 hsync 0001:16 hsync 0010:15 hsync 0011:14 hsync 0100:13 hsync 0101:12 hsync 0110:11 hsync 0111:10 hsync 1000:9 hsync 1001:8 hsync 1010:7 hsync 1011:6 hsync 1100:5 hsync 1101:4 hsync 1110:3 hsync 1111:2 hsync



VBD[1:0]: Border data selection.
B/W/Red mode(BWR=0)

Bit 4	Bit7-6	Description
DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTR
	10	LUTW
	11	LUTB
1 (default)	00	LUTB
	01	LUTW
	10	LUTR
	11 (default)	Floating

B/W mode (BWR=1)

Bit 4	Bit7-6	Description
DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTBW (1->0)
	10	LUTWB (0->1)
	11	Floating
1 (default)	00	Floating
	01	LUTWB (0->1)
	10	LUTBW (1->0)
	11	Floating

Border output voltage level: The level selection is based on mapping LUT data.
Level Selection:
00b: VCOM
01b: VSH
10b: VSL
11b: VSHR
DDX[1:0]: Data polarity
1. DDX[1] for RED data, DDX[0] for BW data in the B/W/Red mode
2. DDX[0] for B/W mode

B/W/Red mode(BWR=0)
DDX[1] is for RED data
DDX[0] is for B/W data

Bit 5-4	Description	
DDX[1:0]	Data (DTM2, DTM1)	LUT
00	00	LUTW
	01	LUTB
	10	LUTR
	11	LUTR
01 (default)	00	LUTB
	01	LUTW
	10	LUTR
	11	LUTR
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTB
11	00	LUTR
	01	LUTR
	10	LUTB
	11	LUTW

B/W mode (BWR=1)

DDX[1]=0 is for BW mode with NEW/OLD

Bit 5-4	Description	
DDX[1:0]	Data (DTM2, DTM1)	LUT
00	00	LUTWW (0->0)
	01	LUTBW(1->0)
	10	LUTWB(0->1)
	11	LUTBB(1->1)
01 (default)	00	LUTBB(0->0)
	01	LUTWB(1->0)
	10	LUTBW(0->1)
	11	LUTWW(1->1)

DDX[1]=1 is for BW mode without NEW/OLD

Bit 5-4	Description	
DDX[1:0]	Data (DTM2)	LUT
10	0	LUTBW(1->0)
	1	LUTWB(0->1)
11	0	LUTWB(0->1)
	1	LUTBW(1->0)

Restriction

8.1.21 R60H (TCON): TCON setting

R60H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TCON	W	0	0	1	1	0	0	0	0	0	60H
1st Parameter	W	1	S2G[3]	S2G[2]	S2G[1]-	S2G[0]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	22h

NOTE: "-" Don't care, can be set to VDD or GND level

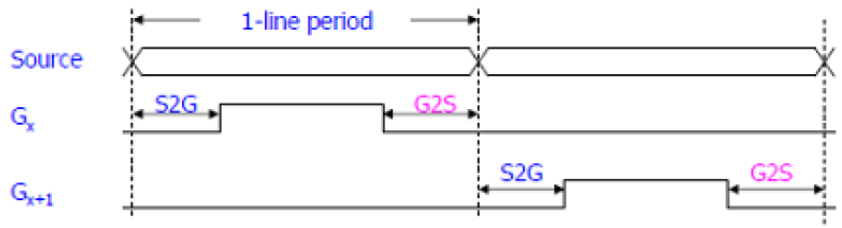
Description

- The command define Non-overlap period of gate and source as below:

1st Parameter:

Bit	Name	Description
7-0	S2G[3:0] G2S[3:0]	0000: 4 clock 0001: 8 clock 0010: 12 clock (default) 0011:16 clock 0100: 20 clock 0101: 24 clock 0110: 28 clock 0111: 32 clock 1000: 36 clock 1001: 40 clock 1010: 44 clock 1011: 48 clock 1100: 52 clock 1101: 56 clock 1110: 60 clock 1111: 64 clock

Period=660ns



Restriction

8.1.22 R61H (TRES): Resolution setting

R61H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TRES	W	0	0	1	1	0	0	0	0	1	61H
1st Parameter	W	1	HRES[7]	HRES[6]	HRES[5]	HRES[4]	HRES[3]	-	-	-	00h
2nd Parameter	W	1								VRES[8]	00h
3th Parameter	W	1	VRES[7]	VRES[6]	VRES[5]	VRES[4]	VRES[3]	VRES[2]	VRES[1]	VRES[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: When using register: Horizontal display resolution(source) = HRES Vertical display resolution(gate) = VRES Channel disable calculation: GD : First G active = G0; LAST active GD= first active +VRES[8:0] -1 SD : First active channel: =S0 ; LAST active SD= first active +HRES[7:3]*8-1 EX :128X272 GD: First G active = G0 LAST active GD= 0+272-1= 271; (G271) SD : First active channel: =S0 LAST active SD=0+16*8-1=127; (S127) Note : Only supports source 176.ch for source 160ch. above
Restriction	

8.1.23 R82H (VDCS): VCOM_DC Setting Register

R82H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VDCS	W	0	1	0	0	0	0	0	1	0	82H
1st Parameter	W	1	-	-	VDCS[5]	VDCS [4]	VDCS [3]	VDCS [2]	VDCS [1]	VDCS [0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description --The command defines as:

This command set the VCOM DC value. Driver will base on this value for VCM_DC.

1st Parameter:

Bit	Name	Function
5-0	VDCS[5:0]	VCOM value

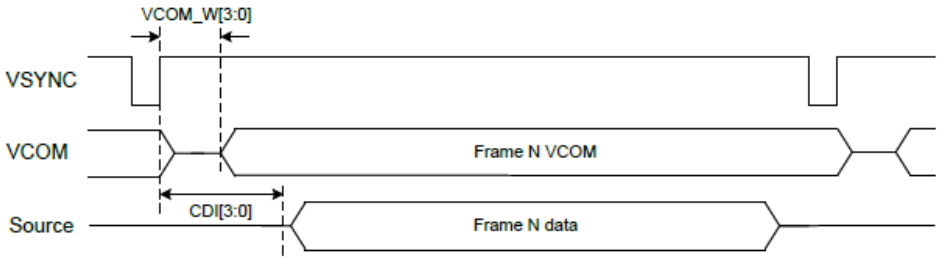
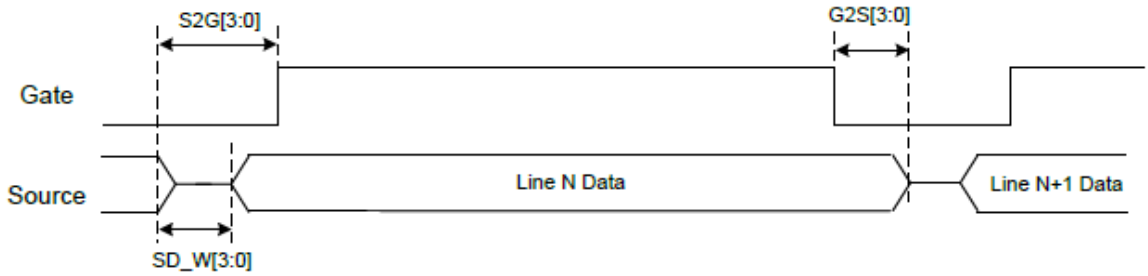
VCOM[5:0]		Voltage (V)	VCOM[5:0]		Voltage (V)	VCOM[5:0]		Voltage (V)
000000	00h	-0.1	010100	14h	-1.1	101000	28h	-2.1
000001	01h	-0.15	010101	15h	-1.15	101001	29h	-2.15
000010	02h	-0.2	010110	16h	-1.2	101010	2Ah	-2.2
000011	03h	-0.25	010111	17h	-1.25	101011	2Bh	-2.25
000100	04h	-0.3	011000	18h	-1.3	101100	2Ch	-2.3
000101	05h	-0.35	011001	19h	-1.35	101101	2Dh	-2.35
000110	06h	-0.4	011010	1Ah	-1.4	101110	2Eh	-2.4
000111	07h	-0.45	011011	1Bh	-1.45	101111	2Fh	-2.45
001000	08h	-0.5	011100	1Ch	-1.5	110000	30h	-2.5
001001	09h	-0.55	011101	1Dh	-1.55	110001	31h	-2.55
001010	0Ah	-0.6	011110	1Eh	-1.6	110010	32h	-2.6
001011	0Bh	-0.65	011111	1Fh	-1.65	110011	33h	-2.65
001100	0Ch	-0.7	100000	20h	-1.7	110100	34h	-2.7
001101	0Dh	-0.75	100001	21h	-1.75	110101	35h	-2.75
001110	0Eh	-0.8	100010	22h	-1.8	110110	36h	-2.8
001111	0Fh	-0.85	100011	23h	-1.85	110111	37h	-2.85
010000	10h	-0.9	100100	24h	-1.9	111000	38h	-2.9
010001	11h	-0.95	100101	25h	-1.95	111001	39h	-2.95
010010	12h	-1	100110	26h	-2	111010	3Ah	-3
010011	13h	-1.05	100111	27h	-2.05			

Restriction

8.1.24 RE3H (PWS): Power Saving Register

RE3H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWS	W	0	1	1	1	0	0	0	1	1	E3H
1st Parameter	W	1	VCOM_W[3:0]				SD_W[3:0]				00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	- This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters. VCOM_W: VCOM power saving width (unit = line period)  SD_W: Source power saving width (unit = 660nS) 
Restriction	

9.Reference Circuit

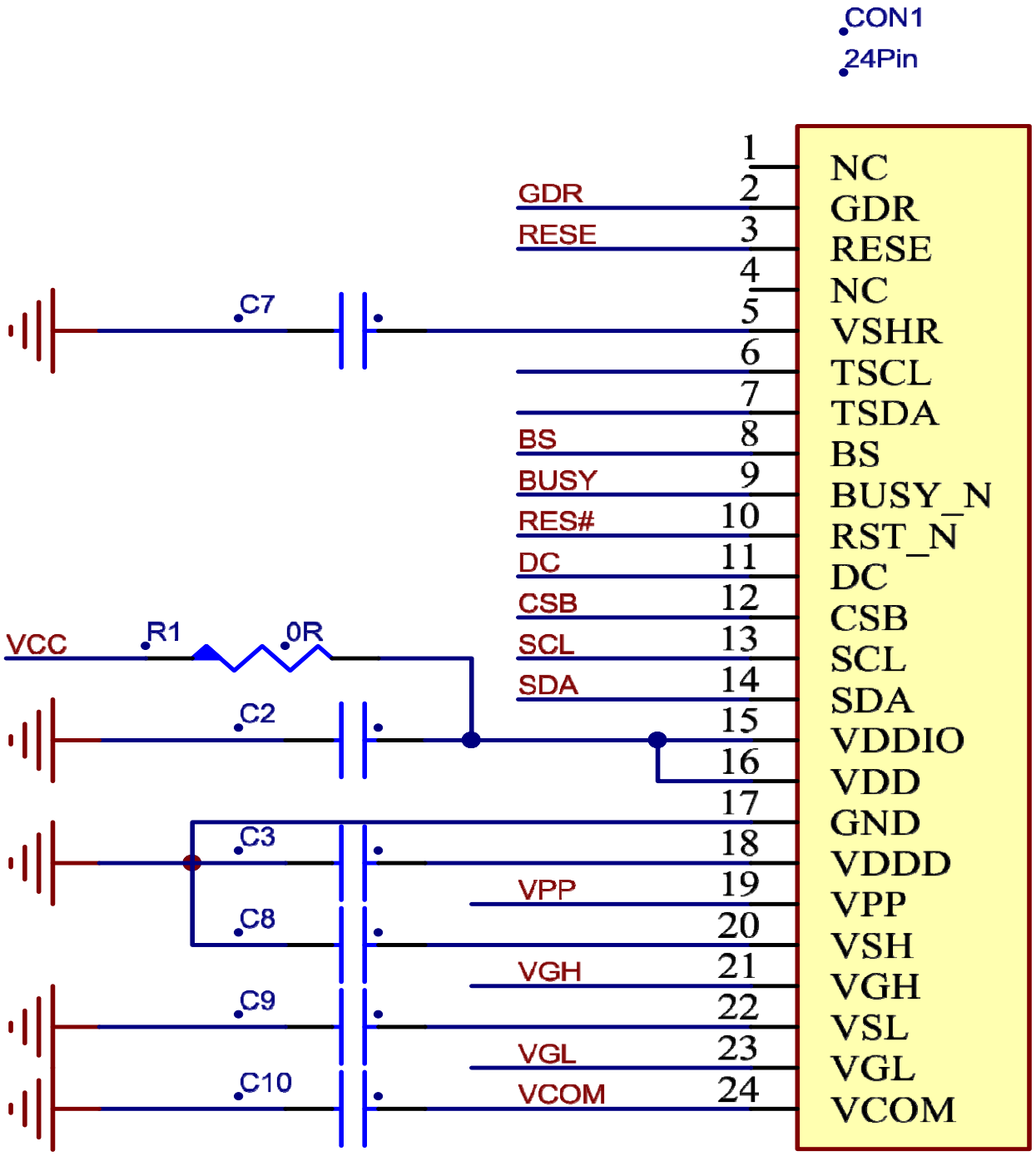


Figure. 9-1

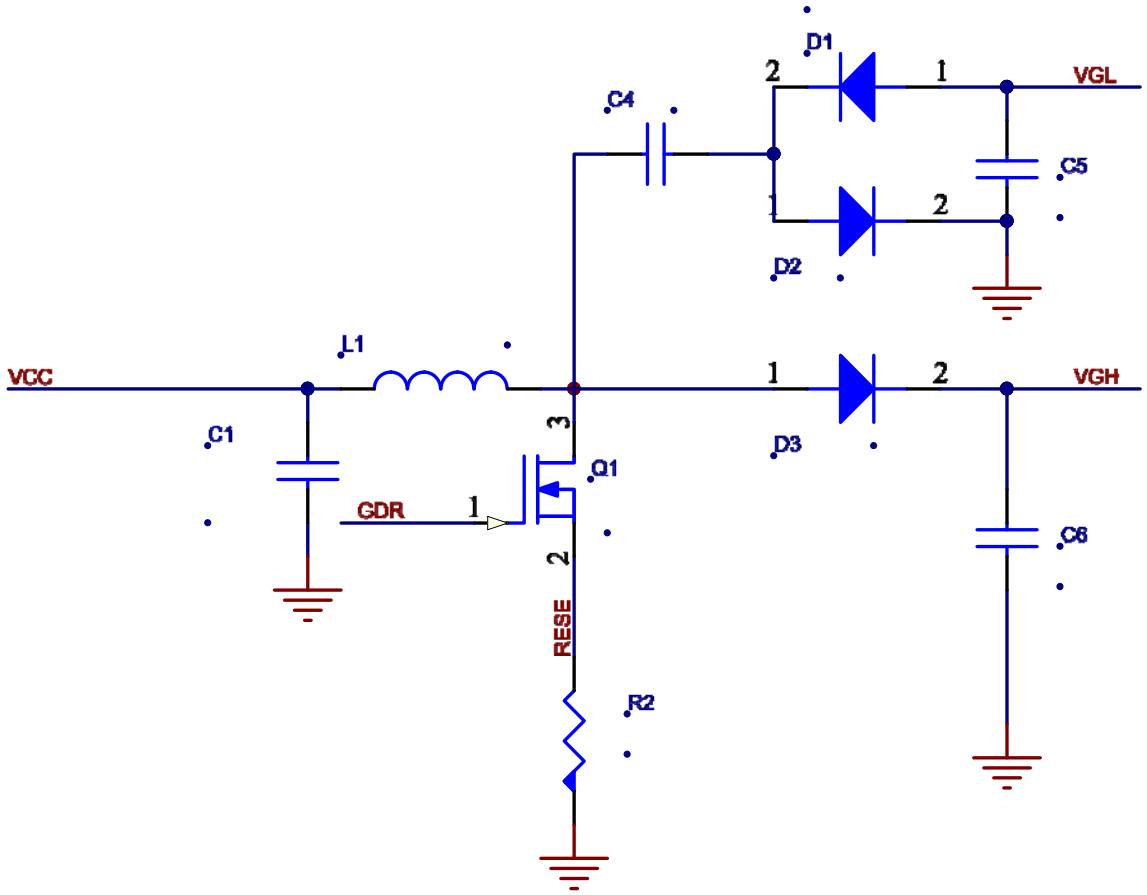


Figure. 9-2

Part Name	Value /requirement/Reference Part
C1—C3	1uF/0603;X5R/X7R;Voltage Rating: 25V
C4-C9	1uF/0603;X5R/X7R;Voltage Rating: 50V
C10	0.47uF/0603; X5R/X7R;Voltage Rating: 25V
D1—D3	MBR0530 1) Reverse DC voltage≥30V 2) Forward current≥500mA 3)Forward voltage≤430mV
R2	2.2 Ω/0603：1% variation
Q1	NMOS:Si1308EDL、Si1304BDL 1） Drain-Source breakdown voltage ≥30V 2）Gate-source threshold voltage ≤ 1.5V 3） Rds on≤ 2.1Ω @ Vgs=2.5V
L1	47uH/CDRH2D18、LDNP-470NC Maximum DC current~420mA Maximum DC resistance~650mΩ
CON24Pin	0.5mm ZIF Socket 24Pins,0.5mm pitch

10. ABSOLUTE MAXIMUM RATING

Table 10-1: Maximum Ratings

Symbol	Parameter	Rating	Unit	Humidity	Unit	Note
V_{CI}	Logic supply voltage	-0.5 to +6.0	V	-	-	
T_{OPR}	Operation temperature range	0 to 50	°C	35 to70	%	
Tttg	Transportation temperature range	-25 to 60	°C	-	-	Note10-2
Tstg	Storage condition	0 to 40	°C	35 to70	%	Maximum storage time: 5 years

Note 10-1:Maximum ratings are those values beyond which damages to the device may occur.
Functional operation should be restricted to the limits in the Electrical Characteristics chapter.
Note10-2: Tttg is the transportation condition, the transport time is within 10 days for -25℃~0℃ or 50℃~60℃

11. DC CHARACTERISTICS

The following specifications apply for: VSS=0V, VDD=3.3V, TOPR=25℃.

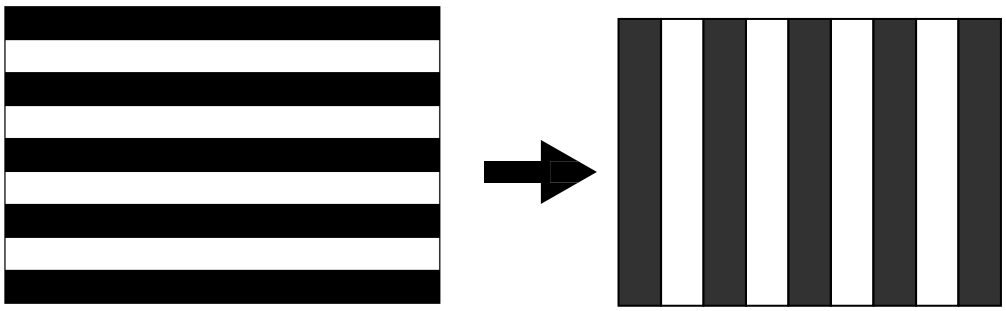
Table 13-1: DC Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
VDD	VDD operation voltage	-	2.5	3	3.3	V
VIH	High level input voltage	-	0.7xVIO	-	VIO-	V
VIL	Low level input voltage	-	GND-	-	0.3xVDD	V
VOH	High level output voltage	IOH = 400μA	VIO-0.4	-	-	V
VOL	Low level output voltage	IOL = -400μA	GND	-	GND+0.4	V
Iupdate	Module operating current	-	-	2	-	mA
Isleep	Deep sleep mode	VCI=3.3V	-	-	3	uA

- The Typical power consumption is measured using associated 25℃ waveform with following pattern transition: from horizontal scan pattern to vertical scan pattern. (Note 11-1)
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by XingTai.
- Vcom value will be OTP before in factory or present on the label sticker.

Note 11-1

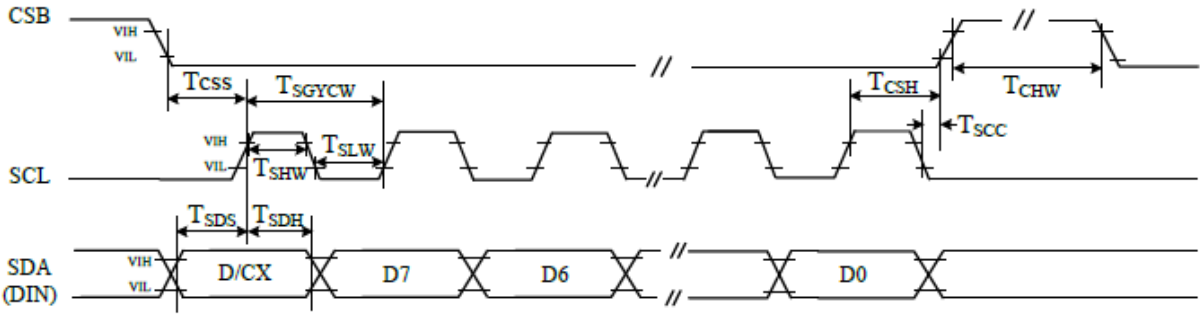
The Typical power consumption



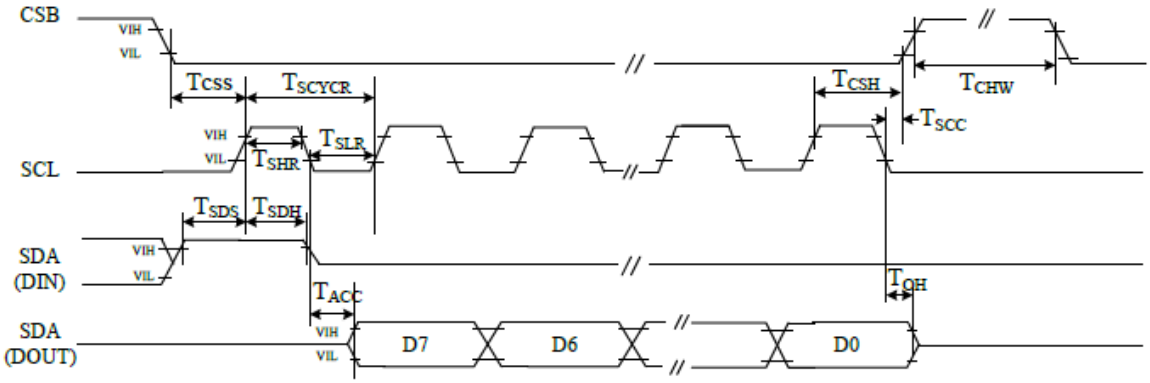
12. Serial Peripheral Interface Timing

The following specifications apply for: VSS=0V, VDD=2.5V to 3.6V, T_{OPR}=25℃

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
SERIAL COMMUNICATION						
CSB	TCSS	60			ns	Chip select setup time
	TCSH	65			ns	Chip select hold time
	TSCC	20			ns	Chip select CSB setup time
	TCHW	40			ns	Chip select setup time
SCL	TSCYCW	100			ns	Serial clock cycle (Write)
	TSHW	35			ns	SCL “H” pulse width (Write)
	TSLW	35			ns	SCL “L” pulse width (Write)
	TSCYCR	150			ns	Serial clock cycle (Read)
	TSHR	60			ns	SCL “H” pulse width (Read)
	TSLR	60			ns	SCL “L” pulse width (Read)
SDA (DIN) (DOUT)	TSDS	30			ns	Data setup time
	TSDH	30			ns	Data hold time
	TACC			50	ns	Access time
	TOH	15				Output disable time
D/C	TDCS	20				DC setup time
	TDCH	20				DC hold time



3 pin serial interface characteristics (write mode)



3 pin serial interface characteristics (read mode)

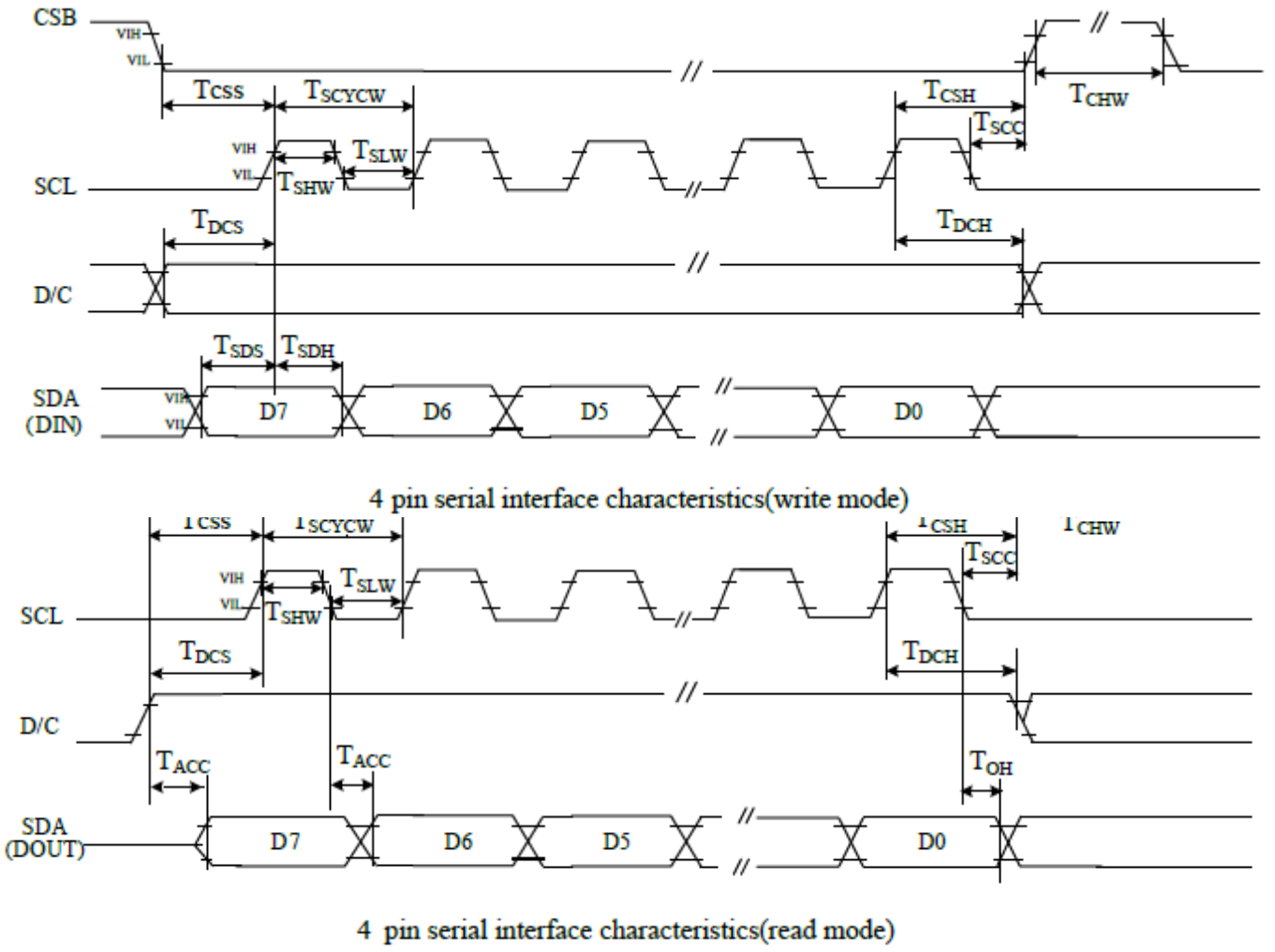


Figure 12-1 SPI interface timing

13. Power ON /OFF Sequence

In order to prevent IC fail in power on resetting, the power sequence must be followed as below.

Power ON Sequence

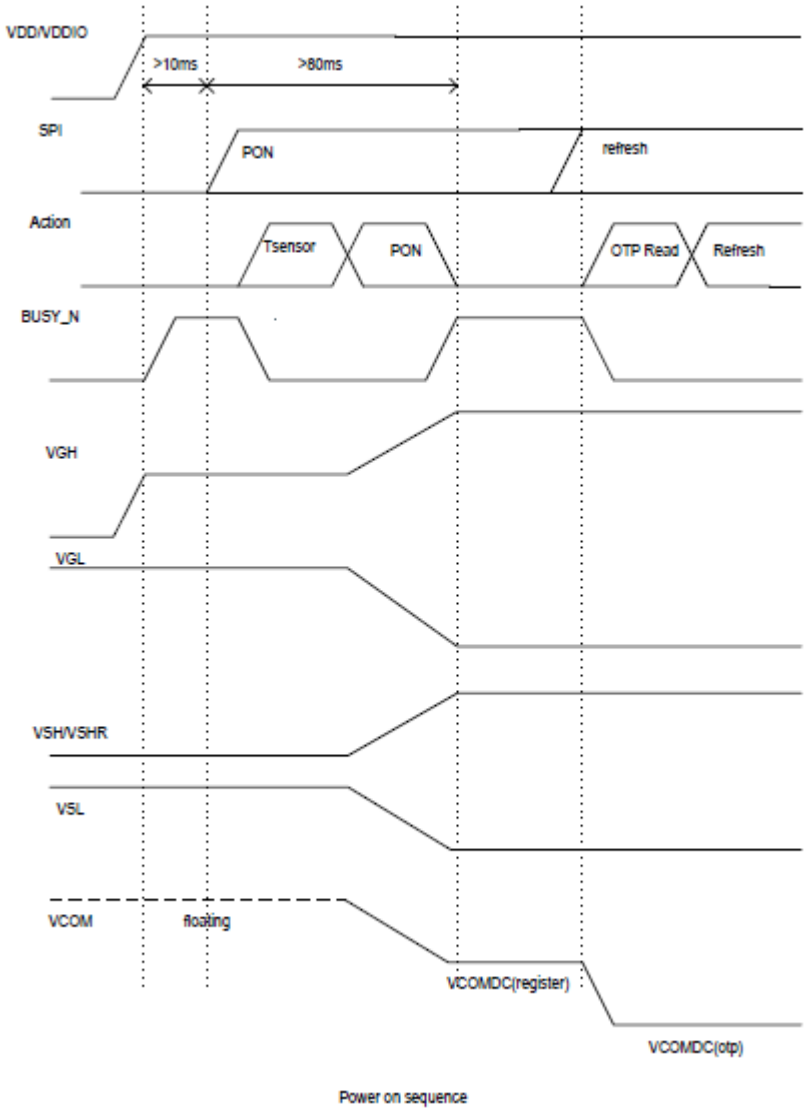


Figure 13-1: Power on sequence

Power OFF Sequence

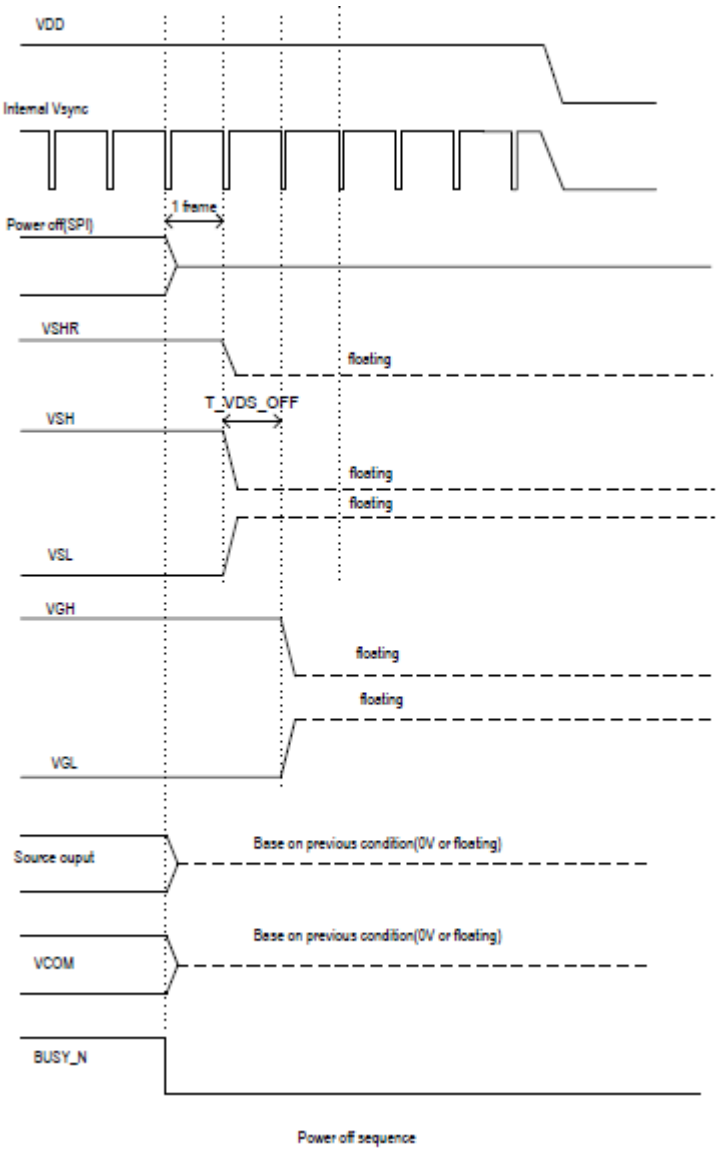


Figure 13-2: Power off sequence

DSLP sequence

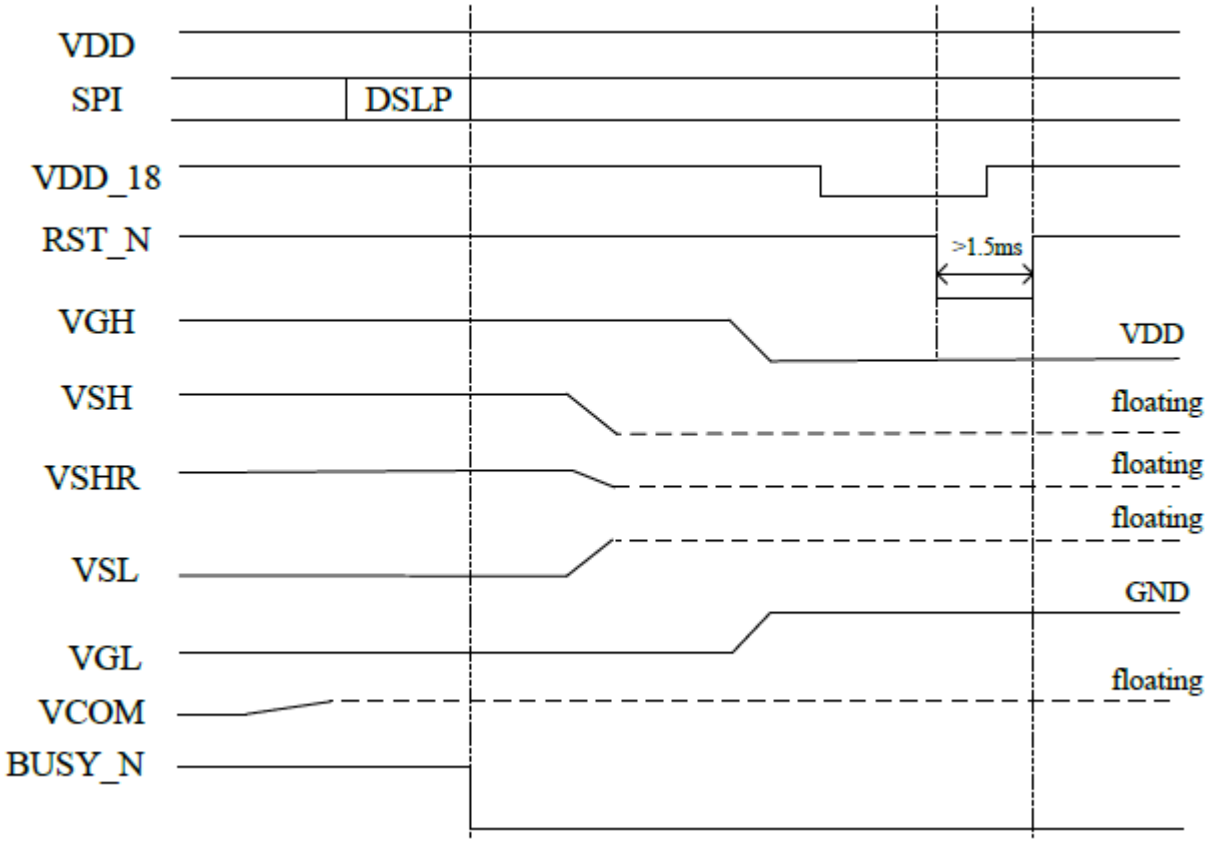


Figure 13-3: DSLP sequence

14. Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25℃	-	20	mAs	-
Deep sleep mode	-	25℃	-	3	uA	-

mAs=update average current×update time

15.Optical characteristics

15.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless
otherwise specified.

T=25℃

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 15-1
Gn	2Grey Level	-	-	KS+(WS-KS)×n(m-1)	-	L*	-
CR	Contrast Ratio	-	-	10	-	-	-
KS	Black State L* value	-	-	18	-	-	Note 15-1
	Black State a* value	-	-	0.2	-	-	Note 15-1
WS	White State L* value	-	-	67	-	-	Note 15-1
Panel	Image Update	Storage and transportation	-	Update the white screen	-	-	-
	Update Time	Operation	-	Suggest Updated once a day	-	-	-

WS: White state, KS : Dark state

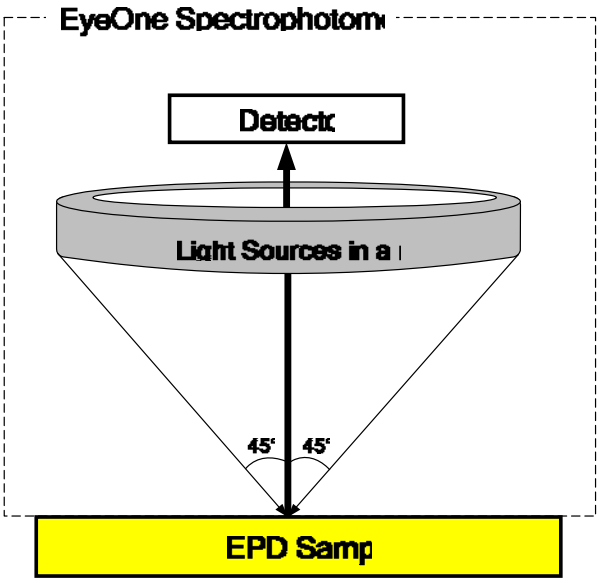
Note 15-1: Luminance meter : Eye - One Pro Spectrophotometer

Note 15-2: We guarantee display quality from 0℃～30℃ generally, If operation ambient temperature from 0℃～50℃,will offer special waveform by Xingtai.

15.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd):

CR = Rl/Rd

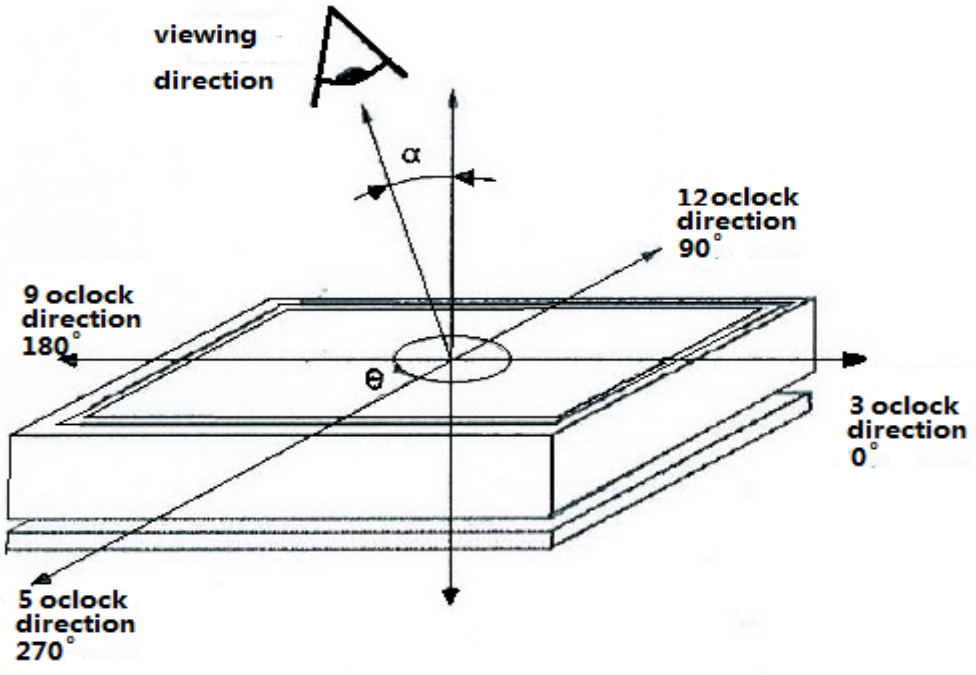


15.3 Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factor $_{\text{white board}}$ x (L_{center} / $L_{\text{white board}}$)

L_{center} is the luminance measured at center in a white area (R=G =B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



16. HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display module should be kept flat or fixed to a rigid, curved support with limited bending along the long axis. It should not be used for continual flexing and bending. Handle with care. Should the display break do not touch any material that leaks out. In case of contact with the leaked material then wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.
Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status	
Product specification	The data sheet contains final product specifications.

Limiting values
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.
Application information
Where application information is given, it is advisory and dose not form part of the specification.

Product Environmental certification
ROHS
REMARK
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

17. Reliability test

17.1 Reliability test items

	TEST	CONDITION	REMARK
1	High-Temperature Operation	T=40℃，RH=35%RH，For 240Hr	
2	Low-Temperature Operation	T = 0℃ for 240 hrs	
3	High-Temperature Storage	T=60℃ RH=35%RH For 240Hr	Test in white pattern
4	Low-Temperature Storage	T = -25℃ for 240 hrs	Test in white pattern
5	High Temperature, High-Humidity Operation	T=40℃，RH=90%RH，For 168Hr	
6	High Temperature, High-Humidity Storage	T=60℃，RH=80%RH，For 240Hr	Test in white pattern
7	Temperature Cycle	-25℃(30min)~70℃(30min)，100 Cycle	Test in white pattern
8	Package Vibration	1.04G,Frequency : 20~200Hz Direction : X,Y,Z Duration: 30 minutes in each direction	Full packed for shipment
9	Package Drop Impact	Drop from height of 100 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment
10	UV exposure Resistance	765 W/㎡ for 168hrs,40℃	
11	Electrostatic discharge	Machine model: +/-250V,0Ω,200pF	

Actual EMC level to be measured on customer application.

Note1：Stay white pattern for storage and non-operation test.

Note2：Operation is black/white pattern , hold time is 150S.

Note3：The function ,appearance, opticals should meet the requirements of the test before and after the test.

Note4：Keep testing after 2 hours placing at 20℃-25℃.

17.2 Product life time

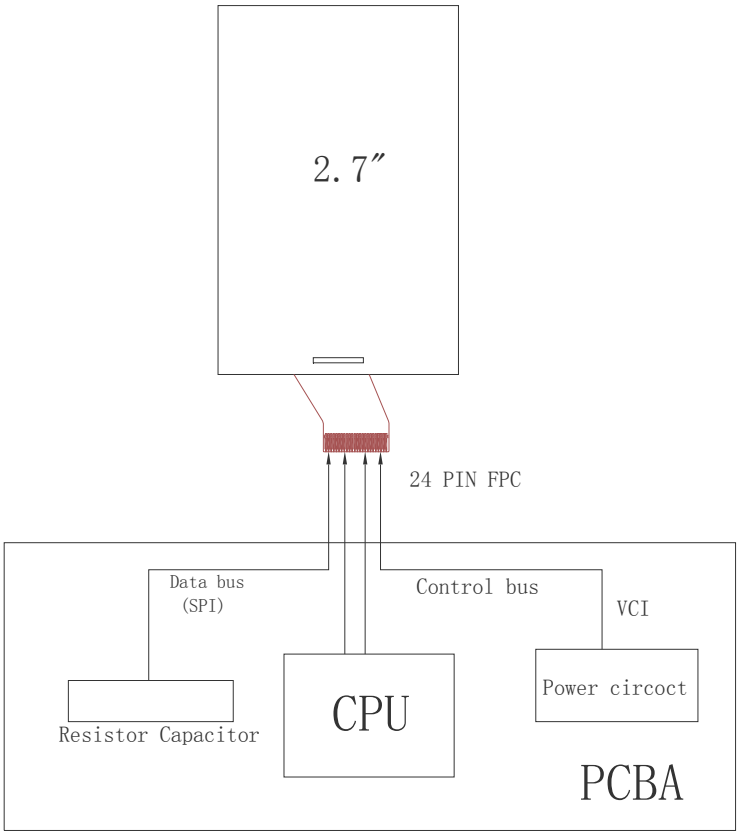
Reliability estimation testing with accelerated life-time theory would be demonstrated to provide confidence of EPD lifetime.

17.3 Product warranty

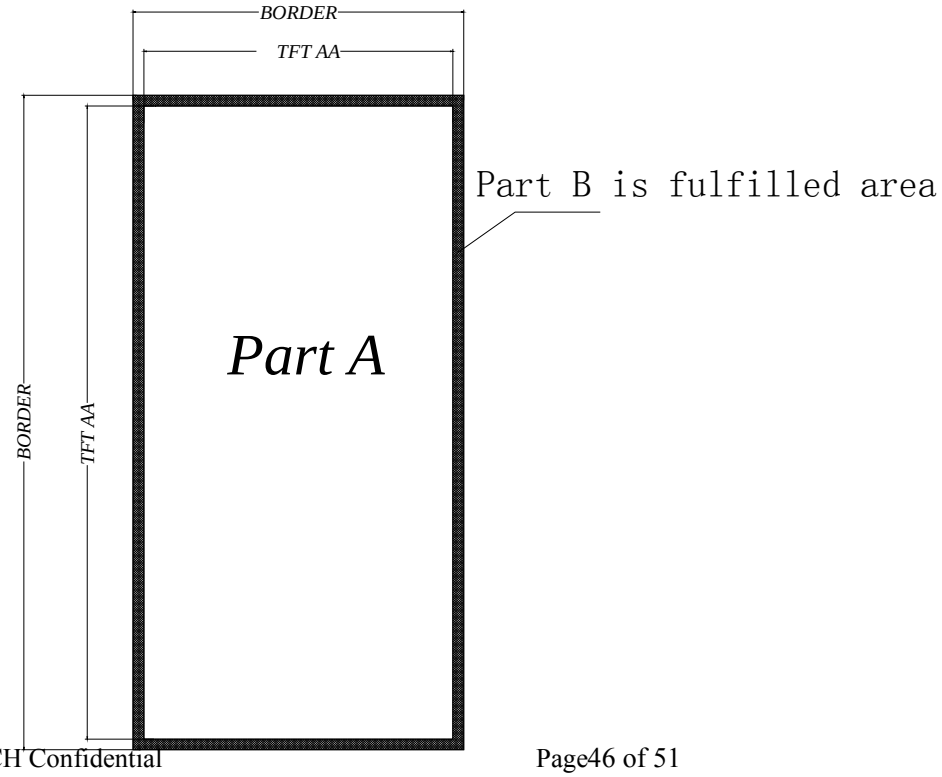
Warranty conditions have to be negotiated between Xingtai and individual customers.

Xingtai provides 12+1(one month delivery time) months warranty for all products which are purchased from Xingtai.

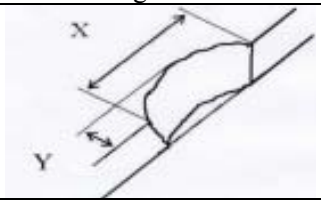
18. Block Diagram

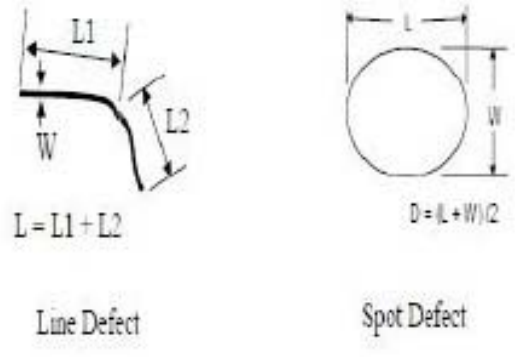


19. PartA/PartB specification



20. Point and line standard

Shipment Inspection Standard						
Equipment：Electrical test fixture, Point gauge						
Outline dimension	45.8(H)×70.42(V) ×0.9(D)	Unit：㎜	Part-A	Active area	Part-B	Border area
Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle
	19℃～25℃	55%±5%RH	800～1300Lux	300 ㎜	35Sec	
Defect type	Inspection method	Standard		Part-A		Part-B
Spot	Electric Display	D≤0.25 ㎜		Ignore		Ignore
		0.25 ㎜＜D≤0.4 ㎜		N≤4		Ignore
		D＞0.4 ㎜		Not Allow		Ignore
Display unwork	Electric Display	Not Allow		Not Allow		Ignore
Display error	Electric Display	Not Allow		Not Allow		Ignore
Scratch or line defect(include dirt)	Visual/Film card	L≤2 ㎜，W≤0.2 ㎜		Ignore		Ignore
		2.0mm＜L≤5.0mm，0.2＜W≤0.3mm,		N≤2		Ignore
		L＞5 ㎜，W＞0.3 ㎜		Not Allow		Ignore
PS Bubble	Visual/Film card	D≤0.2mm		Ignore		Ignore
		0.2mm≤D≤0.35mm & N≤4		N≤4		Ignore
		D＞0.35 mm		Not Allow		Ignore
Side Fragment	Visual/Film card	X≤6mm，Y≤0.4mm, Do not affect the electrode circuit (Edge chipping) X≤1mm，Y≤1mm, Do not affect the electrode circuit((Corner chipping) Ignore				
						
Remark	1.Cannot be defect & failure cause by appearance defect;					
	2.Cannot be larger size cause by appearance defect;					
	L=long W=wide D=point size N=Defects NO					



L=long W=wide D=point size

21.Barcode

21.1 Babel appearance

ABBBBBBBCC
DDDEEEFGGG

21.2 QR scanned information（Total 28 code number+ 2 blank spaces）

A BBBBBBB CC □ DDD EEE F GGG □ H III J KKK
① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑪

① A——The factory code
② BBBBBBB———Module name of EPD
③ CC———FPL model name
④ DDD———Date of production
⑤ EEE———Production lot
⑥ F———Separator
⑦ GGG———FPL Lot
⑧ H———Normal Lot
⑨ III———TFT、PS、EC.
⑩ J———IC
⑪ KKK———Serial NO.
□ blank spaces

22. Packing

Packing Spec

Sheet No :

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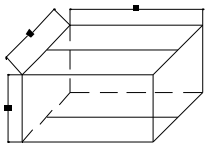
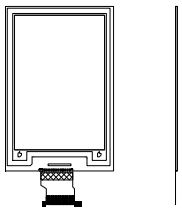
一, Package Type: Box

Box No	Holitech shipping box
Box size	515*322*170
Containment	252PCS



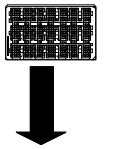
PRODUCT DRAWING



二,Inside package type:Plastic Tray unit: mm

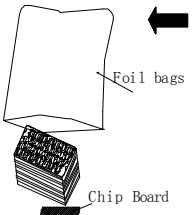
Plastic Tray	465*280*15	13 pcs
Anti-static foil bags	700*530*0.1	1 pcs
EPE(inside)	405.5*250.4*2	12 pcs
EPE(Up-Down)	485*145*10	2 pcs
EPE(Left-Right)	285*480*10	2 pcs
EPE(Front-back)	310*145*10	2 pcs
Chip board	500*306*5	2 pcs
Quantity/tray	21 pcs	
Tray number/sheet	12+1 Sheets	
Box	1	

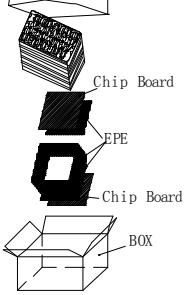
Step 1:
Material: Tray, EPE
Put the product in to the tray and keep the dispaly side up. Then put anti-static EPE in to each holes.



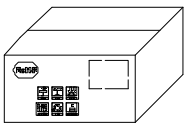
Step 2:
1) Must keep the angle 180 degree placed between the neighboring Plastic trays.
2) There are 12 layers product, total14*12=168pcs。
3) An empty Plastic tray intersects put on the top of the plastic trays.

Step 3:
1) In each case, put 2 bags of desiccant. then seal the trays with adhesive tapes.
2) Put the trays into foil bags.
3) heat seal the foil bags.





Step 4:
1)First put a chip board on the buttom of the box, then placed the down EPE, the left - right and front -back EPE.
2) Placed the sealed products into the box.
3) The last placed the up EPE on the top of the trays, and place a chip board on it.



Step 5:
1) Seal the box with adhensive tapes 。
2) Paste the lable onto the exterior box, and the lable can't cover the safety , transfer and RoSH sign。

Design	Z.Z.Q	Approve	H.Z.P	Confirm	X.X.M
Date	2020.11.20	Date	2020.11.20	Date	2020.11.20

Packing Spec

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The label outside the carton print as below

90.00

65.00

Label	
Customer Part No	
Customers Item No	A
MFG order No	B
MFG batch No	C
QTY	D
G.W	E
N.W	F
MFG Date	J
Carton No	
Remark	

NOTE:

1."A" Print customer Item No

2."B" Print customer Order No

3."C" Print MFG Batch No(Separate packing for different batch products. Mixed packing available for the odd number of different batch print all the batch NO&QTY accordingly if happened.

4."D"Print product qty

5."E"Print the G.W

6."F"Print the N.W

7."J"Print the MFG date

8.Before packing make sure the FPL batch ,item and qty are the same as which on the Final passed card.

Design	Z.Z.Q	Approve	H.Z.P	Confirm	X.X.M
Date	2020.11.20	Date	2020.11.20	Date	2020.11.20