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Version	A0	Page Number	1 of 40

Specification For HINK 2.9"EPD

Model NO.: HINK-E029A115

Product VER:A0

Customer Approval

Customer	
Approval By	
Date Of Approval	

It will be agreed by the receiver,if not sign back the Specification within 15days.

Prepared By	Checked By	Approval By
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Version	Content	Date	Producer
A0	New release	2020/11/19	Daisy Zhu



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1.General Description

HINK-E029A115 is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design. The 2.9" active area contains 128×296 pixels, and has 1-bit B/W full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

2.Features

- 128×296 pixels display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Low voltage detect for supply voltage
- High voltage ready detect for driving voltage
- Internal temperature sensor
- 10-byte OTP space for module identification
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C signal master interface to read external temperature sensor/ built-in temperature sensor

3.Application

Electronic Shelf Label System

4.Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.9	Inch	
Display Resolution	128(H)×296(V)	Pixel	Dpi:112
Active Area	29.06(H)×66.90(V)	mm	
Pixel Pitch	0.226×0.227	mm	
Pixel Configuration	Rectangle		
Outline Dimension	36.7(H)×79.0 (V) × 0.9(D)	mm	Without masking film
Weight	5±0.2	g	



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5. Mechanical Drawing of EPD module

Signature: _____ **Date:** _____

A1 confirmed

HSE FRONT VIEW

SIDE VIEW

BOTTOM VIEW

NOTES:

1. DISPLAY MODE 2.9" ARREY FOR EPD;
2. DRIVE IC: SSD1680
3. RESOLUTION: 128source X 296gate;
4. pixel size: 0.227mm X 0.226mm;
5. dpi: 112
6. Unspecified Tolerance: ±0.20;
7. Material conform to the ROHS standard
8. * as the focus control size

ALL UNITS: mm	DATE	MODEL NUMBER:	PROJECTION	SHEET: 1
DWN:		HINK-E029A115-A1(BW)		DATE: 2020.10.23
CHK:		CUSTOMER NO.		
APP:		P/N		

HOLITECH

JIANGXI HOLITECH TECHNOLOGY CO.,LTD.

REV.:	DESCRIPTION	DATE
A0	Previous A0	2020.09.04
A1	Modified RPL size	2020.10.23

PIN	SIGNAL
1	NC
2	GDR
3	RESR
4	NC
5	VSHD
6	TSCL
7	TSDA
8	BSI
9	BRISY
10	RES#
11	D/C#
12	CS#
13	SCI
14	SDA
15	VDDIO
16	YCI
17	VSS
18	VDD
19	VPP
20	VSHH
21	VGH
22	VSI
23	VGI
24	VCOM



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6.Input/Output Terminals

Pin #	Single	Description	Remark
1	NC	No connection and do not connect with other NC pins	Keep Open
2	GDR	N-Channel MOSFET Gate Drive Control	
3	RESE	Current Sense Input for the Control Loop	
4	NC	No connection and do not connect with other NC pins	Keep Open
5	VSH2	Positive Source driving voltage	
6	TSCL	I ² C Interface to digital temperature sensor Clock pin	
7	TSDA	I ² C Interface to digital temperature sensor Data pin.	
8	BS1	Bus selection pin	Note 6-5
9	BUSY	Busy state output pin	Note 6-4
10	RES #	Reset signal input.	Note 6-3
11	D/C #	Data /Command control pin	Note 6-2
12	CS #	The chip select input connecting to the MCU.	Note 6-1
13	SCL	Serial clock pin for interface.	
14	SDA	Serial data pin for interface.	
15	VDDIO	Power input pin for the Interface.	
16	VCI	Power Supply pin for the chip	
17	VSS	Ground (Digital)	
18	VDD	Core logic power pin	
19	VPP	Power Supply for OTP Programming	
20	VSH1	Positive Source driving voltage	
21	VGH	Power Supply pin for Positive Gate driving voltage and VSH	
22	VSL	Negative Source driving voltage	
23	VGL	Power Supply pin for Negative Gate driving voltage, VCOM and VSL	
24	VCOM	VCOM driving voltage	

Note 6-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication: only when CS# is pulled LOW.

Note 6-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Note 6-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 6-4: This pin (BUSY) is Busy state output pin. When Busy is High, the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin High when the driver IC is working such as:

- Outputting display waveform;



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- Communicating with digital temperature sensor

Note 6-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected.

7.MCU Interface

7.1 MCU interface selection

The HINK-E029A115 can support 3-wire/4-wire serial peripheral interface. In the Module, the MCU interface is pin selectable by BS1 pins shown in table 7-1.

Table 7-1: Interface pin assignment for different MCU interfaces

MCU Interface	Pin name					
	BS1	RES#	CS#	D/C#	SCL	SDA
4-wire serial peripheral interface (SPI)	L	RES#	CS#	D/C#	SCL	SDI
3-wire serial peripheral interface (SPI) - 9 bits SPI	H	RES#	CS#	L	SCL	SDI

Note:

(1) L is connected to VSS H is connected to VDDIO

7.2 MCU Serial Peripheral Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, D/C# and CS#. The control pins status in 4-wire SPI in writing command/data is shown in Table 7-2 and the write procedure 4-wire SPI is shown in table 7-2.

Table 7-2 : Control pins status of 4-wire SPI

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

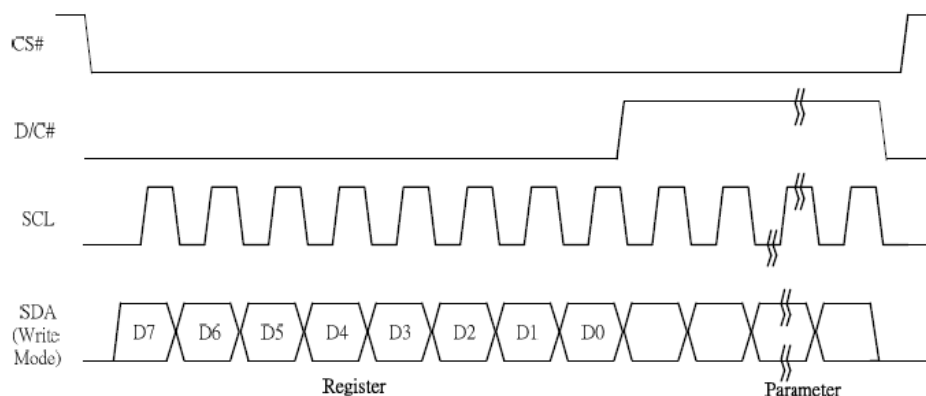
Note:

(1) L is connected to VSS and H is connected to VDDIO

(2) ↑ stands for rising edge of signal

(3) SDA (Write Mode) is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ...D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

Figure 7-1 Write procedure in 4-wire SPI mode





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In the read operation (Command 0x1B, 0x27, 0x2D, 0x2E, 0x2F, 0x35). After CS# is pulled low, the first byte sent is command byte, D/C# is pulled low. After command byte sent, the following byte(s) read are data byte(s), so D/C# bit is then pulled high. An 8-bit data will be shifted out on every clock falling edge. The serial data SDA bit shifting sequence is D7, D6, to D0 bit. Figure 6-2 shows the read procedure in 4-wire SPI.

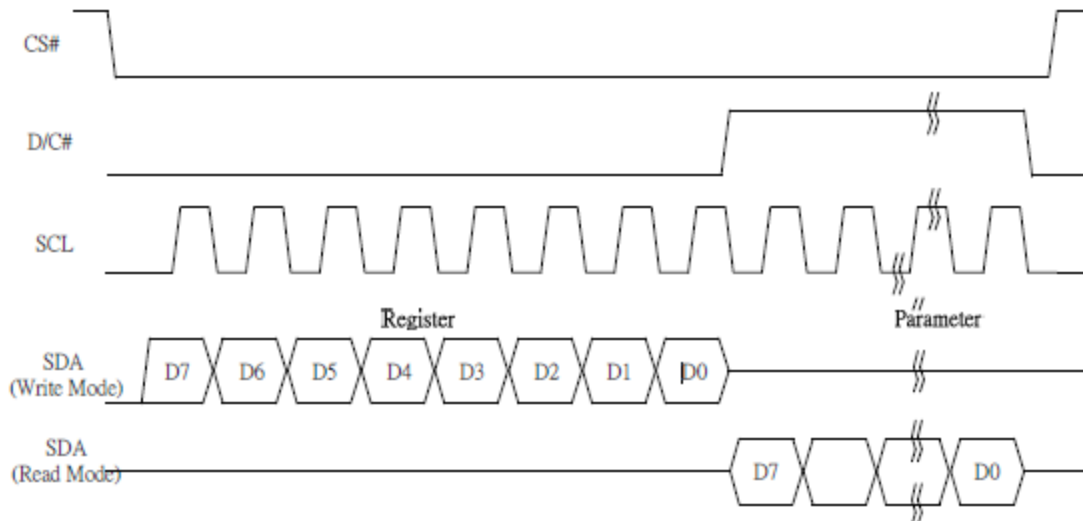


Figure 7-2 Read procedure in 4-wire SPI mode

7.3MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data SDA and CS#. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 6-3. In the write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1, the following byte is data. Table 6-3 shows the write procedure in 3-wire SPI

Table 7-3 : Control pins status of 3-wire SPI

Function	SCL pin	SDI pin	D/C# pin	CS# pin
Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

Note:

- (1) L is connected to V_{SS} and H is connected to V_{DDIO}
- (2) ↑ stands for rising edge of signal

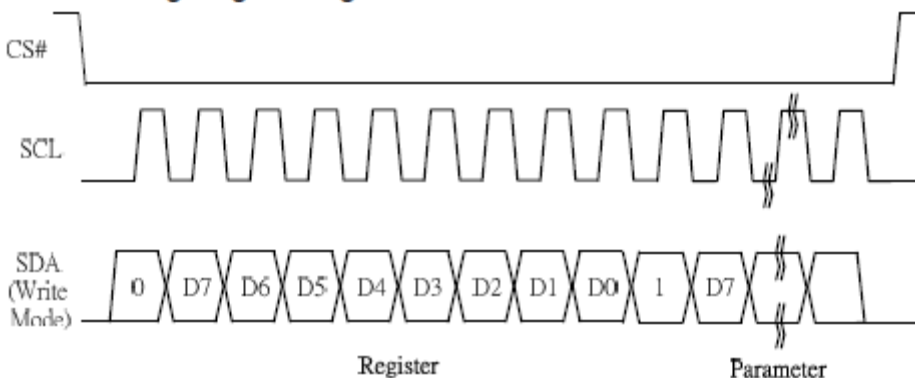


Figure 7-3 Write procedure in 3-wire SPI mode



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In the read operation (command 0x1B, 0x27, 0x2D, 0x2E, 0x2F, 0x35). SDA data are transferred in the unit of 9 bits. After CS# pull low, the first byte is command byte, the D/C# bit is as 0 and following with the register byte. After command byte send, the following byte(s) are data byte(s), with D/C# bit is 1. After D/C# bit sending from MCU, an 8-bit data will be shifted out on every clock falling edge. The serial data SDA bit shifting sequence is D7, D6, to D0 bit. Figure 6-4 shows the read procedure in 3-wire SPI.

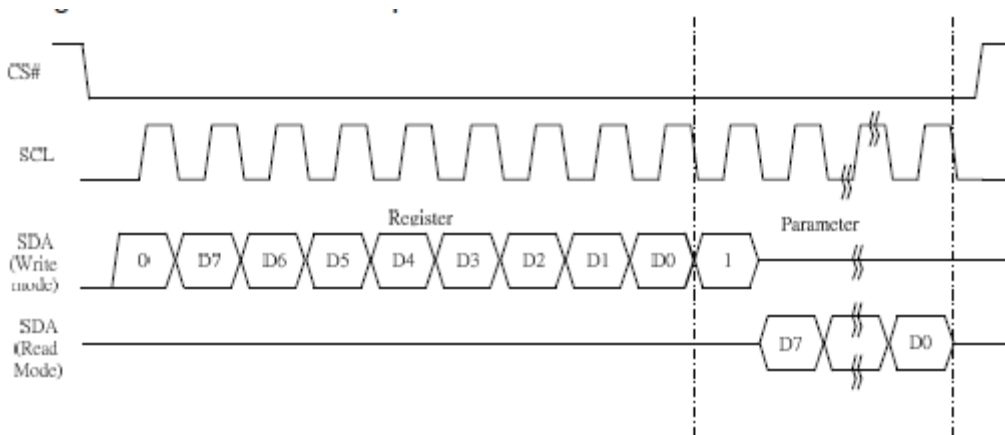


Figure 7-4 Read procedure in 3-wire SPI mode



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8. Temperature sensor operation

Following is the way of how to sense the ambient temperature of the module. First, use an external temperature sensor to get the temperature value and converted it into HEX format with below mapping table, then send command 0x1A with the HEX temperature value to the module thru the SPI interface.

The temperature value to HEX conversion is as follow:

1. If the Temperature value MSByte bit D11 = 0, then

The temperature is positive and value (DegC) = + (Temperature value) / 16

2. If the Temperature value MSByte bit D11 = 1, then

The temperature is negative and value (DegC) = ~ (2's complement of Temperature value) /16

Table 8-1 : Example of 12-bit binary temperature settings for temperature ranges

12-bit binary (2's complement)	Hexadecimal Value	TR Value [DegC]
0111 1111 1111	7FF	128
0111 1111 1111	7FF	127.9
0110 0100 0000	640	100
0101 0000 0000	500	80
0100 1011 0000	4B0	75
0011 0010 0000	320	50
0001 1001 0000	190	25
0000 0000 0100	004	0.25
0000 0000 0000	000	0
1111 1111 1100	FFC	-0.25
1110 0111 0000	E70	-25
1100 1001 0000	C90	-55



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9.COMMAND TABLE

Command Table											Command	Description																																																								
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0																																																										
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting																																																								
0	1		A7	A6	A5	A4	A3	A2	A1	A0		A[8:0]= 127h [POR], 296 MUX																																																								
0	1		0	0	0	0	0	0	0	A8		MUX Gate lines setting as (A[8:0] + 1).																																																								
0	1		0	0	0	0	0	B2	B1	B0		B[2:0] = 000 [POR]. Gate scanning sequence and direction																																																								
												B[2]: GD Selects the 1st output Gate GD=0 [POR], G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, ... GD=1, G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, ...																																																								
												B[1]: SM Change scanning order of gate driver. SM=0 [POR], G0, G1, G2, G3...295 (left and right gate interlaced) SM=1, G0, G2, G4 ...G294, G1, G3, ...G295																																																								
												B[0]: TB TB = 0 [POR], scan from G0 to G295 TB = 1, scan from G295 to G0.																																																								
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage Control	Set Gate driving voltage																																																								
0	1		0	0	0	A4	A3	A2	A1	A0		A[4:0] = 00h [POR] VGH setting from 10V to 20V																																																								
												<table border="1"> <thead> <tr> <th>A[4:0]</th> <th>VGH</th> <th>A[4:0]</th> <th>VGH</th> </tr> </thead> <tbody> <tr><td>00h</td><td>20</td><td>0Dh</td><td>15</td></tr> <tr><td>03h</td><td>10</td><td>0Eh</td><td>15.5</td></tr> <tr><td>04h</td><td>10.5</td><td>0Fh</td><td>16</td></tr> <tr><td>05h</td><td>11</td><td>10h</td><td>16.5</td></tr> <tr><td>06h</td><td>11.5</td><td>11h</td><td>17</td></tr> <tr><td>07h</td><td>12</td><td>12h</td><td>17.5</td></tr> <tr><td>08h</td><td>12.5</td><td>13h</td><td>18</td></tr> <tr><td>07h</td><td>12</td><td>14h</td><td>18.5</td></tr> <tr><td>08h</td><td>12.5</td><td>15h</td><td>19</td></tr> <tr><td>09h</td><td>13</td><td>16h</td><td>19.5</td></tr> <tr><td>0Ah</td><td>13.5</td><td>17h</td><td>20</td></tr> <tr><td>0Bh</td><td>14</td><td>Other</td><td>NA</td></tr> <tr><td>0Ch</td><td>14.5</td><td></td><td></td></tr> </tbody> </table>	A[4:0]	VGH	A[4:0]	VGH	00h	20	0Dh	15	03h	10	0Eh	15.5	04h	10.5	0Fh	16	05h	11	10h	16.5	06h	11.5	11h	17	07h	12	12h	17.5	08h	12.5	13h	18	07h	12	14h	18.5	08h	12.5	15h	19	09h	13	16h	19.5	0Ah	13.5	17h	20	0Bh	14	Other	NA	0Ch	14.5		
A[4:0]	VGH	A[4:0]	VGH																																																																	
00h	20	0Dh	15																																																																	
03h	10	0Eh	15.5																																																																	
04h	10.5	0Fh	16																																																																	
05h	11	10h	16.5																																																																	
06h	11.5	11h	17																																																																	
07h	12	12h	17.5																																																																	
08h	12.5	13h	18																																																																	
07h	12	14h	18.5																																																																	
08h	12.5	15h	19																																																																	
09h	13	16h	19.5																																																																	
0Ah	13.5	17h	20																																																																	
0Bh	14	Other	NA																																																																	
0Ch	14.5																																																																			



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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source driving voltage
0	1		A7	A6	A5	A4	A3	A2	A1	A0		A[7:0] = 41h [POR], VSH1 at 15V
0	1		B7	B6	B5	B4	B3	B2	B1	B0		B[7:0] = A8h [POR], VSH2 at 5V.
0	1		C7	C6	C5	C4	C3	C2	C1	C0		C[7:0] = 32h [POR], VSL at -15V
												Remark: VSH1>=VSH2

A[7]/B[7] = 1,
VSH1/VSH2 voltage setting from 2.4V to 8.8V

A[7]/B[7] = 0,
VSH1/VSH2 voltage setting from 9V to 17V

C[7] = 0,
VSL setting from -5V to -17V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
8Eh	2.4	AFh	5.7
8Fh	2.5	B0h	5.8
90h	2.6	B1h	5.9
91h	2.7	B2h	6
92h	2.8	B3h	6.1
93h	2.9	B4h	6.2
94h	3	B5h	6.3
95h	3.1	B6h	6.4
96h	3.2	B7h	6.5
97h	3.3	B8h	6.6
98h	3.4	B9h	6.7
99h	3.5	BAh	6.8
9Ah	3.6	BBh	6.9
9Bh	3.7	BCh	7
9Ch	3.8	BDh	7.1
9Dh	3.9	BEh	7.2
9Eh	4	BFh	7.3
9Fh	4.1	C0h	7.4
A0h	4.2	C1h	7.5
A1h	4.3	C2h	7.6
A2h	4.4	C3h	7.7
A3h	4.5	C4h	7.8
A4h	4.6	C5h	7.9
A5h	4.7	C6h	8
A6h	4.8	C7h	8.1
A7h	4.9	C8h	8.2
A8h	5	C9h	8.3
A9h	5.1	CAh	8.4
AAh	5.2	CBh	8.5
ABh	5.3	CCh	8.6
ACH	5.4	CDh	8.7
ADh	5.5	CEh	8.8
Aeh	5.6	Other	NA

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
23h	9	3Ch	14
24h	9.2	3Dh	14.2
25h	9.4	3Eh	14.4
26h	9.6	3Fh	14.6
27h	9.8	40h	14.8
28h	10	41h	15
29h	10.2	42h	15.2
2Ah	10.4	43h	15.4
2Bh	10.6	44h	15.6
2Ch	10.8	45h	15.8
2Dh	11	46h	16
2Eh	11.2	47h	16.2
2Fh	11.4	48h	16.4
30h	11.6	49h	16.6
31h	11.8	4Ah	16.8
32h	12	4Bh	17
33h	12.2	Other	NA
34h	12.4		
35h	12.6		
36h	12.8		
37h	13		
38h	13.2		
39h	13.4		
3Ah	13.6		
3Bh	13.8		

C[7:0]	VSL
0Ah	-5
0Ch	-5.5
0Eh	-6
10h	-6.5
12h	-7
14h	-7.5
16h	-8
18h	-8.5
1Ah	-9
1Ch	-9.5
1Eh	-10
20h	-10.5
22h	-11
24h	-11.5
26h	-12
28h	-12.5
2Ah	-13
2Ch	-13.5
2Eh	-14
30h	-14.5
32h	-15
34h	-15.5
36h	-16
38h	-16.5
3Ah	-17
Other	NA

0	0	08	0	0	0	0	0	1	0	0	0	Initial Code Setting OTP Program	Program Initial Code Setting
													The command required ENABLE CLOCK SIGNAL. Refer to Register 0x22 for detail. BUSY pad will output high during operation.

0	0	09	0	0	0	0	0	1	0	0	1	Write Register for Initial Code Setting	Write Register for Initial Code Setting Selection
0	1		A7	A6	A5	A4	A3	A2	A1	A0			A[7:0] ~ D[7:0]: Reserved
0	1		B7	B6	B5	B4	B3	B2	B1	B0			Details refer to Application Notes of Initial Code Setting
0	1		C7	C6	C5	C4	C3	C2	C1	C0			
0	1		D7	D6	D5	D4	D3	D2	D1	D0			

0	0	0A	0	0	0	0	0	1	0	1	0	Read Register for Initial Code Setting	Read Register for Initial Code Setting
---	---	----	---	---	---	---	---	---	---	---	---	--	--



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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																																																									
0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start	Booster Enable with Phase 1, Phase 2 and Phase 3 for soft start current and duration setting. A[7:0] -> Soft start setting for Phase1 = 8Bh [POR] B[7:0] -> Soft start setting for Phase2 = 9Ch [POR] C[7:0] -> Soft start setting for Phase3 = 96h [POR] D[7:0] -> Duration setting = 0Fh [POR] Bit Description of each byte: A[6:0] / B[6:0] / C[6:0]: <table border="1" data-bbox="1075 748 1533 1088"> <thead> <tr> <th>Bit[6:4]</th> <th>Driving Strength Selection</th> </tr> </thead> <tbody> <tr><td>000</td><td>1(Weakest)</td></tr> <tr><td>001</td><td>2</td></tr> <tr><td>010</td><td>3</td></tr> <tr><td>011</td><td>4</td></tr> <tr><td>100</td><td>5</td></tr> <tr><td>101</td><td>6</td></tr> <tr><td>110</td><td>7</td></tr> <tr><td>111</td><td>8(Strongest)</td></tr> </tbody> </table> <table border="1" data-bbox="1075 1115 1533 1664"> <thead> <tr> <th>Bit[3:0]</th> <th>Min Off Time Setting of GDR [Time unit]</th> </tr> </thead> <tbody> <tr><td>0000</td><td rowspan="2">NA</td></tr> <tr><td>0011</td></tr> <tr><td>0100</td><td>2.6</td></tr> <tr><td>0101</td><td>3.2</td></tr> <tr><td>0110</td><td>3.9</td></tr> <tr><td>0111</td><td>4.6</td></tr> <tr><td>1000</td><td>5.4</td></tr> <tr><td>1001</td><td>6.3</td></tr> <tr><td>1010</td><td>7.3</td></tr> <tr><td>1011</td><td>8.4</td></tr> <tr><td>1100</td><td>9.8</td></tr> <tr><td>1101</td><td>11.5</td></tr> <tr><td>1110</td><td>13.8</td></tr> <tr><td>1111</td><td>16.5</td></tr> </tbody> </table> D[5:0]: duration setting of phase D[5:4]: duration setting of phase 3 D[3:2]: duration setting of phase 2 D[1:0]: duration setting of phase 1 <table border="1" data-bbox="1075 1787 1533 1982"> <thead> <tr> <th>Bit[1:0]</th> <th>Duration of Phase [Approximation]</th> </tr> </thead> <tbody> <tr><td>00</td><td>10ms</td></tr> <tr><td>01</td><td>20ms</td></tr> <tr><td>10</td><td>30ms</td></tr> <tr><td>11</td><td>40ms</td></tr> </tbody> </table>	Bit[6:4]	Driving Strength Selection	000	1(Weakest)	001	2	010	3	011	4	100	5	101	6	110	7	111	8(Strongest)	Bit[3:0]	Min Off Time Setting of GDR [Time unit]	0000	NA	0011	0100	2.6	0101	3.2	0110	3.9	0111	4.6	1000	5.4	1001	6.3	1010	7.3	1011	8.4	1100	9.8	1101	11.5	1110	13.8	1111	16.5	Bit[1:0]	Duration of Phase [Approximation]	00	10ms	01	20ms	10	30ms	11	40ms
Bit[6:4]	Driving Strength Selection																																																																				
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10	30ms																																																																				
11	40ms																																																																				
0	1		1	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	Control																																																										
0	1		1	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀																																																											
0	1		1	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀																																																											
0	1		0	0	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀																																																											



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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description								
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control: <table border="1"> <tr> <th>A[1:0] :</th> <th>Description</th> </tr> <tr> <td>00</td> <td>Normal Mode [POR]</td> </tr> <tr> <td>01</td> <td>Enter Deep Sleep Mode 1</td> </tr> <tr> <td>11</td> <td>Enter Deep Sleep Mode 2</td> </tr> </table> After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high. Remark: To Exit Deep Sleep mode, User required to send HWRESET to the driver	A[1:0] :	Description	00	Normal Mode [POR]	01	Enter Deep Sleep Mode 1	11	Enter Deep Sleep Mode 2
A[1:0] :	Description																			
00	Normal Mode [POR]																			
01	Enter Deep Sleep Mode 1																			
11	Enter Deep Sleep Mode 2																			
0	1		0	0	0	0	0	0	A ₁	A ₀										
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A[2:0] = 011 [POR] A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 - Y decrement, X decrement, 01 - Y decrement, X increment, 10 - Y increment, X decrement, 11 - Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.								
0	1		0	0	0	0	0	A ₂	A ₁	A ₀										
0	0	12	0	0	0	1	0	0	1	0	SW RESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode During operation, BUSY pad will output high. Note: RAM are unaffected by this command.								



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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description														
0	0	14	0	0	0	1	0	1	0	0	HV Ready Detection	HV ready detection A[7:0] = 00h [POR] The command required CLKEN=1 and ANALOGEN=1. Refer to Register 0x22 for detail. After this command initiated, HV Ready detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).														
0	1		0	A ₆	A ₅	A ₄	0	A ₂	A ₁	A ₀			A[6:4]=n for cool down duration: 10ms x (n+1) A[2:0]=m for number of Cool Down Loop to detect. The max HV ready duration is 10ms x (n+1) x (m) HV ready detection will be trigger after each cool down time. The detection will be completed when HV is ready. For 1 shot HV ready detection, A[7:0] can be set as 00h.													
0	0	15	0	0	0	1	0	1	0	1	VCI Detection	VCI Detection A[2:0] = 100 [POR] , Detect level at 2.3V A[2:0] : VCI level Detect <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>A[2:0]</th> <th>VCI level</th> </tr> </thead> <tbody> <tr> <td>011</td> <td>2.2V</td> </tr> <tr> <td>100</td> <td>2.3V</td> </tr> <tr> <td>101</td> <td>2.4V</td> </tr> <tr> <td>110</td> <td>2.5V</td> </tr> <tr> <td>111</td> <td>2.6V</td> </tr> <tr> <td>Other</td> <td>NA</td> </tr> </tbody> </table>	A[2:0]	VCI level	011	2.2V	100	2.3V	101	2.4V	110	2.5V	111	2.6V	Other	NA
A[2:0]	VCI level																									
011	2.2V																									
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Other	NA																									
0	1		0	0	0	0	0	A ₂	A ₁	A ₀	The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. After this command initiated, VCI detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).															
0	0	18	0	0	0	1	1	0	0	0	Temperature Sensor Control	Temperature Sensor Selection A[7:0] = 0x48[POR], external temperature sensor A[7:0] = 0x 80 Internal temperature sensor														
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[7:0] = 0x 7F [POR]														
0	1		A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄																
0	1		A ₃	A ₂	A ₁	A ₀	0	0	0	0																



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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																
0	0	1B	0	0	0	1	1	0	1	1	Temperature Sensor Control (Read from temperature register)	Read from temperature register.																
1	1		A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄																		
1	1		A ₃	A ₂	A ₁	A ₀	0	0	0	0																		
0	0	1C	0	0	0	1	1	1	0	0	Temperature Sensor Control (Write Command to External temperature sensor)	Write Command to External temperature sensor. A[7:0] = 00h [POR], B[7:0] = 00h [POR], C[7:0] = 00h [POR], A[7:6] <table border="1"> <tr> <td>A[7:6]</td> <td>Select no of byte to be sent</td> </tr> <tr> <td>00</td> <td>Address + pointer</td> </tr> <tr> <td>.</td> <td>Address + pointer + 1st parameter</td> </tr> <tr> <td>10</td> <td>Address + pointer + 1st parameter + 2nd pointer</td> </tr> <tr> <td>11</td> <td>Address</td> </tr> </table> A[5:0] - Pointer Setting B[7:0] - 1 st parameter C[7:0] - 2 nd parameter The command required ENABLE CLOCK SIGNAL.. Refer to Register 0x22 for detail. After this command initiated, Write Command to external temperature sensor starts. BUSY pad will output high during operation.	A[7:6]	Select no of byte to be sent	00	Address + pointer	.	Address + pointer + 1st parameter	10	Address + pointer + 1st parameter + 2nd pointer	11	Address						
A[7:6]	Select no of byte to be sent																											
00	Address + pointer																											
.	Address + pointer + 1st parameter																											
10	Address + pointer + 1st parameter + 2nd pointer																											
11	Address																											
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																		
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀																		
0	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀																		
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h. BUSY pad will output high during operation. User should not interrupt this operation to avoid corruption of panel images.																
0	0	21	0	0	1	0	0	0	0	1	Display Update Control	RAM content option for Display Update A[7:0] = 00h [POR] B[7:0] = 00h [POR] A[7:4] Red RAM option <table border="1"> <tr> <td>0000</td> <td>Normal</td> </tr> <tr> <td>0100</td> <td>Bypass RAM content as 0</td> </tr> <tr> <td>1000</td> <td>Inverse RAM content</td> </tr> </table> A[3:0] BW RAM option <table border="1"> <tr> <td>0000</td> <td>Normal</td> </tr> <tr> <td>0100</td> <td>Bypass RAM content as 0</td> </tr> <tr> <td>1000</td> <td>Inverse RAM content</td> </tr> </table> B[7] Source Output Mode <table border="1"> <tr> <td>0</td> <td>Available Source from S0 to S175</td> </tr> <tr> <td>1</td> <td>Available Source from S8 to S167</td> </tr> </table>	0000	Normal	0100	Bypass RAM content as 0	1000	Inverse RAM content	0000	Normal	0100	Bypass RAM content as 0	1000	Inverse RAM content	0	Available Source from S0 to S175	1	Available Source from S8 to S167
0000	Normal																											
0100	Bypass RAM content as 0																											
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1	Available Source from S8 to S167																											
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																		
0	1		B ₇	0	0	0	0	0	0	0																		



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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																																																																																						
0	0	22	0	0	1	0	0	0	1	0	Display Update	Display Update Sequence Option:																																																																																						
0	1		A7	A6	A5	A4	A3	A2	A1	A0	Control 2	Enable the stage for Master Activation A[7:0]= FFh (POR)																																																																																						
												<table border="1"> <thead> <tr> <th>Operating sequence</th> <th>Parameter (in Hex)</th> </tr> </thead> <tbody> <tr> <td>Enable clock signal</td> <td>80</td> </tr> <tr> <td>Disable clock signal</td> <td>01</td> </tr> <tr> <td>Enable clock signal</td> <td>C0</td> </tr> <tr> <td>Enable Analog</td> <td></td> </tr> <tr> <td>Disable Analog</td> <td>03</td> </tr> <tr> <td>Disable clock signal</td> <td></td> </tr> <tr> <td>Enable clock signal</td> <td></td> </tr> <tr> <td>Load LUT with DISPLAY Mode 1</td> <td>91</td> </tr> <tr> <td>Disable clock signal</td> <td></td> </tr> <tr> <td>Enable clock signal</td> <td></td> </tr> <tr> <td>Load LUT with DISPLAY Mode 2</td> <td>99</td> </tr> <tr> <td>Disable clock signal</td> <td></td> </tr> <tr> <td>Enable clock signal</td> <td></td> </tr> <tr> <td>Load temperature value</td> <td></td> </tr> <tr> <td>Load LUT with DISPLAY Mode 1</td> <td>B1</td> </tr> <tr> <td>Disable clock signal</td> <td></td> </tr> <tr> <td>Enable clock signal</td> <td></td> </tr> <tr> <td>Load temperature value</td> <td></td> </tr> <tr> <td>Load LUT with DISPLAY Mode 2</td> <td>B9</td> </tr> <tr> <td>Disable clock signal</td> <td></td> </tr> <tr> <td>Enable clock signal</td> <td></td> </tr> <tr> <td>Enable Analog</td> <td></td> </tr> <tr> <td>Display with DISPLAY Mode 1</td> <td>C7</td> </tr> <tr> <td>Disable Analog</td> <td></td> </tr> <tr> <td>Disable OSC</td> <td></td> </tr> <tr> <td>Enable clock signal</td> <td></td> </tr> <tr> <td>Enable Analog</td> <td></td> </tr> <tr> <td>Display with DISPLAY Mode 2</td> <td>CF</td> </tr> <tr> <td>Disable Analog</td> <td></td> </tr> <tr> <td>Disable OSC</td> <td></td> </tr> <tr> <td>Enable clock signal</td> <td></td> </tr> <tr> <td>Enable Analog</td> <td></td> </tr> <tr> <td>Load temperature value</td> <td></td> </tr> <tr> <td>DISPLAY with DISPLAY Mode 1</td> <td>F7</td> </tr> <tr> <td>Disable Analog</td> <td></td> </tr> <tr> <td>Disable OSC</td> <td></td> </tr> <tr> <td>Enable clock signal</td> <td></td> </tr> <tr> <td>Enable Analog</td> <td></td> </tr> <tr> <td>Load temperature value</td> <td></td> </tr> <tr> <td>DISPLAY with DISPLAY Mode 2</td> <td>FF</td> </tr> <tr> <td>Disable Analog</td> <td></td> </tr> <tr> <td>Disable OSC</td> <td></td> </tr> </tbody> </table>	Operating sequence	Parameter (in Hex)	Enable clock signal	80	Disable clock signal	01	Enable clock signal	C0	Enable Analog		Disable Analog	03	Disable clock signal		Enable clock signal		Load LUT with DISPLAY Mode 1	91	Disable clock signal		Enable clock signal		Load LUT with DISPLAY Mode 2	99	Disable clock signal		Enable clock signal		Load temperature value		Load LUT with DISPLAY Mode 1	B1	Disable clock signal		Enable clock signal		Load temperature value		Load LUT with DISPLAY Mode 2	B9	Disable clock signal		Enable clock signal		Enable Analog		Display with DISPLAY Mode 1	C7	Disable Analog		Disable OSC		Enable clock signal		Enable Analog		Display with DISPLAY Mode 2	CF	Disable Analog		Disable OSC		Enable clock signal		Enable Analog		Load temperature value		DISPLAY with DISPLAY Mode 1	F7	Disable Analog		Disable OSC		Enable clock signal		Enable Analog		Load temperature value		DISPLAY with DISPLAY Mode 2	FF	Disable Analog		Disable OSC	
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0	0	24	0	0	1	0	0	1	0	0	Write RAM (Black White) / RAM 0x24	<p>After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly</p> <p>For Write pixel: Content of Write RAM(BW) = 1</p> <p>For Black pixel: Content of Write RAM(BW) = 0</p>																																																																																						



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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED) / RAM 0x26	<p>After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly.</p> <p>For Red pixel: Content of Write RAM0x26 = 1 For non-Red pixel [Black or White]: Content of Write RAM0x26 = 0</p>
0	0	27	0	0	1	0	0	1	1	1	Read RAM	<p>After this command, data read on the MCU bus will fetch data from RAM. According to parameter of Register 41h to select reading RAM0x24/ RAM0x26, until another command is written. Address pointers will advance accordingly.</p> <p>The 1st byte of data read is dummy data.</p>
0	0	28	0	0	1	0	1	0	0	0	VCOM Sense	<p>Enter VCOM sensing conditions and hold for duration defined in command 0x29 before reading VCOM value. The sensed VCOM voltage is stored in register</p> <p>The command required ENABLE CLOCK SIGNAL and ENABLE ANALOG. Refer to Register 0x22 for detail.</p> <p>BUSY pad will output high during operation.</p>
0	0	29	0	0	1	0	1	0	0	1	VCOM Sense Duration	<p>Stabling time between entering VCOM sensing mode and reading acquired.</p> <p>A[3:0] = 0x 9, duration = 10s. VCOM sense duration = (A[3:0]+1) sec</p>
0	1		0	1	0	0	A ₃	A ₂	A ₁	A ₀		
0	0	2A	0	0	1	0	1	0	1	0	Program VCOM OTP	<p>Program VCOM register into OTP</p> <p>The command required ENABLE CLOCK SIGNAL. Refer to Register 0x22 for detail.</p> <p>BUSY pad will output high during operation.</p>



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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description				
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Write VCOM register from MCU interface A[7:0] = 00h [POR]				
0	1		A7	A6	A5	A4	A3	A2	A1	A0						
													A[7:0]	VCOM	A[7:0]	VCOM
													08h	-0.2	44h	-1.7
													0Ch	-0.3	48h	-1.8
													10h	-0.4	4Ch	-1.9
													14h	-0.5	50h	-2
													18h	-0.6	54h	-2.1
													1Ch	-0.7	58h	-2.2
													20h	-0.8	5Ch	-2.3
													24h	-0.9	60h	-2.4
													28h	-1	64h	-2.5
													2Ch	-1.1	68h	-2.6
													30h	-1.2	6Ch	-2.7
													34h	-1.3	70h	-2.8
											38h	-1.4	74h	-2.9		
											3Ch	-1.5	78h	-3		
											40h	-1.6	Other	NA		

0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read for Display Option	Read Register for Display Option: A[7:0]: VCOM OTP Selection (Command 0x37, Byte A) B[7:0]: VCOM Register (Command 0x2C) C[7:0]~G[7:0]: Display Mode (Command 0x37, Byte B to Byte F) [5 bytes] H[7:0]~K[7:0]: Waveform Version (Command 0x37, Byte G to Byte J) [4 bytes]	
1	1		A7	A6	A5	A4	A3	A2	A1	A0			
1	1		B7	B6	B5	B4	B3	B2	B1	B0			
1	1		C7	C6	C5	C4	C3	C2	C1	C0			
1	1		D7	D6	D5	D4	D3	D2	D1	D0			
1	1		E7	E6	E5	E4	E3	E2	E1	E0			
1	1		F7	F6	F5	F4	F3	F2	F1	F0			
1	1		G7	G6	G5	G4	G3	G2	G1	G0			
1	1		H7	H6	H5	H4	H3	H2	H1	H0			
1	1		I7	I6	I5	I4	I3	I2	I1	I0			
1	1		J7	J6	J5	J4	J3	J2	J1	J0			
1	1		K7	K6	K5	K4	K3	K2	K1	K0			

0	0	2E	0	0	1	0	1	1	1	0	User ID Read	Read 10 Byte User ID stored in OTP: A[7:0]~J[7:0]: UserID (R38, Byte A and Byte J) [10 bytes]	
1	1		A7	A6	A5	A4	A3	A2	A1	A0			
1	1		B7	B6	B5	B4	B3	B2	B1	B0			
1	1		C7	C6	C5	C4	C3	C2	C1	C0			
1	1		D7	D6	D5	D4	D3	D2	D1	D0			
1	1		E7	E6	E5	E4	E3	E2	E1	E0			
1	1		F7	F6	F5	F4	F3	F2	F1	F0			
1	1		G7	G6	G5	G4	G3	G2	G1	G0			
1	1		H7	H6	H5	H4	H3	H2	H1	H0			
1	1		I7	I6	I5	I4	I3	I2	I1	I0			
1	1		J7	J6	J5	J4	J3	J2	J1	J0			



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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	2F	0	0	1	0	1	1	1	1	Status Bit Read	Read IC status Bit [POR 0x01]
1	1		0	0	A5	A4	0	0	A1	A0		A[5]: HV Ready Detection flag [POR=0] 0: Ready 1: Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1: VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01] Remark: A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively.

0	0	37	0	0	1	1	0	1	1	1	Write Register for Display Option	Write Register for Display Option	
0	1		A7	0	0	0	0	0	0	0			A[7] Spare VCOM OTP selection 0: Default [POR] 1: Spare
0	1		B7	B6	B5	B4	B3	B2	B1	B0			B[7:0] Display Mode for WS[7:0]
0	1		C7	C6	C5	C4	C3	C2	C1	C0			C[7:0] Display Mode for WS[15:8]
0	1		D7	D6	D5	D4	D3	D2	D1	D0			D[7:0] Display Mode for WS[23:16]
0	1		E7	E6	E5	E4	E3	E2	E1	E0			E[7:0] Display Mode for WS[31:24]
0	1		0	F6	0	0	F3	F2	F1	F0			F[3:0] Display Mode for WS[35:32]
0	1		G7	G6	G5	G4	G3	G2	G1	G0			0: Display Mode 1 1: Display Mode 2
0	1		H7	H6	H5	H4	H3	H2	H1	H0			
0	1		I7	I6	I5	I4	I3	I2	I1	I0			
0	1		J7	J6	J5	J4	J3	J2	J1	J0			F[6]: PingPong for Display Mode 2 0: RAM Ping-Pong disable [POR] 1: RAM Ping-Pong enable G[7:0]~J[7:0] module ID /waveform version. Remarks: 1) A[7:0]~J[7:0] can be stored in OTP 2) RAM Ping-Pong function is not support for Display Mode 1

0	0	38	0	0	1	1	1	0	0	0	Write Register for User ID	Write Register for User ID	
0	1		A7	A6	A5	A4	A3	A2	A1	A0			A[7:0]~J[7:0]: UserID [10 bytes]
0	1		B7	B6	B5	B4	B3	B2	B1	B0			
0	1		C7	C6	C5	C4	C3	C2	C1	C0			
0	1		D7	D6	D5	D4	D3	D2	D1	D0			
0	1		E7	E6	E5	E4	E3	E2	E1	E0			
0	1		F7	F6	F5	F4	F3	F2	F1	F0			
0	1		G7	G6	G5	G4	G3	G2	G1	G0			Remarks: A[7:0]~J[7:0] can be stored in OTP by command 0x36



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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																																										
0	1		H7	H6	H5	H4	H3	H2	H1	H0																																												
0	1		I7	I6	I5	I4	I3	I2	I1	I0																																												
0	1		J7	J6	J5	J4	J3	J2	J1	J0																																												
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A[7:0] = C0h [POR], set VBD as HiZ. A [7:6] :Select VBD option																																										
0	1		A7	A6	A5	A4	0	A2	A1	A0		<table border="1"> <tr> <td>A[7:6]</td> <td>Select VBD as</td> </tr> <tr> <td>00</td> <td>GS Transition, Defined in A[2] and A[1:0]</td> </tr> <tr> <td>01</td> <td>Fix Level, Defined in A[5:4]</td> </tr> <tr> <td>10</td> <td>VCOM</td> </tr> <tr> <td>11[POR]</td> <td>HiZ</td> </tr> </table> <table border="1"> <tr> <td>A [5:4] Fix Level Setting for VBD</td> <td></td> </tr> <tr> <td>A[5:4]</td> <td>VBD level</td> </tr> <tr> <td>00</td> <td>VSS</td> </tr> <tr> <td>01</td> <td>VSH1</td> </tr> <tr> <td>10</td> <td>VSL</td> </tr> <tr> <td>11</td> <td>VSH2</td> </tr> </table> <table border="1"> <tr> <td>A[2] GS Transition control</td> <td></td> </tr> <tr> <td>A[2]</td> <td>GS Transition control</td> </tr> <tr> <td>0</td> <td>Follow LUT (Output VCOM @ RED)</td> </tr> <tr> <td>1</td> <td>Follow LUT</td> </tr> </table> <table border="1"> <tr> <td>A [1:0] GS Transition setting for VBD</td> <td></td> </tr> <tr> <td>A[1:0]</td> <td>VBD Transition</td> </tr> <tr> <td>00</td> <td>LUT0</td> </tr> <tr> <td>01</td> <td>LUT1</td> </tr> <tr> <td>10</td> <td>LUT2</td> </tr> <tr> <td>11</td> <td>LUT3</td> </tr> </table>	A[7:6]	Select VBD as	00	GS Transition, Defined in A[2] and A[1:0]	01	Fix Level, Defined in A[5:4]	10	VCOM	11[POR]	HiZ	A [5:4] Fix Level Setting for VBD		A[5:4]	VBD level	00	VSS	01	VSH1	10	VSL	11	VSH2	A[2] GS Transition control		A[2]	GS Transition control	0	Follow LUT (Output VCOM @ RED)	1	Follow LUT	A [1:0] GS Transition setting for VBD		A[1:0]	VBD Transition	00	LUT0	01	LUT1	10	LUT2	11	LUT3
A[7:6]	Select VBD as																																																					
00	GS Transition, Defined in A[2] and A[1:0]																																																					
01	Fix Level, Defined in A[5:4]																																																					
10	VCOM																																																					
11[POR]	HiZ																																																					
A [5:4] Fix Level Setting for VBD																																																						
A[5:4]	VBD level																																																					
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01	VSH1																																																					
10	VSL																																																					
11	VSH2																																																					
A[2] GS Transition control																																																						
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0	Follow LUT (Output VCOM @ RED)																																																					
1	Follow LUT																																																					
A [1:0] GS Transition setting for VBD																																																						
A[1:0]	VBD Transition																																																					
00	LUT0																																																					
01	LUT1																																																					
10	LUT2																																																					
11	LUT3																																																					
0	0	41	0	1	0	0	0	0	0	1	Read RAM Option	Read RAM Option A[0]= 0 [POR]																																										
0	1		0	0	0	0	0	0	0	A0		0 : Read RAM corresponding to RAM0x24 1 : Read RAM corresponding to RAM0x26																																										
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address	Specify the start/end positions of the window address in the X direction by an address unit for RAM																																										
0	1		0	0	A5	A4	A3	A2	A1	A0	Start / End position																																											
0	1		0	0	B5	B4	B3	B2	B1	B0		A[5:0]: XSA[5:0], XStart, POR = 00h B[5:0]: XEA[5:0], XEnd, POR = 15h																																										
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address	Specify the start/end positions of the window address in the Y direction by an address unit for RAM																																										
0	1		A7	A6	A5	A4	A3	A2	A1	A0	Start / End position																																											
0	1		0	0	0	0	0	0	0	A8																																												
0	1		B7	B6	B5	B4	B3	B2	B1	B0		A[8:0]: YSA[8:0], YStart, POR = 000h B[8:0]: YEA[8:0], YEnd, POR = 127h																																										
0	1		0	0	0	0	0	0	0	B8																																												



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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																																								
0	0	46	0	1	0	0	0	1	1	0	Auto Write RAM0x26 for Regular Pattern	Auto Write RAM0x26 for Regular Pattern A[7:0] = 00h [POR]																																								
0	1		A ₇	A ₆	A ₅	A ₄	0	A ₂	A ₁	A ₀		<p>A[7]: The 1st step value, POR = 0 A[6:4]: Step Height, POR= 000 Step of alter RAM in Y-direction according to Gate</p> <table border="1"> <thead> <tr> <th>A[6:4]</th> <th>Height</th> <th>A[6:4]</th> <th>Height</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>8</td> <td>100</td> <td>128</td> </tr> <tr> <td>001</td> <td>16</td> <td>101</td> <td>256</td> </tr> <tr> <td>010</td> <td>32</td> <td>110</td> <td>296</td> </tr> <tr> <td>011</td> <td>64</td> <td>111</td> <td>NA</td> </tr> </tbody> </table> <p>A[2:0]: Step Width, POR= 000 Step of alter RAM in X-direction according to Source</p> <table border="1"> <thead> <tr> <th>A[2:0]</th> <th>Width</th> <th>A[2:0]</th> <th>Width</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>8</td> <td>100</td> <td>128</td> </tr> <tr> <td>001</td> <td>16</td> <td>101</td> <td>176</td> </tr> <tr> <td>010</td> <td>32</td> <td>110</td> <td>NA</td> </tr> <tr> <td>011</td> <td>64</td> <td>111</td> <td>NA</td> </tr> </tbody> </table> <p>BUSY pad will output high during operation.</p>	A[6:4]	Height	A[6:4]	Height	000	8	100	128	001	16	101	256	010	32	110	296	011	64	111	NA	A[2:0]	Width	A[2:0]	Width	000	8	100	128	001	16	101	176	010	32	110	NA	011	64	111	NA
A[6:4]	Height	A[6:4]	Height																																																	
000	8	100	128																																																	
001	16	101	256																																																	
010	32	110	296																																																	
011	64	111	NA																																																	
A[2:0]	Width	A[2:0]	Width																																																	
000	8	100	128																																																	
001	16	101	176																																																	
010	32	110	NA																																																	
011	64	111	NA																																																	

0	0	47	0	1	0	0	0	1	1	1	Auto Write RAM0x24 for Regular Pattern	Auto Write RAM0x24 for Regular Pattern A[7:0] = 00h [POR]																																								
0	1		A ₇	A ₆	A ₅	A ₄	0	A ₂	A ₁	A ₀		<p>A[7]: The 1st step value, POR = 0 A[6:4]: Step Height, POR= 000 Step of alter RAM in Y-direction according to Gate</p> <table border="1"> <thead> <tr> <th>A[6:4]</th> <th>Height</th> <th>A[6:4]</th> <th>Height</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>8</td> <td>100</td> <td>128</td> </tr> <tr> <td>001</td> <td>16</td> <td>101</td> <td>256</td> </tr> <tr> <td>010</td> <td>32</td> <td>110</td> <td>296</td> </tr> <tr> <td>011</td> <td>64</td> <td>111</td> <td>NA</td> </tr> </tbody> </table> <p>A[2:0]: Step Width, POR= 000 Step of alter RAM in X-direction according to Source</p> <table border="1"> <thead> <tr> <th>A[2:0]</th> <th>Width</th> <th>A[2:0]</th> <th>Width</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>8</td> <td>100</td> <td>128</td> </tr> <tr> <td>001</td> <td>16</td> <td>101</td> <td>176</td> </tr> <tr> <td>010</td> <td>32</td> <td>110</td> <td>NA</td> </tr> <tr> <td>011</td> <td>64</td> <td>111</td> <td>NA</td> </tr> </tbody> </table> <p>During operation, BUSY pad will output high.</p>	A[6:4]	Height	A[6:4]	Height	000	8	100	128	001	16	101	256	010	32	110	296	011	64	111	NA	A[2:0]	Width	A[2:0]	Width	000	8	100	128	001	16	101	176	010	32	110	NA	011	64	111	NA
A[6:4]	Height	A[6:4]	Height																																																	
000	8	100	128																																																	
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000	8	100	128																																																	
001	16	101	176																																																	
010	32	110	NA																																																	
011	64	111	NA																																																	



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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[5:0]: 00h [POR].
0	1		0	0	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: 000h [POR].
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	1		0	0	0	0	0	0	0	A ₈		
0	0	7F	0	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read Commands.



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10.Data Entry Mode Setting (11h)

This command has multiple configurations and each bit setting is described as follows:

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1						AM	ID1	IDO
POR		0	0	0	0	0	0	1	1

ID[1:0]: The address counter is automatically incremented by 1, after data is written to the RAM when ID[1:0] = "01". The address counter is automatically decremented by 1, after data is written to the RAM when ID[1:0] = "00". The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. The direction of the address when data is written to the RAM is set by AM bits.

AM: Set the direction in which the address counter is updated automatically after data are written to the RAM. When AM = "0", the address counter is updated in the X direction. When AM = "1", the address counter is updated in the Y direction. When window addresses are selected, data are written to the RAM area specified by the window addresses in the manner specified with ID[1:0] and AM bits.

	ID [1:0]="00" X: decrement Y: decrement	ID [1:0]="01" X: increment Y: decrement	ID [1:0]="10" X: decrement Y: increment	ID [1:0]="11" X: increment Y: increment
AM="0" X-mode				
AM="1" Y-mode				

The pixel sequence is defined by the ID [0],

	ID [1:0]="00" X: decrement Y: decrement	D [1:0]="01" X: increment Y: decrement
AM="0" X-mode		



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11. Reference Circuit

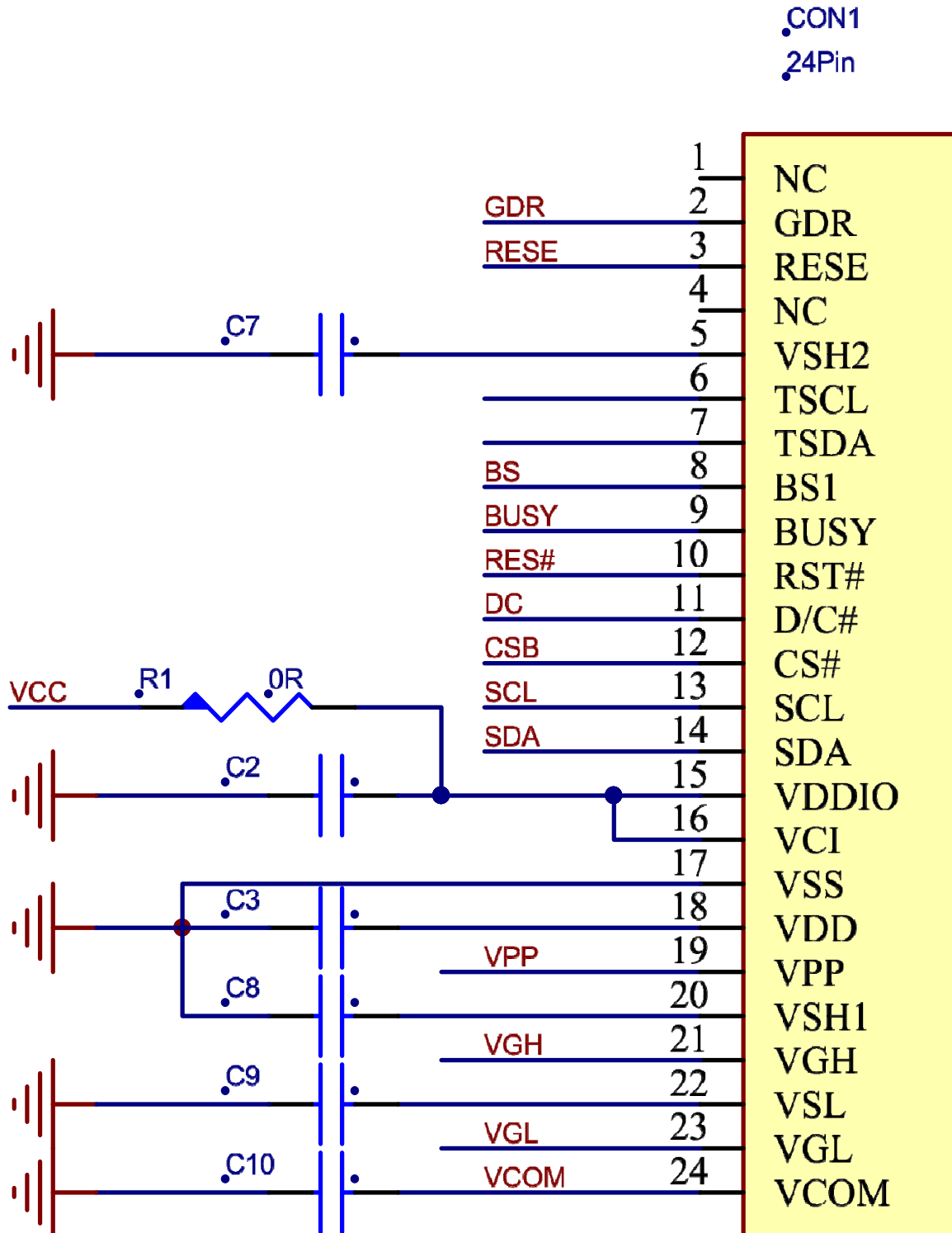


Figure. 11-1



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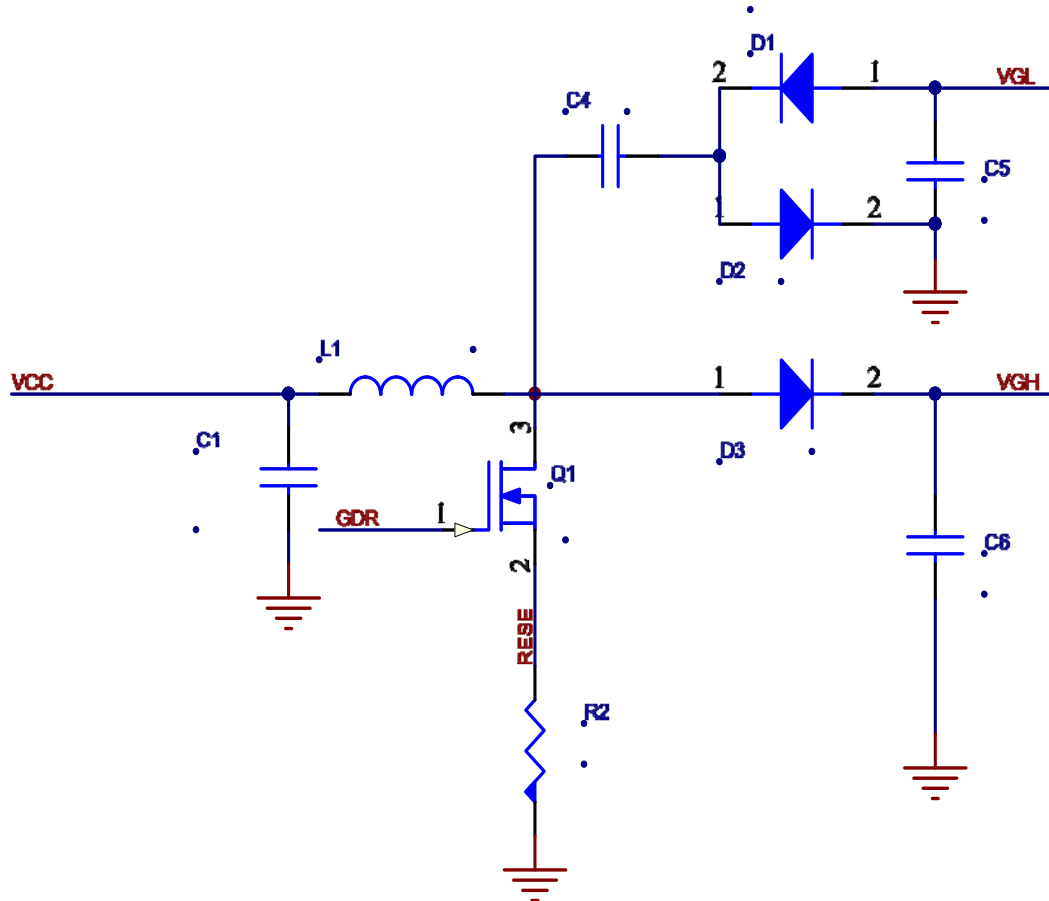


Figure. 11-2

Part Name	Value /requirement/Reference Part
C1—C10	1uF/0603;X5R/X7R;Voltage Rating: 25V
C10	1uF/0603;X7R;Voltage Rating: 25V
D1—D3	MBR0530 1) Reverse DC voltage $\geq 30V$ 2) Forward current $\geq 500mA$ 3) Forward voltage $\leq 430mV$
R2	2.2 Ω /0603: 1% variation
Q1	NMOS:Si1304BDL/NX3008NBK 1) Drain-Source breakdown voltage $\geq 30V$ 2) $V_{gs} (th) = 0.9 (Typ) , 1.3V (Max)$ 3) $R_{ds on} \leq 2.1 \Omega @ V_{gs}=2.5V$
L1	47uH/CDRH2D18、LDNP-470NC Maximum DC current~420mA Maximum DC resistance~650m Ω
CON24Pin	0.5mm ZIF Socket 24Pins,0.5mm pitch



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12. ABSOLUTE MAXIMUM RATING

Table 12-1: Maximum Ratings

Symbol	Parameter	Rating	Unit	Humidity	Unit	Note
V _{CI}	Logic supply voltage	-0.5 to +6.0	V	-	-	
T _{OPR}	Operation temperature range	0 to 50	°C	35 to70	%	
T _{ttg}	Transportation temperature range	-25 to 60	°C	-	-	Note12-2
T _{stg}	Storage condition	0 to 40	°C	35 to70	%	Maximum storage time: 5 years

Note 12-1:Maximum ratings are those values beyond which damages to the device may occur.

Functional operation should be restricted to the limits in the Electrical Characteristics chapter.

Note12-2: T_{ttg} is the transportation condition, the transport time is within 10 days for -25°C~0°C or 50°C~60°C

13.DC CHARACTERISTICS

The following specifications apply for: VSS=0V, VCI=3.3V, T_{OPR}=25°C.

Table 13-1: DC Characteristics

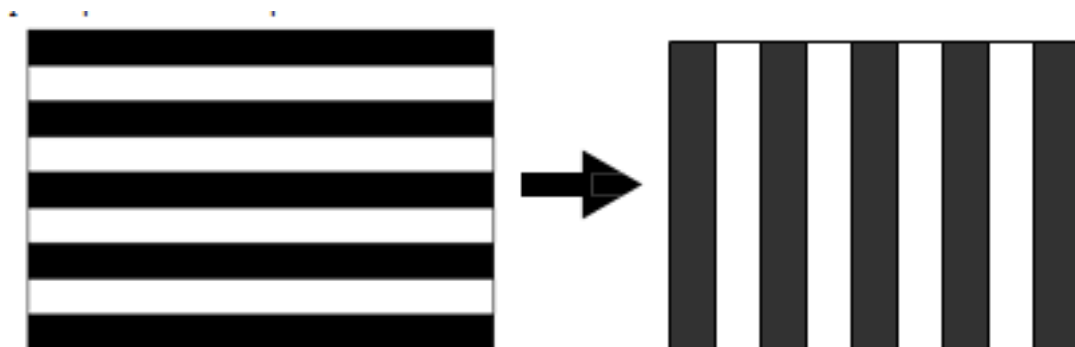
Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
V _{CI}	VCI operation voltage		VCI	2.5	3	3.7	V
V _{IH}	High level input voltage		SDA, SCL, CS#, D/C#, RES#,	0.8VDDIO			V
V _{IL}	Low level input voltage		BS1			0.2VDDIO	V
V _{OH}	High level output voltage	IOH = -100uA	BUSY	0.9VDDIO			V
V _{OL}	Low level output voltage	IOL = 100uA				0.1VDDIO	V
I _{update}	Module operating current			-	3	-	mA
I _{sleep}	Deep sleep mode	VCI=3.3V		-	-	3	uA

The Typical power consumption is measured using associated 25°C waveform with following pattern transition: from horizontal scan pattern to vertical scan pattern. (Note 13-1)

- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by XingTai.
- Vcom value will be OTP before in factory or present on the label sticker.

Note 13-1

The Typical power consumption





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14. Serial Peripheral Interface Timing

The following specifications apply for: VSS=0V, VCI=2.2V to 3.7V, T_{OPR}=25°C, CL=20pF

Write mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Write Mode)			20	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	60			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	65			ns
tCSHIGH	Time CS# has to remain high between two transfers	100			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	25			ns
tSCLLOW	Part of the clock period where SCL has to remain low	25			ns
tSISU	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
tSIHLD	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Read Mode)			2.5	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	100			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	50			ns
tCSHIGH	Time CS# has to remain high between two transfers	250			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	180			ns
tSCLLOW	Part of the clock period where SCL has to remain low	180			ns
tSOSU	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
tSOHLD	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

Note: All timings are based on 20% to 80% of VDDIO-VSS

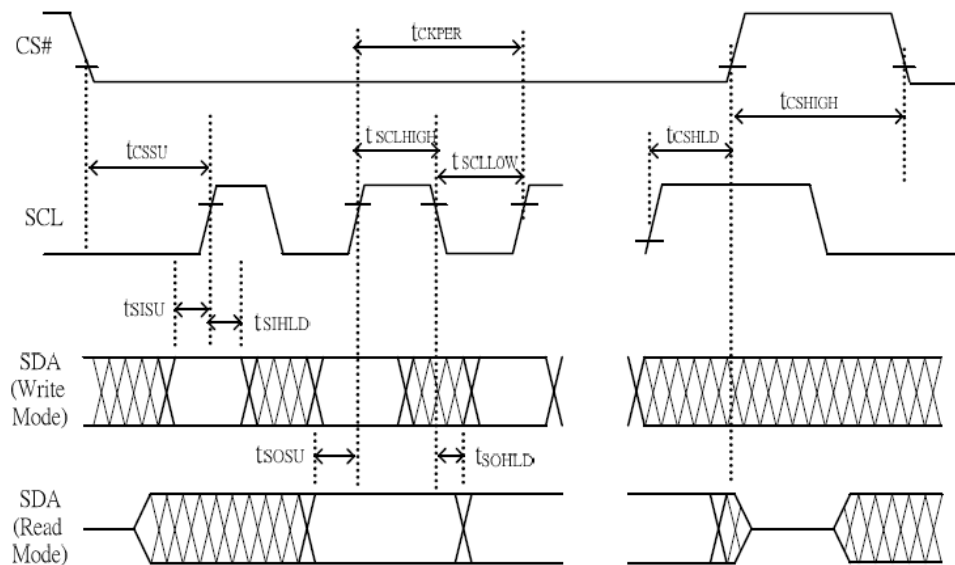


Figure 14-1: SPI timing diagram

15. Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25°C	-	18	mAs	-
Deep sleep mode	-	25°C	-	3	uA	-

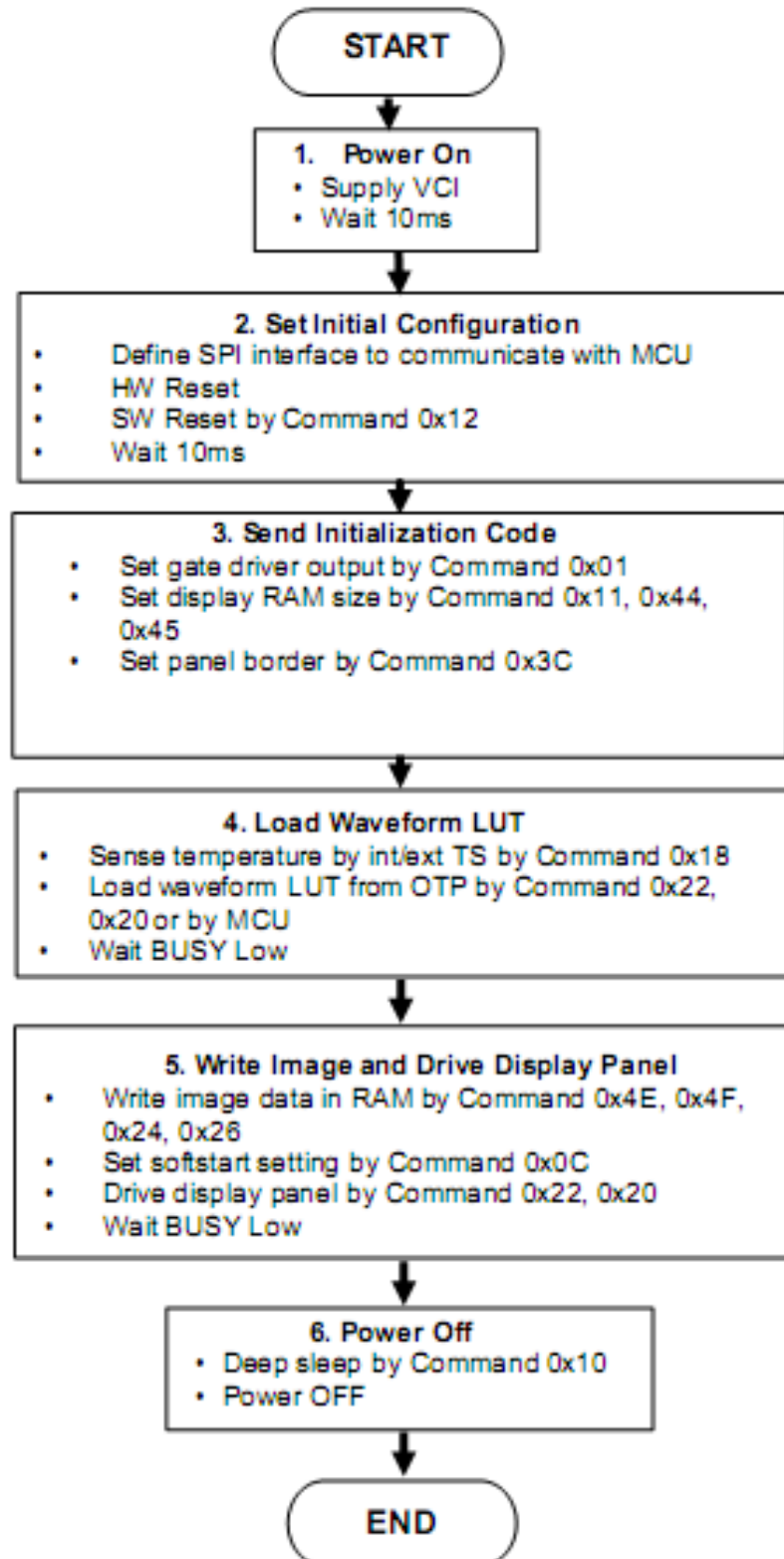
MAS=update average current × update time



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16. Typical Operating Sequence

16.1 Normal Operation Flow





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17. Optical characteristics

17.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 17-1
Gn	2Grey Level	-	-	$KS+(WS-KS) \times n(m-1)$	-	L*	-
CR	Contrast Ratio	-	-	10	-	-	-
KS	Black State L* value	-	-	18	-	-	Note 17-1
	Black State a* value	-	-	0.2	-	-	Note 17-1
WS	White State L* value	-	-	67	-	-	Note 17-1
Panel	Image Update	Storage and transportation	-	Update the white screen	-	-	-
	Update Time	Operation	-	Suggest Updated once a day	-	-	-

WS : White state, KS : Dark state,

Note 17-1 : Luminance meter : Eye - One Pro Spectrophotometer

Note 17-2: We guarantee display quality from 0°C ~ 30°C generally, If operation ambient temperature from 0°C ~ 50°C, will offer special waveform by Xingtai.

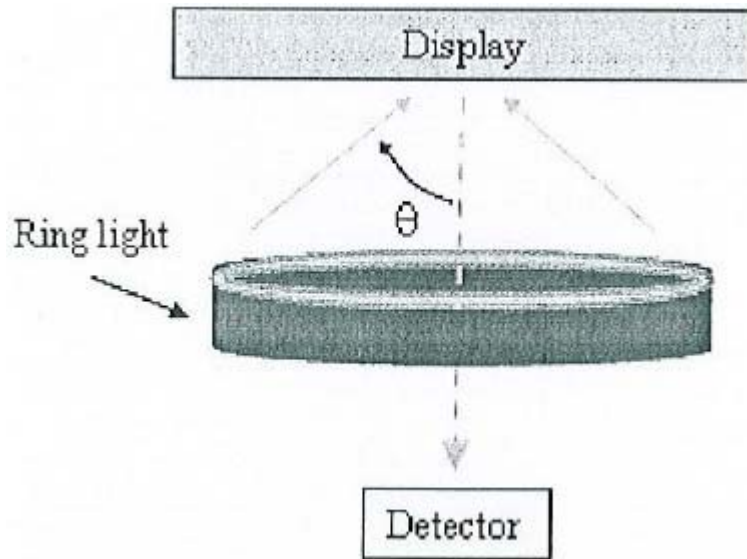


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17.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd):

R1: white reflectance Rd: dark reflectance
CR = R1/Rd

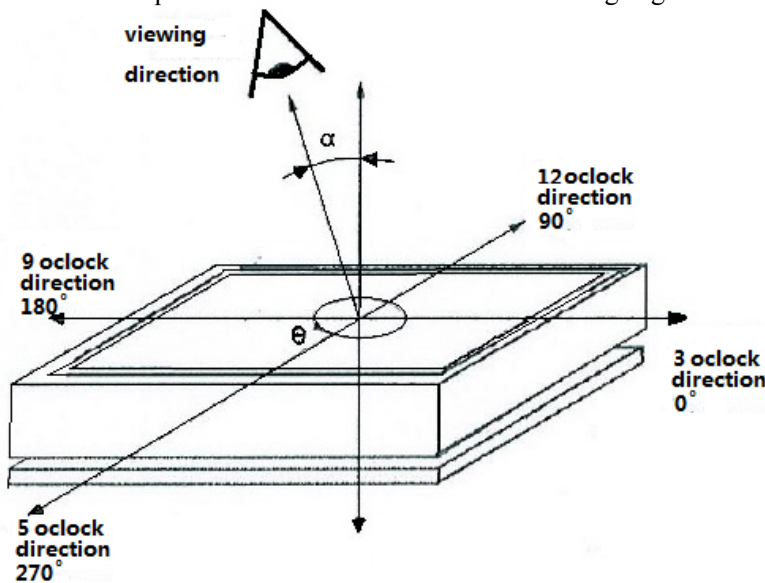


17.3 Reflection Ratio

The reflection ratio is expressed as:

$$R = \text{Reflectance Factor}_{\text{white board}} \times (L_{\text{center}} / L_{\text{white board}})$$

L_{center} is the luminance measured at center in a white area (R=G=B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.





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18. HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING

The display module should be kept flat or fixed to a rigid, curved support with limited bending along the long axis. It should not be used for continual flexing and bending. Handle with care. Should the display break do not touch any material that leaks out. In case of contact with the leaked material then wash with water and soap.

CAUTION

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.

Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions

(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.

(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.

(3) You should adopt radiation structure to satisfy the temperature specification.

(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.

(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)

(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.

(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status

Product specification	The data sheet contains final product specifications.
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Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

Product Environmental certification

ROHS

REMARK

All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.



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19. Reliability test

19.1 Reliability test items

	TEST	CONDITION	REMARK
1	High-Temperature Operation	T=40°C , RH=35%RH, For 240Hr	
2	Low-Temperature Operation	T = 0°C for 240 hrs	
3	High-Temperature Storage	T=60°C RH=35%RH For 240Hr	Test in white pattern
4	Low-Temperature Storage	T = -25°C for 240 hrs	Test in white pattern
5	High Temperature, High-Humidity Operation	T=40°C , RH=90%RH, For 168Hr	
6	High Temperature, High-Humidity Storage	T=60°C , RH=80%RH, For 240Hr	Test in white pattern
7	Temperature Cycle	-25°C(30min)~70°C(30min), 100 Cycle	Test in white pattern
8	Package Vibration	1.04G,Frequency : 20~200Hz Direction : X,Y,Z Duration: 30 minutes in each direction	Full packed for shipment
9	Package Drop Impact	Drop from height of 100 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment
10	UV exposure Resistance	765 W/m² for 168hrs,40°C	
11	Electrostatic discharge	Machine model: +/-250V,0Ω ,200pF	

Actual EMC level to be measured on customer application.

Note1: Stay white pattern for storage and non-operation test.

Note2: Operation is black/white pattern , hold time is 150S.

Note3: The function ,appearance, opticals should meet the requirements of the test before and after the test.

Note4: Keep testing after 2 hours placing at 20°C-25°C.

19.2 Product life time

Reliability estimation testing with accelerated life-time theory would be demonstrated to provide confidence of EPD lifetime.

19.3 Product warranty

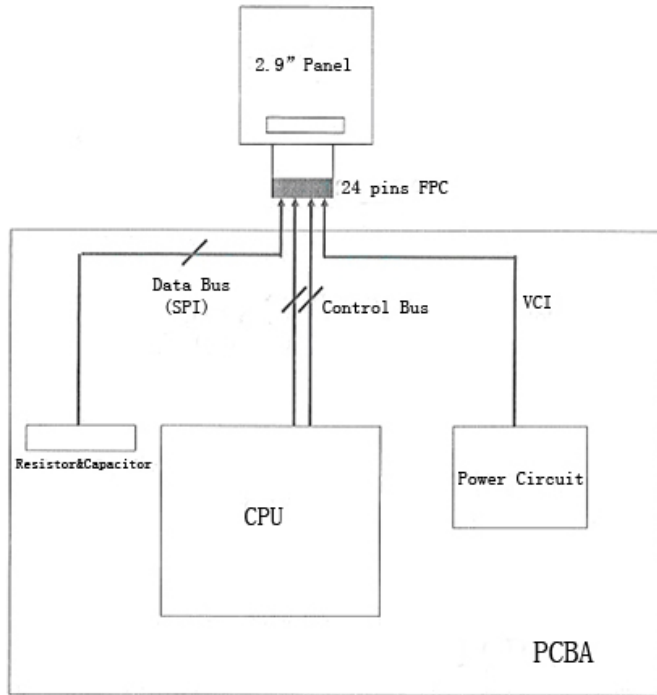
Warranty conditions have to be negotiated between Xingtai and individual customers.

Xingtai provides 12+1(one month delivery time) months warranty for all products which are purchased from Xingtai.

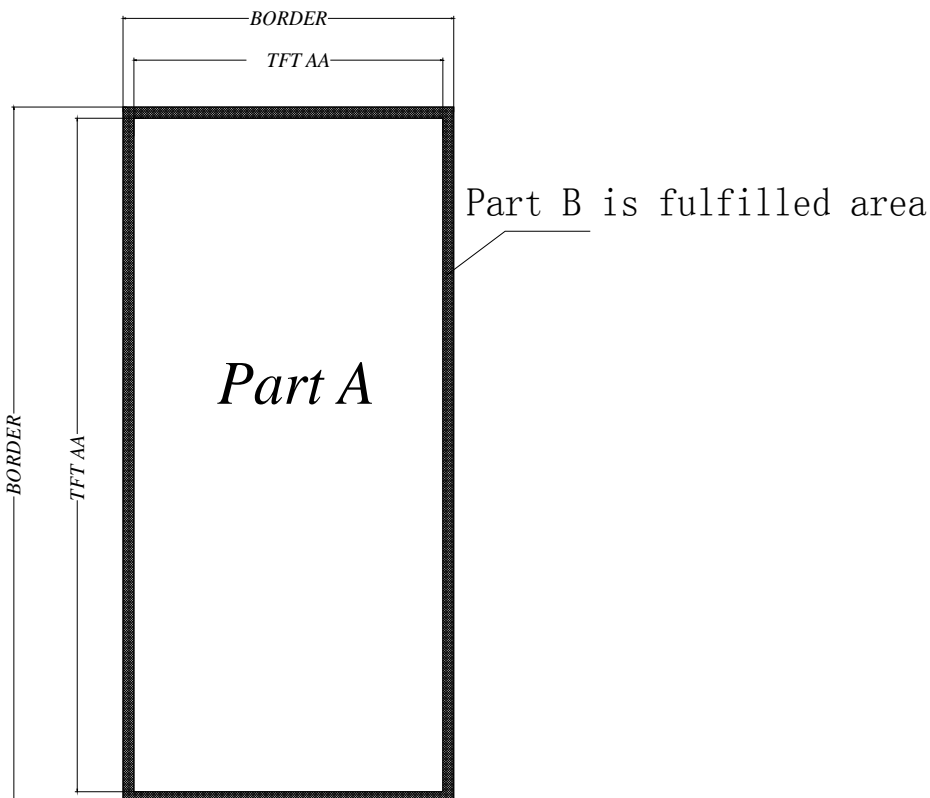


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20. Block Diagram



21. PartA/PartB specification





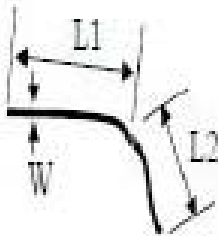
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22. Point and line standard

Shipment Inspection Standard						
Equipment: Electrical test fixture, Point gauge						
Outline dimension	36.7(H)×79.0 (V) × 0.9(D)	Unit: mm	Part-A	Active area	Part-B	Border area
Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle
	19°C~25°C	55%±5%RH	800~1300Lux	300 mm	35Sec	
Defect type	Inspection method	Standard		Part-A	Part-B	
Spot	Electric Display	D≤0.25 mm		Ignore	Ignore	
		0.25 mm < D ≤ 0.4 mm		N≤4	Ignore	
		D > 0.4 mm		Not Allow	Ignore	
Display unwork	Electric Display	Not Allow		Not Allow	Ignore	
Display error	Electric Display	Not Allow		Not Allow	Ignore	
Scratch or line defect(include dirt)	Visual/Film card	L≤2 mm, W≤0.2 mm		Ignore	Ignore	
		2.0mm < L ≤ 5.0mm, 0.2 < W ≤ 0.3mm,		N≤2	Ignore	
		L > 5 mm, W > 0.3 mm		Not Allow	Ignore	
PS Bubble	Visual/Film card	D≤0.2mm		Ignore	Ignore	
		0.2mm ≤ D ≤ 0.35mm		N≤4	Ignore	
		D > 0.35 mm		Not Allow	Ignore	
Side Fragment	Visual/Film card	X≤6mm, Y≤0.4mm, Do not affect the electrode circuit (Edge chipping) X≤1mm, Y≤1mm, Do not affect the electrode circuit((Corner chipping) Ignore				
Remark	1. Appearance defect should not cause electrical defects;					
	2. Appearance defects should not cause dimensional accuracy problems					
	L=long W=wide D=point size N=Defects NO					

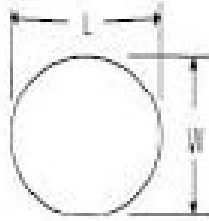


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$$L = L1 + L2$$

Line Defect



$$D = (L + W) / 2$$

Spot Defect

L=long W=wide D=point size



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23.Barcode

23.1 Babel appearance



ABBBBBBBCC
DDDEEEFGGG

23.2 QR scanned information (Total 28 code number+ 2 blank spaces)

A BBBBBBBB CC DDD EEE F GGG H III J KKK
 ① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑪

- ① A——The factory code
- ② BBBBBBBB——Module name of EPD
- ③ CC——FPL model name
- ④ DDD——Date of production
- ⑤ EEE——Production lot
- ⑥ F——Separator
- ⑦ GGG——FPL Lot
- ⑧ H——Normal Lot
- ⑨ III——TFT、PS、EC.
- ⑩ J——IC
- ⑪ KKK——Serial NO.
- blank spaces



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24. Packing

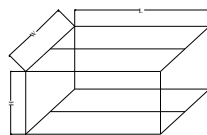
Packing Spec

Sheet No :

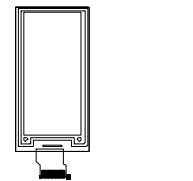
	Part No	HINK-E029A115	DATE	2020. 11. 19	VER	A0	Page	2-1
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一, Package Type: Box

Box No	Holitech shipping box
Box size	515*322*170
Containment	240PCS

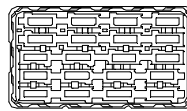


PRODUCT DRAWING



二, Inside package type: Plastic Tray
Tray unit: mm

Plastic Tray	465*280*15	13 pcs
Anti-static foil bags	700*530*0.1	1 pcs
EPE (inside)	408.86*231.5*2	12 pcs
EPE (Up-Down)	485*145*10	2 pcs
EPE (Left-Right)	285*480*10	2 pcs
EPE (Front-back)	310*145*10	2 pcs
Chip board	500*306*5	2 pcs
Quantity/tray	20 pcs	
Tray number/sheet	12+1 Sheets	
Box	1	



Step 1:

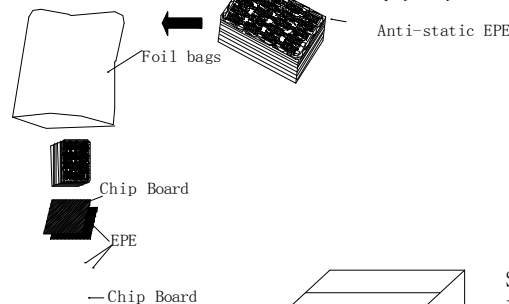
Material: Tray, EPE
Put the product in to the tray and keep the display side up. Then put anti-static EPE in to each holes.

Step 2:

1) Must keep the angle 180 degree placed between the neighboring Plastic trays.
2) There are 12 layers product, total 20*12=240 pcs.
3) An empty Plastic tray intersects put on the top of the plastic trays.

Step 3:

1) In each case, put 2 bags of desiccant, then seal the trays with adhesive tapes.
2) Put the trays into foil bags.
3) heat seal the foil bags.



Step 4:

1) First put a chip board on the bottom of the box, then placed the down EPE, the left - right and front -back EPE.
2) Placed the sealed products into the box.
3) The last placed the up EPE on the top of the trays, and place a chip board on it.

Step 5:

1) Seal the box with adhesive tapes .
2) Paste the lable onto the exterior box, and the lable can't cover the safety , transfer and RoSH sign.

Design	X. Z. P	Approve	H. Z. P	Confirm	X.X.M
Date	2020. 11. 19	Date	2020. 11. 19	Date	2020. 11. 19



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Packing Spec

Sheet No

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The label outside the carton print as below

90.00	
Label	
Customer Part No	
Customers Item No	A
MFG order No	B
MFG batch No	C
QTY	D
G. W	E
N. W	F
MFG Date	J
Carton No	
Remark	

NOTE:

1. "A" Print customer Item No
2. "B" Print customer Order No
3. "C" Print MFG Batch No (Separate packing for different batch products. Mixed packing available for the odd number of different batch print all the batch NO&QTY accordingly if happened.
4. "D" Print product qty
5. "E" Print the G. W
6. "F" Print the N. W
7. "J" Print the MFG date
8. Before packing make sure the FPL batch , item and qty are the same as which on the Final passed card.

Design	X. Z. P	Approve	H. Z. P	Confirm	X.X.M
Date	2020. 11. 19	Date	2020. 11. 19	Date	2020. 11. 19