

SPECIFICATIONS

CUSTOMER : CCN552

SAMPLE CODE : SE1602WRT-017-L-Q

MASS PRODUCTION CODE : PE1602WRT-017-L-Q

SAMPLE VERSION : 01

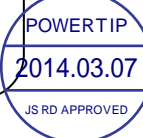
SPECIFICATIONS EDITION : 002

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Customer Approved

Date:



Approved	Checked	Designer
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- ☐ Preliminary specification for design input
- ☒ Specification for sample approval

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RECORDS OF REVISION

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Total : 32Pages

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1. SPECIFICATIONS

1.1 Features

Item	Standard Value
Display Type	16 * 2 Characters
LCD Type	FSTN, Black Negative, Transmissive, Extended temp
Driver Condition	LCD Module :1/16Duty, 1/5Bias
Viewing Direction	12H
Weight	17g
Interface	I ² C interface / serial interface
Other(controller IC)	ST7032i
ROHS	THIS PRODUCT CONFORMS THE ROHS OF PTC Detail information please refer web site : http://www.powertip.com.tw/news.php?area_id_view=1085560481/

1.2 Mechanical Specifications

Item	Standard Value	Unit
Outline Dimension	70.0(L)*32.0(W)*4.7(H)	mm
Viewing Area	63.0(L)*18.0(W)	mm
Active Area	56.21(L)*11.5(W)	mm
Character Size	2.96(L) *5.56(W)	mm
Characte Pitch	3.55(L) *5.94 (W)	mm

Note : For detailed information please refer to LCM drawing

1.3 Absolute Maximum Ratings

Item	Symbol	Condition	Min.	Max.	Unit
Power Supply Voltage	V _{DD}	-	-0.3	6.0	V
LCM Driver Voltage	V _{OP}	-	7.0-VSS	-0.3+VSS	V
Input Voltage	V _{IN}	-	-0.3	V _{DD} +0.3	V
Operating Temperature	T _{OP}	-	-20	70	°C
Storage Temperature	T _{ST}	-	-30	80	°C
Storage Humidity	H _D	Ta < 60 °C	-	90	%RH

1.4 DC Electrical Characteristics

Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic Supply Voltage	V _{DD}	-	3.0	3.3	3.5	V
“H” Input Voltage	V _{IH}	-	1.9	-	V _{DD}	V
“L” Input Voltage	V _{IL}	-	-0.3	-	0.8	V
“H” Output Voltage (SDA ,SCL)	V _{OH1}	I _{OH} = -1.0mA	0.75 V _{DD}	-	-	V
“L” Output Voltage (SDA ,SCL)	V _{OL1}	I _{OL} = 1.0mA	-	-	0.8	V
“H” Output Voltage (Except SDA ,SCL)	V _{OH2}	I _{OH} = -0.04mA	0.8V _{DD}	-	V _{DD}	V
“L” Output Voltage (Except SDA ,SCL)	V _{OL2}	I _{OL} = 0.04mA	-	-	0.2V _{DD}	V
Supply Current	I _{DD}	VDD=3.3V;VOP=4.5V; Pattern= Horizontal line *1	-	0.3	0.5	mA
LCM Driver Voltage	V _{OP} *2	25°C	4.3	4.5	4.7	V

NOTE: *1 The Maximum current display

*2 The VOP test point is V0-VSS

1.5 Optical Characteristics

LCD Panel : :1/16 Duty , 1/5 Bias , $V_{LCD} = 4.5V$, $T_a = 25^{\circ}C$

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Reference
Response Time	Rise	tr	-	-	162	243	ms	Note2
	Fall	tf		-	92	138		
Viewing angle range	Top	Θ+	C≥2.0	-	35	-	Deg.	Notes 1
	Bottom	Θ-		-	30	-		
	Left	ΘL		-	45	-		
	Right	ΘR		-	45	-		
Contrast Ratio		CR	-	-	84	-	-	Note 3
Average Brightness (with LCD) *2		IV	VF=6.5V	80	100	-	cd/m ²	Note 4
CIE Color Coordinate (With LCD) *1		X		0.24	0.29	0.34	-	
		Y		0.29	0.34	0.39		
Uniformity *1		△B			70	-	-	

Note 4 :

1 : $\Delta B = B(\min) / B(\max) * 100\%$

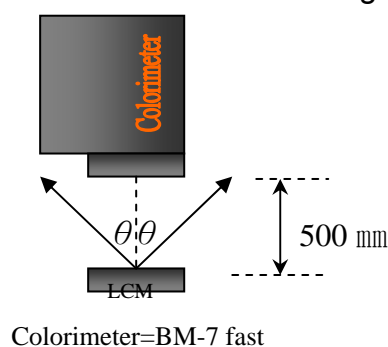
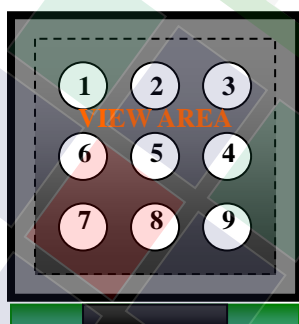
2 : Measurement Condition for Optical Characteristics:

a : Environment: $25^{\circ}C \pm 5^{\circ}C$ / $60 \pm 20\% R.H$, no wind , dark room below 10 Lux at typical lamp current and typical operating frequency.

b : Measurement Distance: $500 \pm 50 \text{ mm}$, ($\theta = 0^{\circ}$)

c : Equipment: TOPCON BM-7 fast , (field 1°) , after 10 minutes operation.

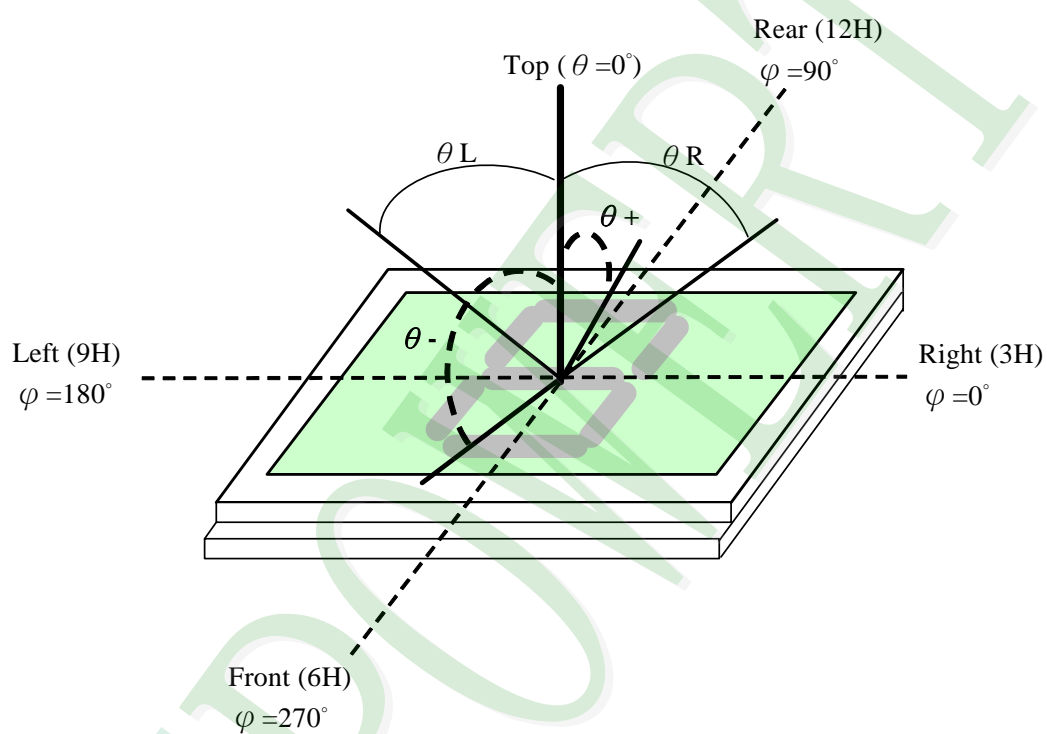
d : The uncertainty of the C.I.E coordinate measurement ± 0.01 , Average Brightness $\pm 4\%$



Note 1.

Optical characteristics-2

Viewing angle

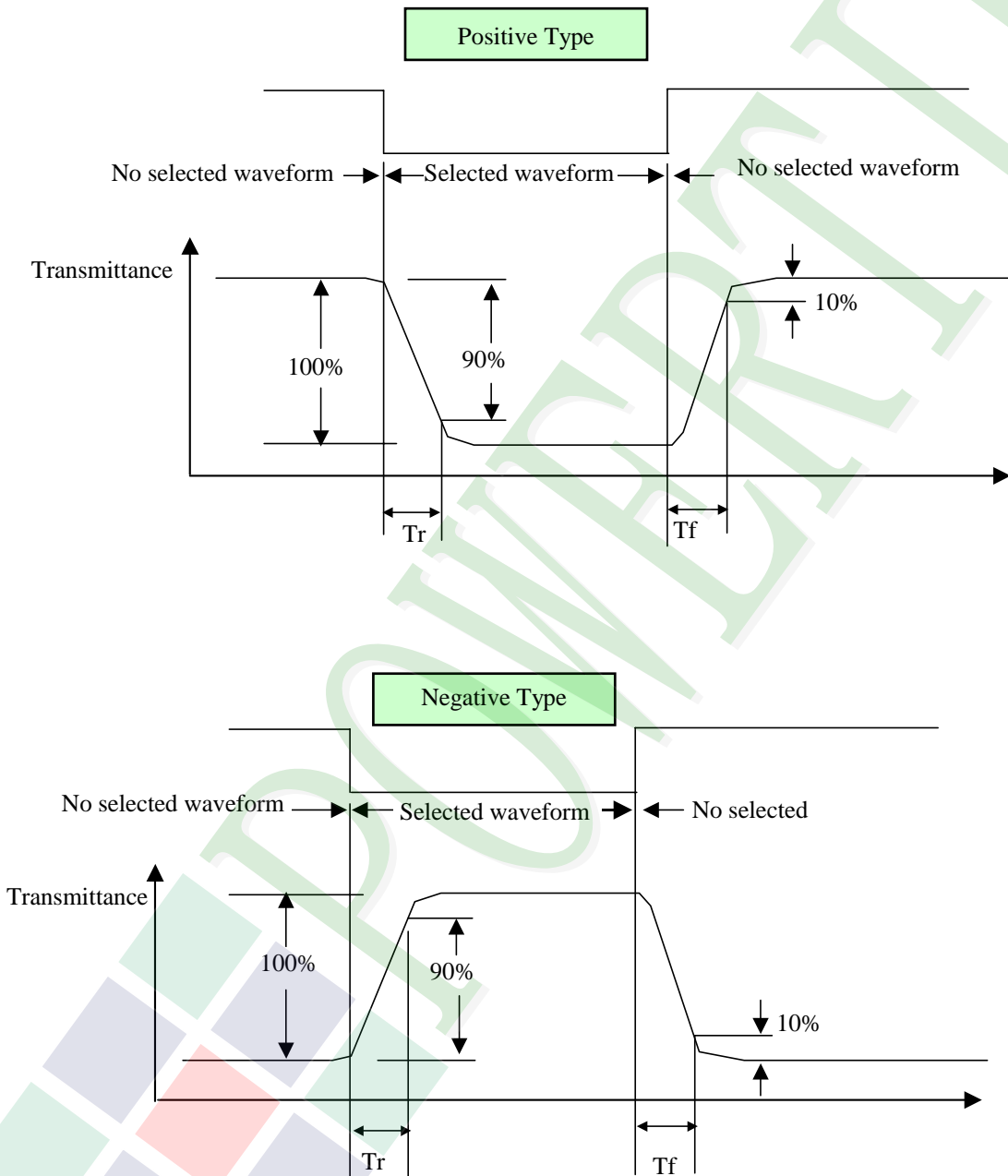


Viewing angle

Note 2.

Optical characteristics-3

Fig.2 Definition of response time



Electrical characteristics-2

※2 Drive waveform

V_{op} : Drive voltage

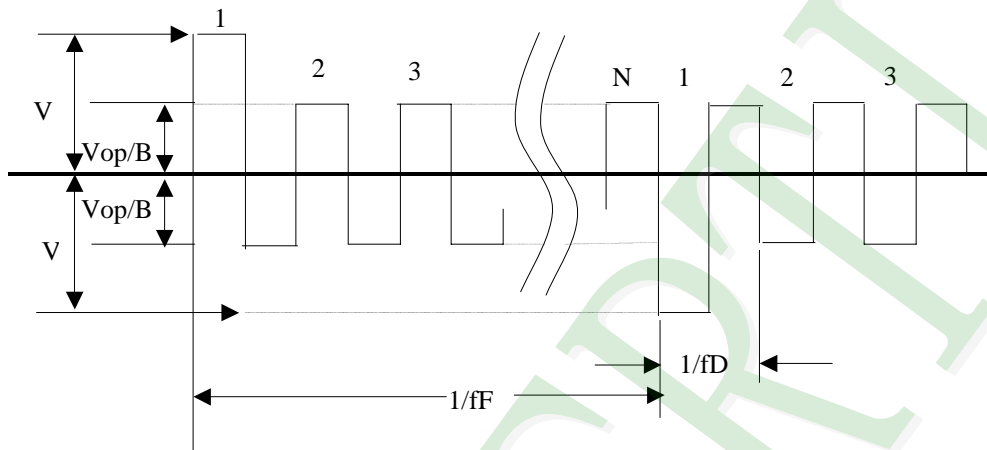
$1/B$: Bias

N : Duty

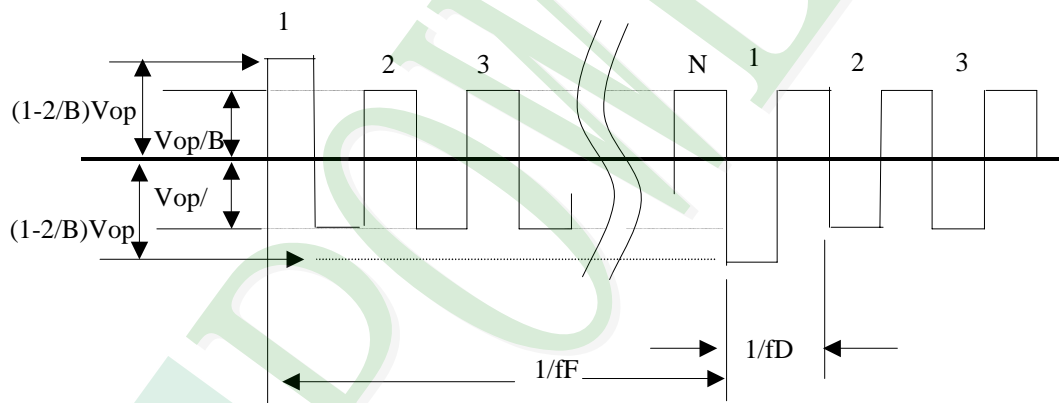
f_F : Frame frequency

f_D : Drive frequency

(1) Selected waveform



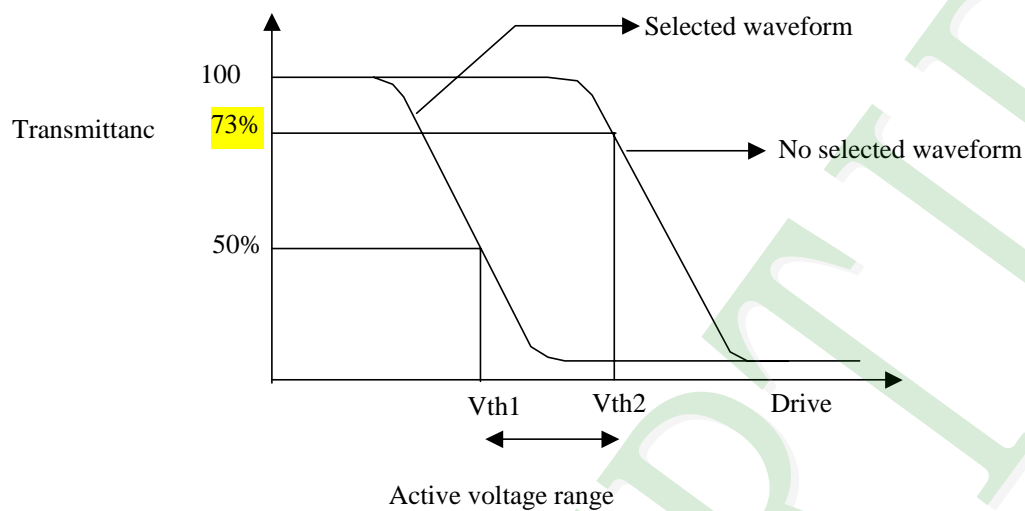
(2) Non- Selected wave form



Note:

Frame frequency is defined as follows: Common side supply voltage peak - to - peak / 2 = 1 period

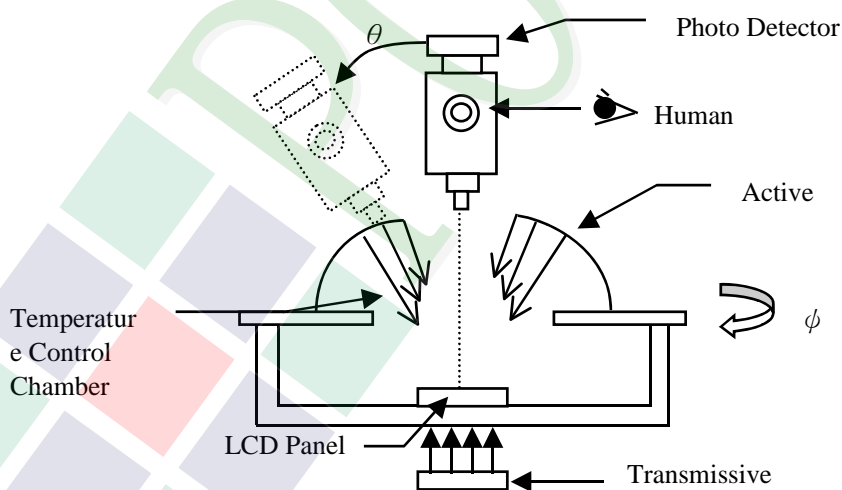
Note 3. : Definition of Vth



	Vth1	Vth2
View direction	10°	40°
Drive waveform	(Selected waveform)	(No selected waveform)
Transmittance	50%	73%

※1 Contrast ratio
= (Brightness in OFF state) / (Brightness in ON state)

Outline of Electro-Optical Characteristics Measuring System



1.6 Backlight Characteristics

Maximum Ratings

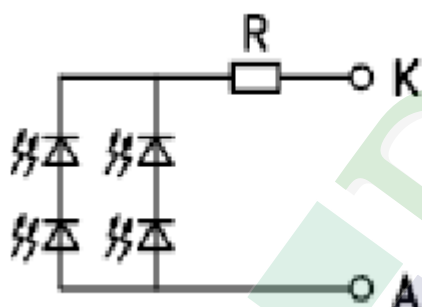
Item	Symbol	Conditions	Min.	Max.	Unit
Peak Forward Current	I_{FP}	$T_a = 25^{\circ}\text{C}$	-	40	mA
Reverse Voltage	V_R	$T_a = 25^{\circ}\text{C}$	-	8	V
Power Dissipation	PD	$T_a = 25^{\circ}\text{C}$	-	260	mw

Electrical / Optical Characteristics

$T_a = 25^{\circ}\text{C}$

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Reverse Current	IR	Vr= 8V	-	-	100	μA
Forward Current	IF	VF=6.5V	-	30	40	mA
Average Brightness (Without LCD)	IV		500	600	-	cd/m ²
CIE Color Coordinate (Without LCD)	X		0.24	-	0.32	-
	Y		0.24	-	0.32	
Color	White					

Circuit Diagram



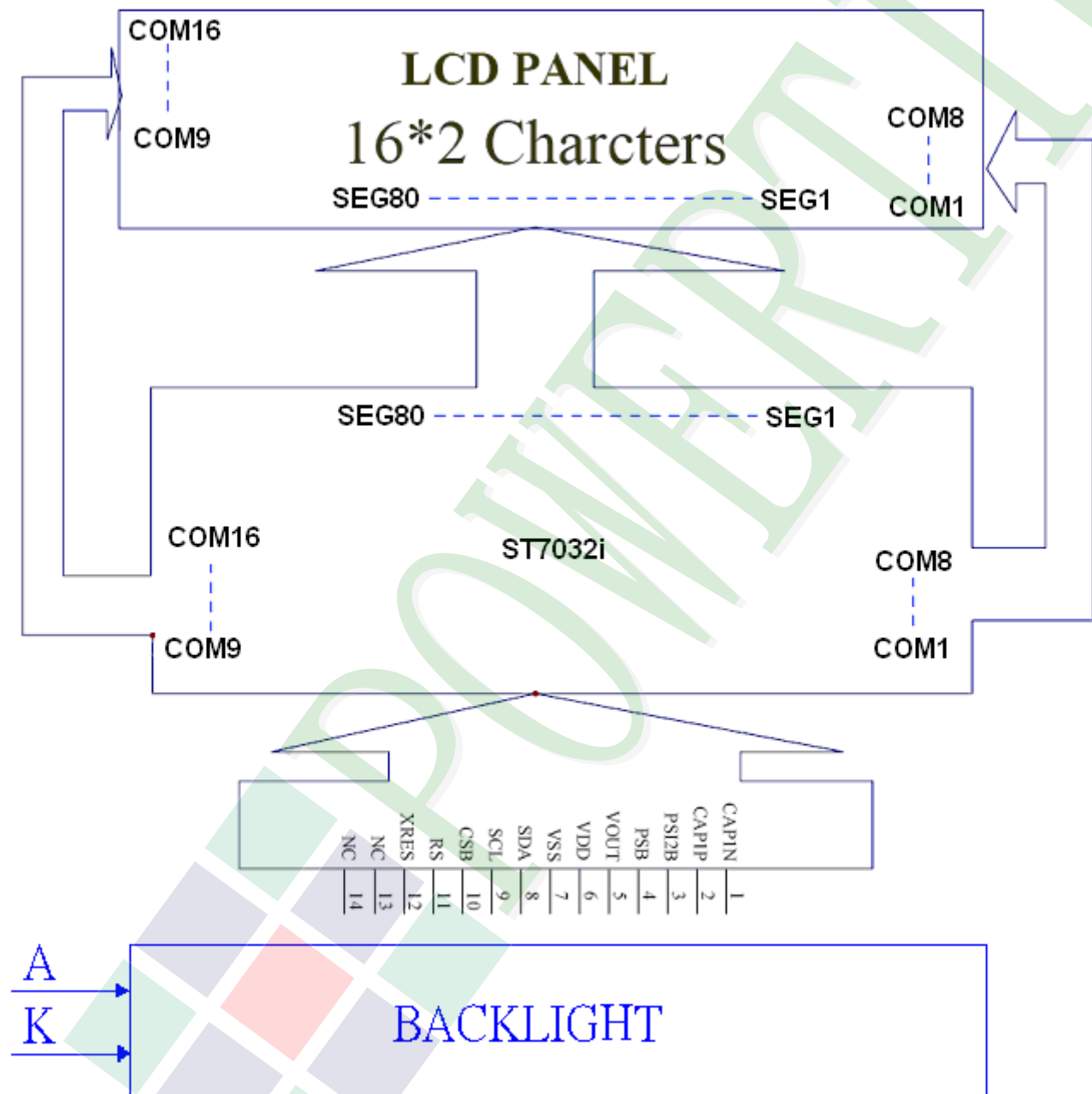
2. MODULE STRUCTURE

2.1 Counter Drawing

2.1.1 LCM Mechanical Diagram

* See Appendix

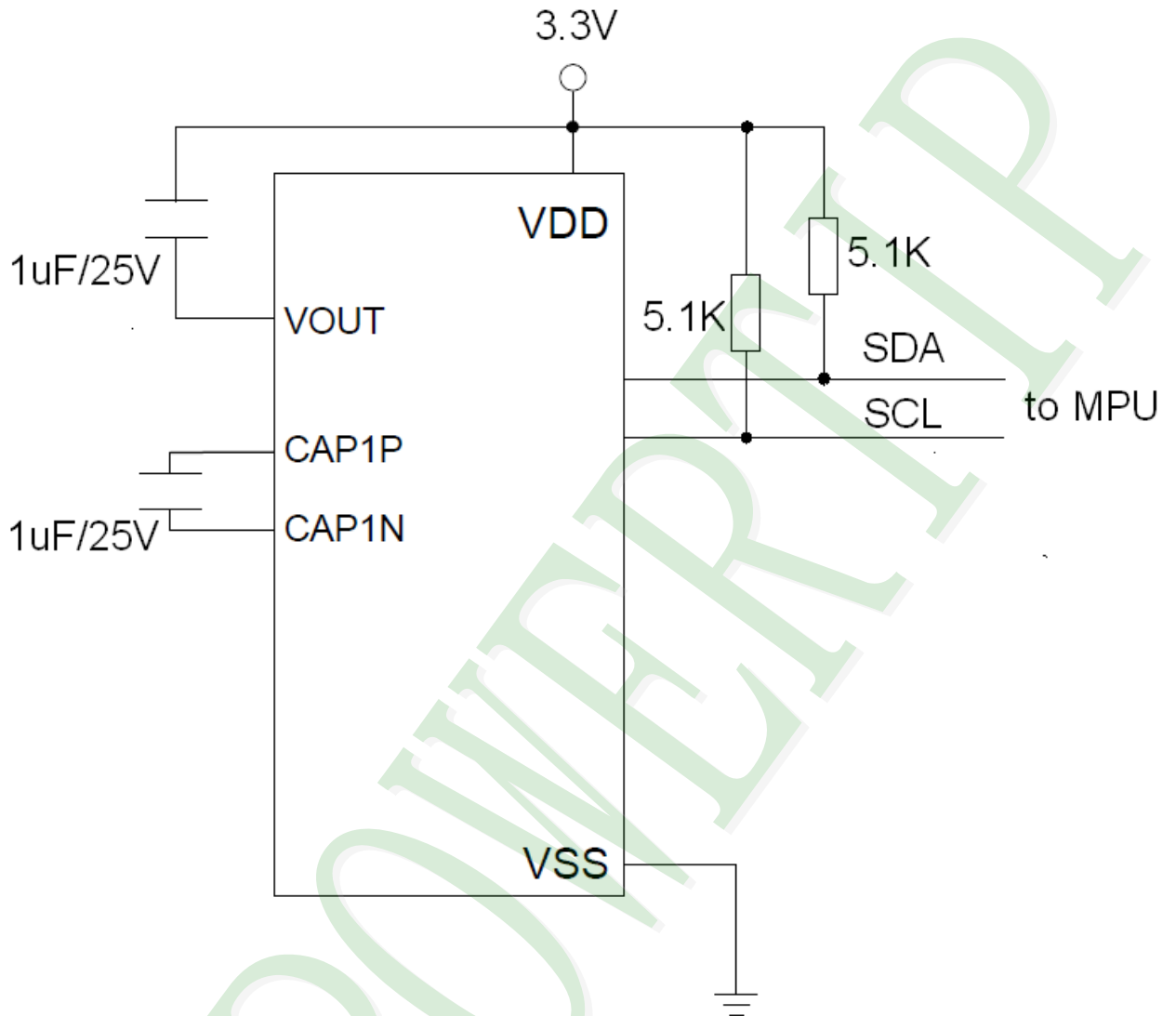
2.1.2 Block Diagram



2.2 Interface Pin Description

Pin No.	Symbol	Function								
1	CAP1N	For voltage booster circuit(VDD-VSS). Connect a capacitor (1uF) between them.								
2	CAP1P									
3	PSI2B	<table><tr><td>PSB</td><td>PSI2B</td><td>Interface</td></tr><tr><td>0</td><td>1</td><td>Serial interface</td></tr></table>			PSB	PSI2B	Interface	0	1	Serial interface
PSB	PSI2B				Interface					
0	1	Serial interface								
4	PSB	<table><tr><td>1</td><td>0</td><td>I²C interface</td></tr></table>			1	0	I ² C interface			
1	0	I ² C interface								
5	VOUT	DC/DC voltage converter. Connect a capacitor (1uF) between this terminal and VDD.								
6	VDD	Power supply.(VDD=3.3V)								
7	VSS	Ground.								
8	SDA	Input data. Connect a resister (5.1K) to VDD in I ² C interface.								
9	SCL	Input clock. Connect a resister (5.1K) to VDD in I ² C interface.								
10	CSB	Chip select in serial interface; Low active.								
11	RS	Select registers 0:instruction register(for write) 1:data register (for write and read) For I2C interface mode, must be connect to VDD.								
12	XRES	Reset pin, Low active.								
13	NC	NC								
14	NC	NC								

2.2.1 Application Notes



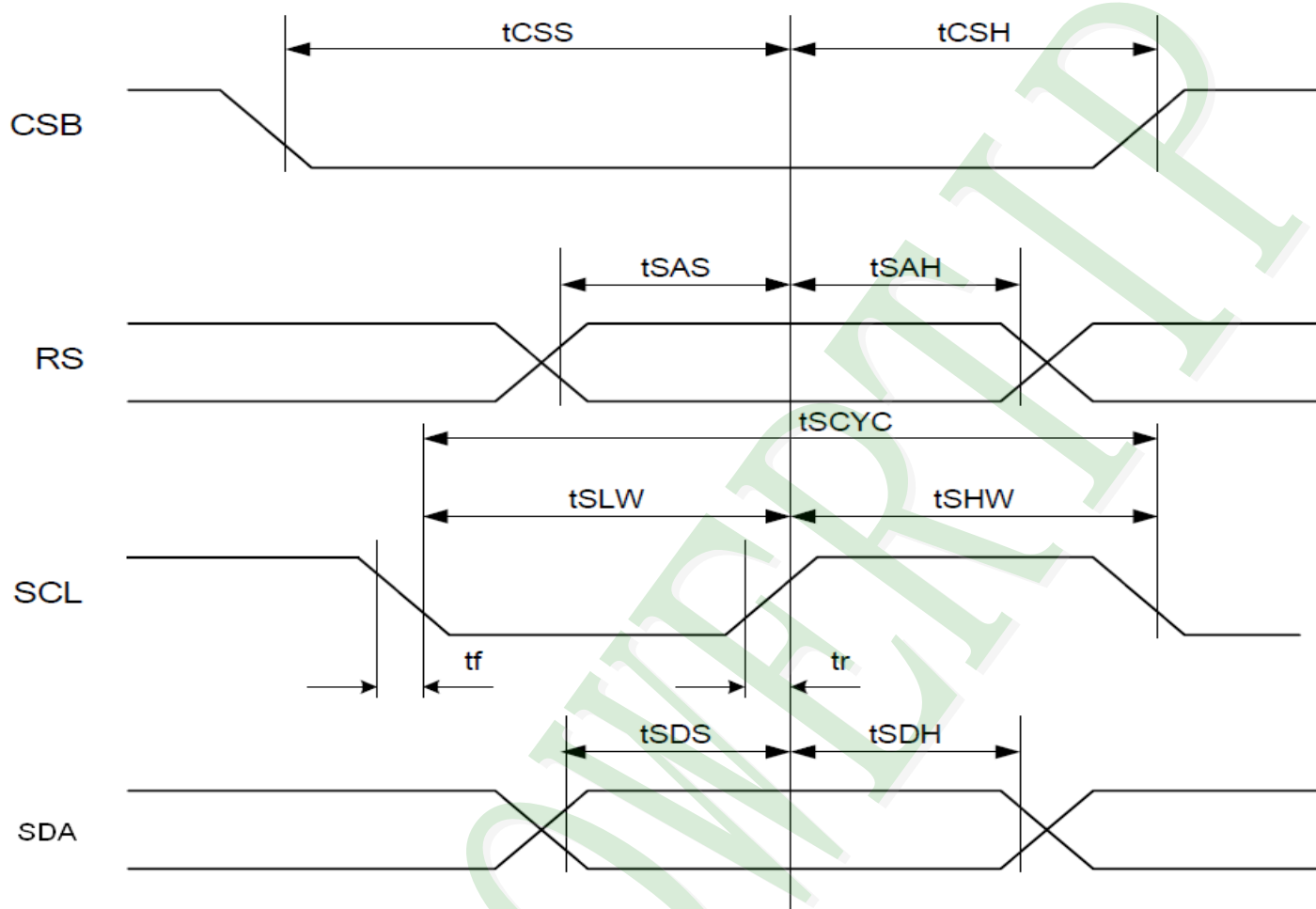
Note : In Serial interface please remove the resistors

2.2.2 Refer Initial Code

```
write_com(0x7c);    //;Set slave address SDA0,1=11
write_com(0x00);    //;Send control byte
write_com(0x38);    //;function set
write_com(0x39);    //;function set
write_com(0x14);    //;internal osc frequency
write_com(0x79);    //;contrast set(C3~C0)
write_com(0x54);    //;power/icon(0)/contrast control
write_com(0x6e);    //;follower control
write_com(0x0c);    //;display on/off control
write_com(0x01);    //;clear display
write_com(0x06);    //;entry mode set
```

2.3 Timing Characteristics

Serial Interface

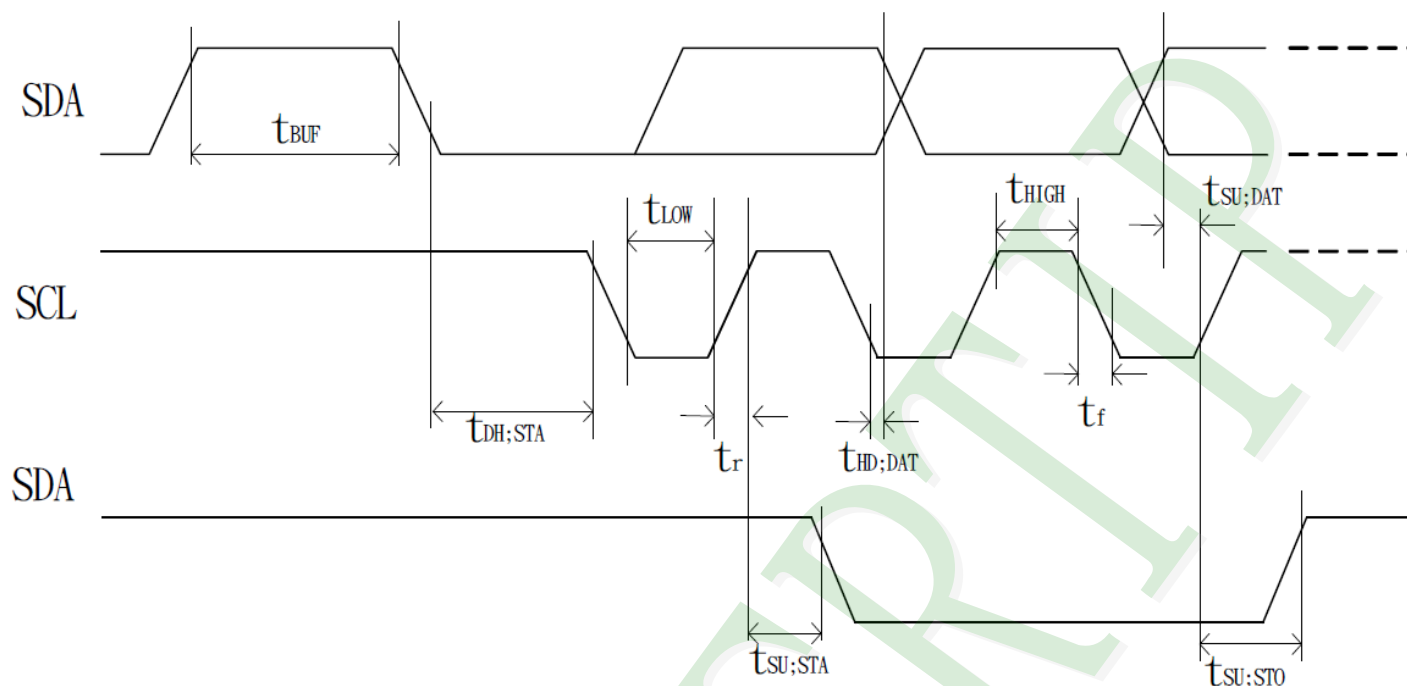


(VDD=3.0~3.5V Ta = 25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Units
Serial Clock Period	SCL	t_{SCYC}	—	200	-	ns
SCL "H" pulse width		t_{SHW}		20	-	
SCL "L" pulse width		t_{SLW}		160	-	
SCL Rise/Fall time	SCL	t_r, t_f	—	-	20	ns
Address setup time	RS	t_{SAS}	—	10	-	ns
Address hold time		t_{SAH}		250	-	
Data setup time	SDA	t_{SDS}	—	10	-	ns
Data hold time		t_{SDH}		10	-	
CS-SCL time	CS	t_{CSS}	—	20	-	ns
		t_{CSH}		350	-	

*1 All timing is specified using 20% and 80% of VDD as the standard.

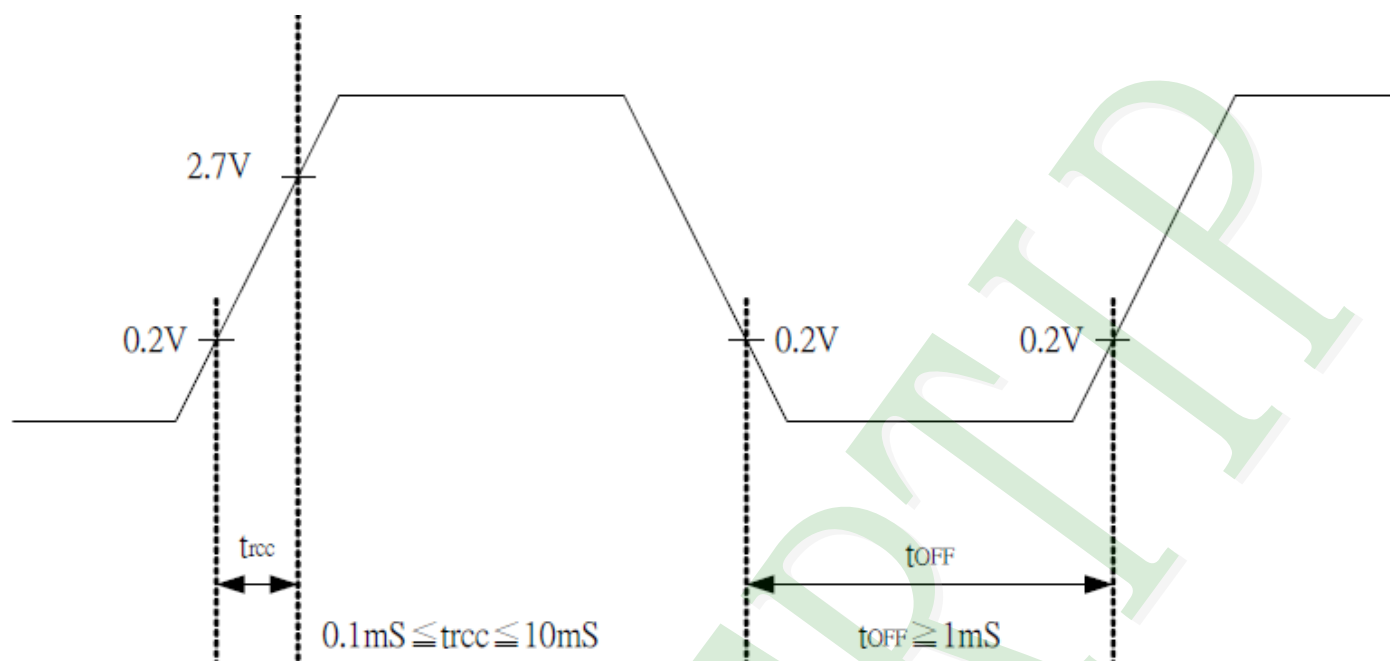
I²C interface



(VDD=3.0~3.5V Ta = 25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Units
SCL clock frequency	SCL	f_{SCLK}	—	DC	400	KHz
SCL clock low period		t_{LOW}		1.3	—	us
SCL clock high period		t_{HIGH}		0.6	—	
Data set-up time	SDA	$t_{SU;DAT}$	—	180	—	ns
Data hold time		$t_{HD;DAT}$		0	0.9	us
SCL,SDA rise time	SCL, SDA	t_r	—	$20+0.1C_b$	300	ns
SCL,SDA fall time		t_f		$20+0.1C_b$	300	
Capacitive load represent by each bus line		C_b	—	—	400	pf
Setup time for a repeated START condition	SDA	$t_{SU;STA}$	—	0.6	—	us
Start condition hold time		$t_{HD;STA}$	—	0.6	—	us
Setup time for STOP condition		$t_{SU;STO}$	—	0.6	—	us
Bus free time between a Stop and START condition	SCL	t_{BUF}	—	1.3	—	us

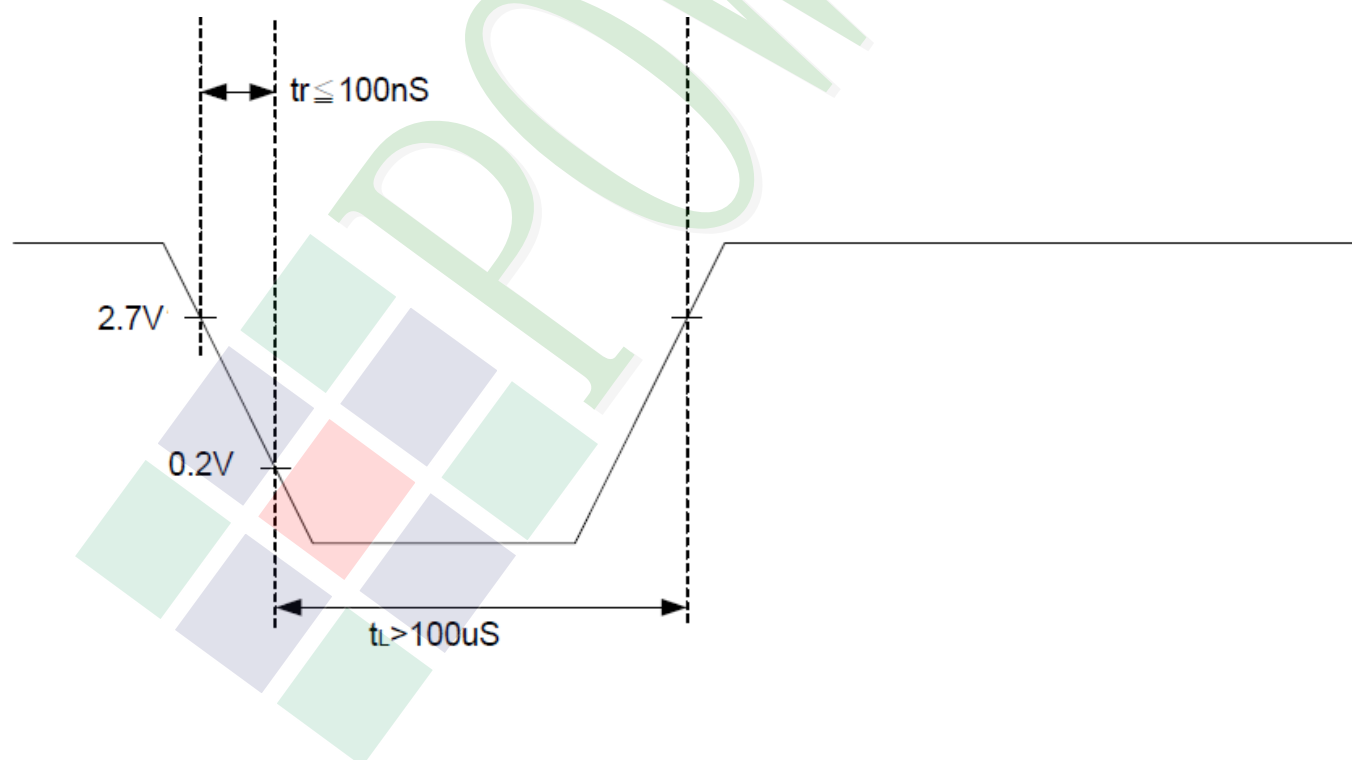
Internal Power Supply Reset



Notes:

1. t_{OFF} compensates for the power oscillation period caused by momentary power supply oscillations.
2. If 2.7V is not reached, internal reset circuit will not operate normally.

Hardware reset (XRES)



2.4 Function Description For I²C interface

It just only could write Data or Instruction to ST7032 by the IIC Interface.

It could not read Data or Instruction from ST7032 (except Acknowledge signal).

SCL: serial clock input

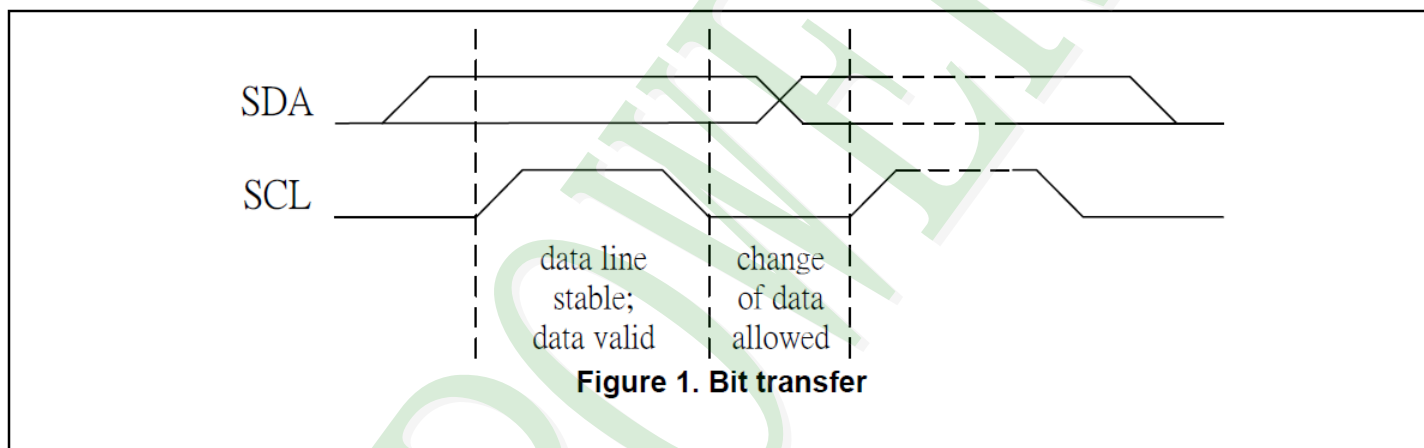
SDA: serial data input

Slaver address could only set to 0111110, no other slaver address could be set

The I2C interface send RAM data and executes the commands sent via the I2C Interface. It could send data bit to the RAM .The I2C Interface is two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

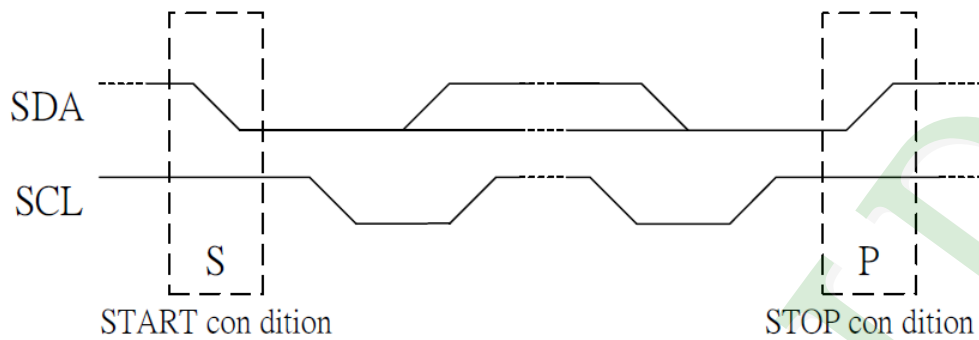
BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Fig.1.



START AND STOP CONDITIONS

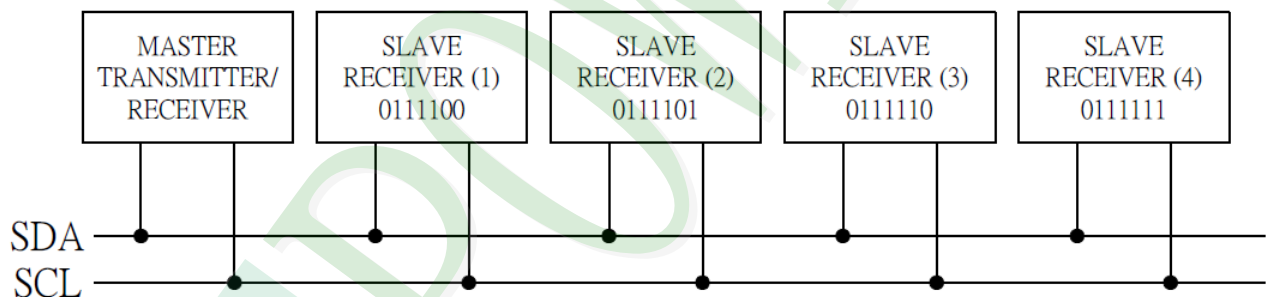
Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.2.



SYSTEM CONFIGURATION

The system configuration is illustrated in Fig.3.

- Transmitter: the device, which sends the data to the bus
- Master: the device, which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.

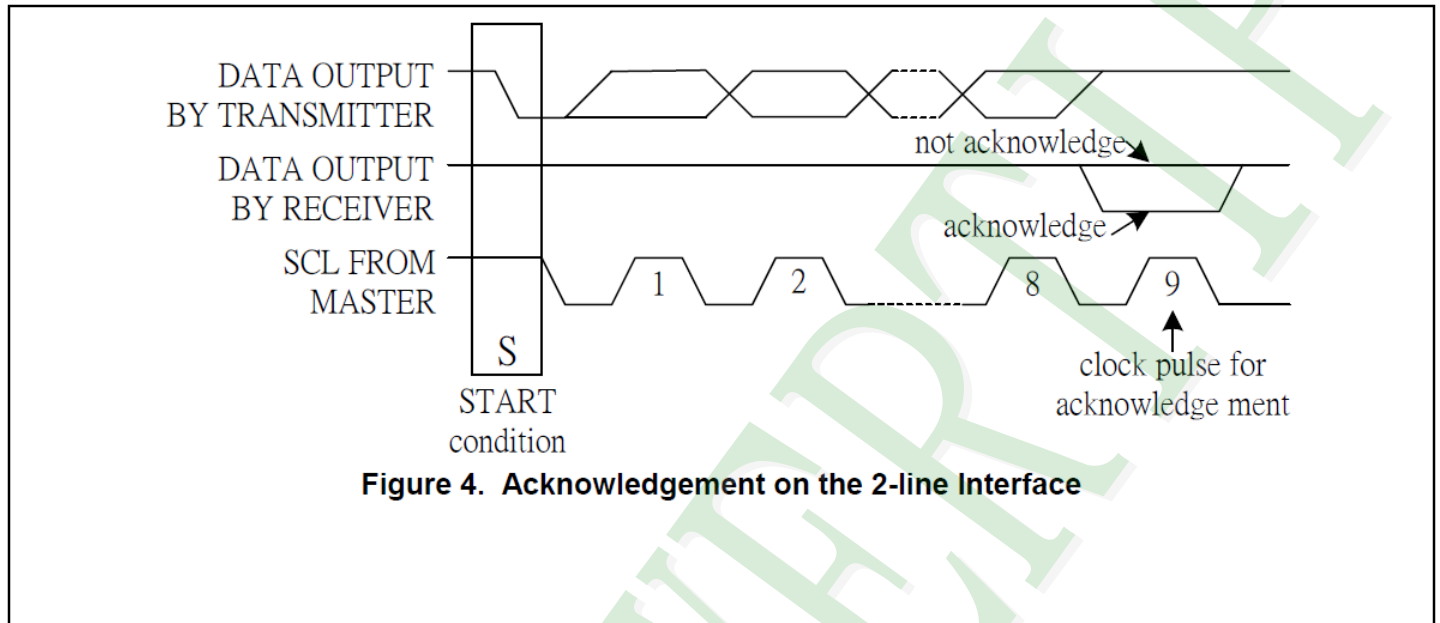


ACKNOWLEDGE

Acknowledge is not Busy Flag in I2C interface.

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the

acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I2C Interface is illustrated in Fig.4.



I2C Interface protocol

The ST7032 supports command, data write addressed slaves on the bus. Before any data is transmitted on the I2C Interface, the device, which should respond, is addressed first. Only one 7-bit slave addresses (0111110) is reserved for the ST7032. The R/W is assigned to 0 for Write only. The I2C Interface protocol is illustrated in Fig.5.

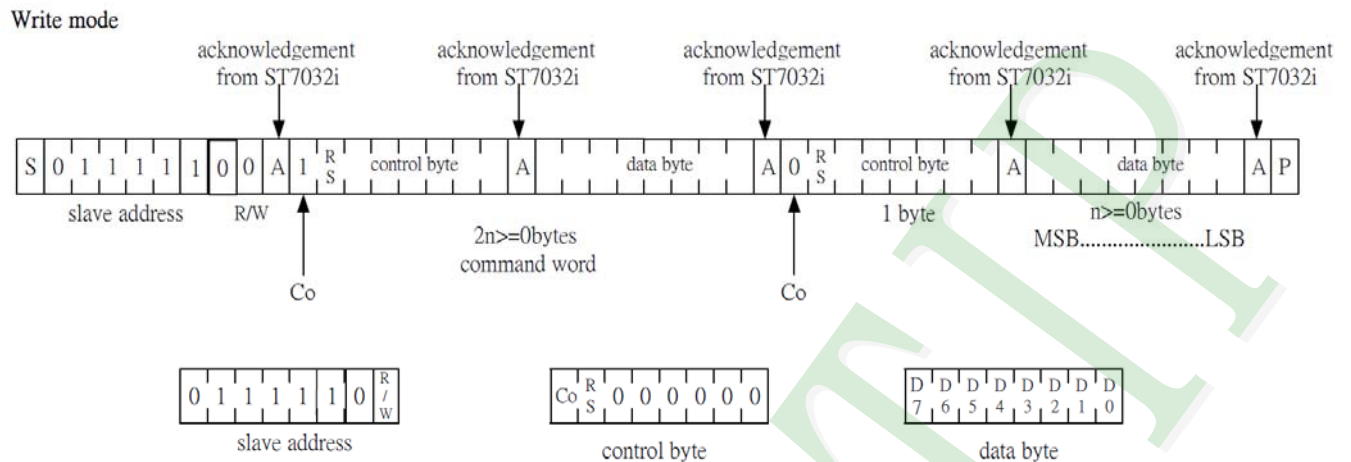


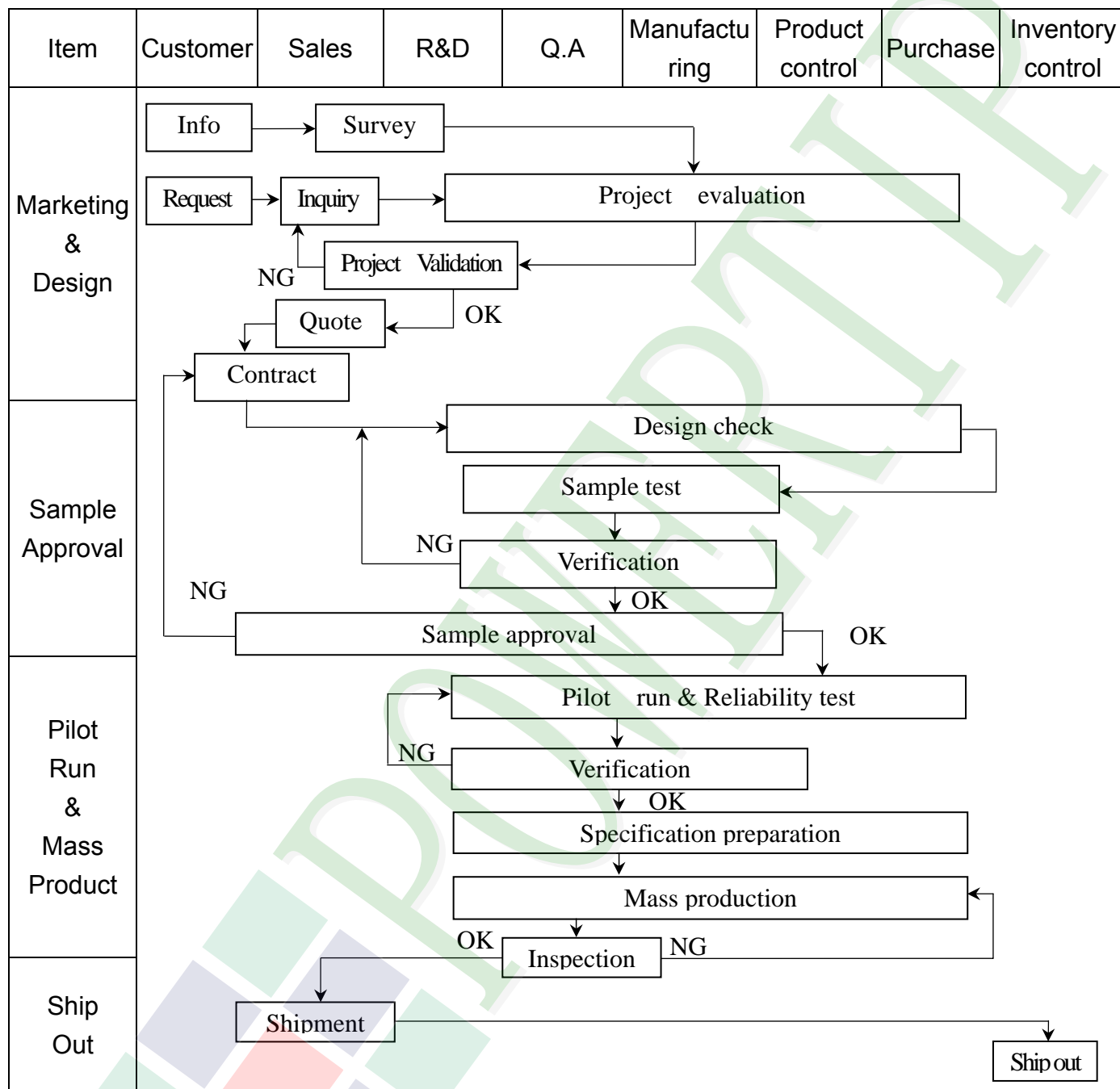
Figure 5. 2-line Interface protocol

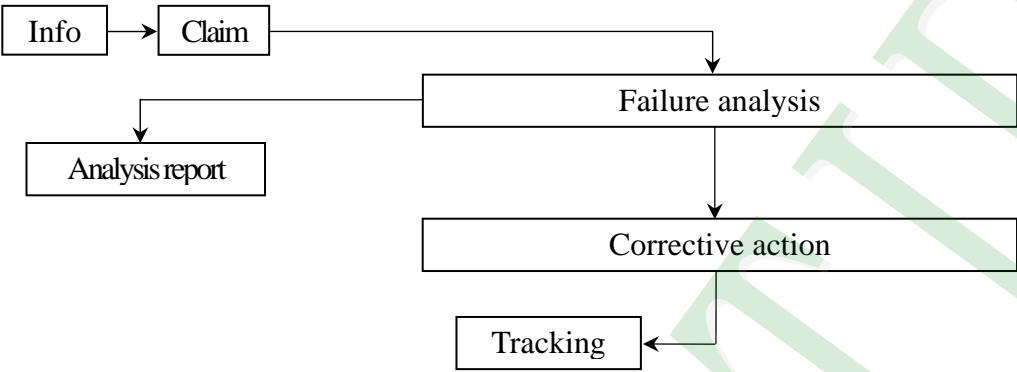
Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by a STOP condition.
	1	Another control byte will follow the data byte unless a STOP condition is received.

The sequence is initiated with a START condition (S) from the I2C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I2C Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines Co and RS, plus a data byte. The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the RS bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the RS bit setting; either a series of display data bytes or command data bytes may follow. If the RS bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended ST7032i device. If the RS bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the I2C INTERFACE-bus master issues a STOP condition (P).

3. QUALITY ASSURANCE SYSTEM

3.1 Quality Assurance Flow Chart



Item	Customer	Sales	R&D	Q.A	Manufacturing	Product control	Purchase	Inventory control
Sales Service	 <pre> graph TD Info[Info] --> Claim[Claim] Claim --> AnalysisReport[Analysis report] Claim --> FailureAnalysis[Failure analysis] FailureAnalysis --> CorrectiveAction[Corrective action] CorrectiveAction --> Tracking[Tracking] </pre>							
Q.A Activity	1. ISO 9001 Maintenance Activities 3. Equipment calibration 5. Standardization Management				2. Process improvement proposal 4. Education And Training Activities			

3.2. Inspection Specification

◆ **Scope** : The document shall be applied to LCD Module for Monotype and Color STN(Ver. B01).

◆ **Inspection Standard** : MIL-STD-105E Table Normal Inspection Single Sampling Level II .

◆ **Equipment** : Gauge 、 MIL-STD 、 Powertip Tester 、 Sample

◆ **Defect Level** : Major Defect AQL : 0.4 ; Minor Defect : AQL : 1.5 .

◆ **OUT Going Defect Level** : Sampling .

◆ **Manner of appearance test** :

(1). The test be under 20W×2 fluorescent light ' and distance of view must be at 30 cm.

(2). Standard of inspection : (Unit : mm)

(3). The test direction is base on about around 45° of vertical line. (Fig. 1)

(4). Definition of area . (Fig. 2)

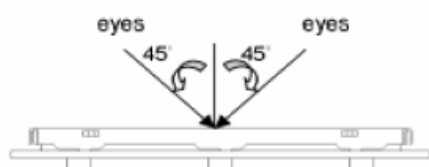


Fig.1

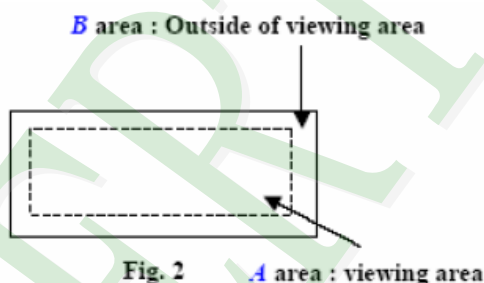


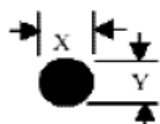
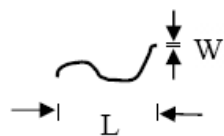
Fig. 2

◆ **Specification:**

NO	Item	Criterion	Level
01	Product condition	1. 1 The part number is inconsistent with work order of Production.	Major
		1. 2 Mixed production types.	Major
		1. 3 Assembled in inverse direction.	Major
02	Quantity	2. 1 The quantity is inconsistent with work order of production.	Major
03	Outline dimension	3. 1 Product dimension and structure must conform to Structure diagram.	Major
04	Electrical Testing	4. 1 Missing line character and icon.	Major
		4. 2 No function or no display.	Major
		4. 3 Output data is error.	Major
		4. 4 LCD viewing angle defect.	Major
		4. 5 Current consumption exceeds product specifications.	Major

◆ Specification For Monotype and Color STN :

(Ver. B01)

NO	Item	Criterion	Level																																				
05	<p>Black or white dot 、 scratch 、 contamination</p> <p>Round type</p>  <p>$\Phi=(x+y)/2$</p> <p>Line type</p> 	<p>5. 1 Round type:</p> <p>5. 1. 1 display only :</p> <ul style="list-style-type: none">• White and black spots on display ≤ 0.30 mm , no more than 4 white or black spots present.• Densely spaced : NO more than two spots or lines within 3 mm. <p>5. 1. 2 Non-display :</p> <table><thead><tr><th rowspan="2">Dimension (diameter : Φ)</th><th colspan="2">Acceptance (Q'ty)</th></tr><tr><th>A area</th><th>B area</th></tr></thead><tbody><tr><td>$\Phi \leq 0.10$</td><td>Accept no dense</td><td rowspan="3">Ignore</td></tr><tr><td>$0.10 < \Phi \leq 0.20$</td><td>3</td></tr><tr><td>$0.20 < \Phi \leq 0.30$</td><td>2</td></tr><tr><td>Total quantity</td><td>4</td><td></td></tr></tbody></table> <p>5. 1. 3 Line type:</p> <table><thead><tr><th colspan="2">Dimension</th><th colspan="2">Acceptance (Q'ty)</th></tr><tr><th>Length (L)</th><th>Width (W)</th><th>A area</th><th>B area</th></tr></thead><tbody><tr><td>---</td><td>$W \leq 0.03$</td><td>Accept no dense</td><td rowspan="3">Ignore</td></tr><tr><td>$L \leq 3.0$</td><td>$0.03 < W \leq 0.05$</td><td rowspan="2">4</td></tr><tr><td>$L \leq 2.5$</td><td>$0.05 < W \leq 0.075$</td></tr><tr><td>---</td><td>$W > 0.075$</td><td colspan="2">As round type</td></tr></tbody></table>	Dimension (diameter : Φ)	Acceptance (Q'ty)		A area	B area	$\Phi \leq 0.10$	Accept no dense	Ignore	$0.10 < \Phi \leq 0.20$	3	$0.20 < \Phi \leq 0.30$	2	Total quantity	4		Dimension		Acceptance (Q'ty)		Length (L)	Width (W)	A area	B area	---	$W \leq 0.03$	Accept no dense	Ignore	$L \leq 3.0$	$0.03 < W \leq 0.05$	4	$L \leq 2.5$	$0.05 < W \leq 0.075$	---	$W > 0.075$	As round type		Minor
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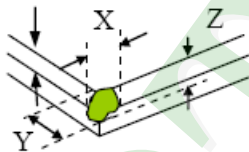
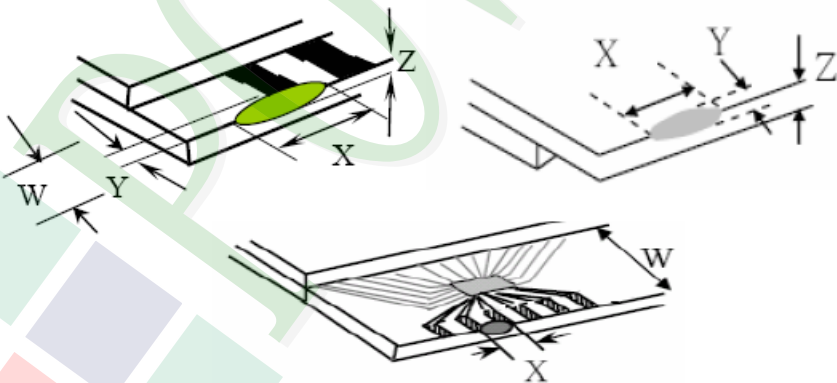
◆ Specification For Monotype and Color STN :

(Ver. B01)

NO	Item	Criterion	Level									
07	The crack of glass	<div> <div> <p>Symbols :</p> <div> <p>X : The length of crack</p> <p>Z : The thickness of crack</p> <p>t : The thickness of glass</p> </div> <div> <p>Y : The width of crack.</p> <p>W : terminal length</p> <p>a : LCD side length</p> </div> </div> <hr/> <p>7.1 General glass chip :</p> <p>7.1.1 Chip on panel surface and crack between panels:</p> <div> </div> <table> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> <tr> <td>$\leq a$</td> <td>Crack can't enter viewing area</td> <td>$\leq 1/2 t$</td> </tr> <tr> <td>$\leq a$</td> <td>Crack can't exceed the half of SP width.</td> <td>$1/2 t < Z \leq 2 t$</td> </tr> </table> </div>	X	Y	Z	$\leq a$	Crack can't enter viewing area	$\leq 1/2 t$	$\leq a$	Crack can't exceed the half of SP width.	$1/2 t < Z \leq 2 t$	Minor
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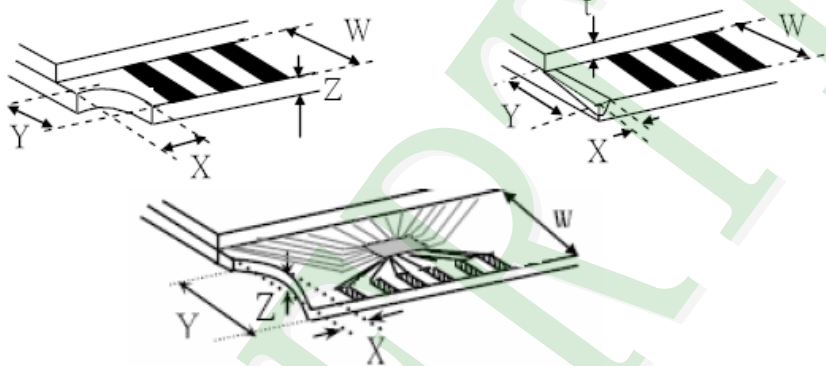
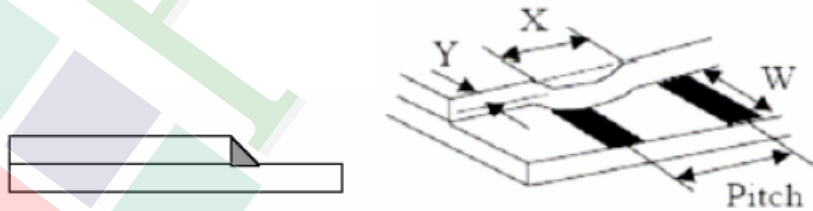
◆ Specification For Monotype and Color STN :

(Ver. B01)

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		X	Y	Z								
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<p>7.2 Protrusion over terminal :</p> <p>7.2.1 Chip on electrode pad :</p>  <table><tr><th></th><th>X</th><th>Y</th><th>Z</th></tr><tr><td>Front</td><td>$\leq a$</td><td>$\leq 1/2 W$</td><td>$\leq t$</td></tr><tr><td>Back</td><td colspan="3">Neglect</td></tr></table>		X	Y	Z	Front	$\leq a$	$\leq 1/2 W$	$\leq t$	Back	Neglect		
	X	Y	Z									
Front	$\leq a$	$\leq 1/2 W$	$\leq t$									
Back	Neglect											

◆ Specification For Monotype and Color STN :

(Ver. B01)

NO	Item	Criterion	Level									
07	The crack of glass	<p>Symbols :</p> <div> <div> <p>X : The length of crack</p> <p>Z : The thickness of crack</p> <p>t : The thickness of glass</p> </div> <div> <p>Y : The width of crack.</p> <p>W : terminal length</p> <p>a : LCD side length</p> </div> </div>	Minor									
		<p>7.2.2 Non-conductive portion :</p>  <table border="1"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>$\leq 1/3 a$</td> <td>$\leq W$</td> <td>$\leq t$</td> </tr> </tbody> </table> <p>☉ If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.</p> <p>7.2.3 Glass remain :</p>  <table border="1"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>$\leq a$</td> <td>$\leq 1/3 W$</td> <td>$\leq t$</td> </tr> </tbody> </table>		X	Y	Z	$\leq 1/3 a$	$\leq W$	$\leq t$	X	Y	Z
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$\leq a$	$\leq 1/3 W$	$\leq t$										

◆ Specification For Monotype and Color STN :

(Ver. B01)

NO	Item	Criterion	Level
08	Backlight elements	8. 1 Backlight can't work normally.	Major
		8. 2 Backlight doesn't light or color is wrong.	Major
		8. 3 Illumination source flickers when lit.	Major
09	General appearance	9. 1 Pin type must match type in specification sheet.	Major
		9. 2 No short circuits in components on PCB or FPC.	Major
		9. 3 Product packaging must the same as specified on packaging specification sheet.	Minor
		9. 4 The folding and peeled off in polarizer are not acceptable.	Minor
		9. 5 The PCB or FPC between B/L assembled distance (PCB or FPC) is ≤ 1.5 mm.	Minor

4. RELIABILITY TEST

4.1 Reliability Test Condition

(Ver.B01)

Reliability Test Condition		(10-201)											
NO.	TEST ITEM	TEST CONDITION											
1	High Temperature Storage Test	Keep in +80 ±2℃ 96 hrs Surrounding temperature, then storage at normal condition 4hrs.											
2	Low Temperature Storage Test	Keep in -30 ±2℃ 96 hrs Surrounding temperature, then storage at normal condition 4hrs.											
3	High Temperature / High Humidity Storage Test	Keep in 60 ℃ / 90% R.H duration for 96 hrs Surrounding temperature, then storage at normal condition 4hrs. (Excluding the polarizer)											
4	Temperature Cycling Storage Test	<div><div><div>-30℃ → +25℃ → +80℃ → +25℃</div><div>(30mins) (5mins) (30mins) (5mins)</div><div>←—————→</div><div>10 Cycle</div></div><div>Surrounding temperature, then storage at normal condition 4hrs.</div></div>											
5	ESD Test	Air Discharge: Apply 2 KV with 5 times Discharge for each polarity +/-	Contact Discharge: Apply 250 V with 5 times discharge for each polarity +/-										
		1. Temperature ambience : 15℃ ~ 35℃ 2. Humidity relative : 30% ~ 60% 3. Energy Storage Capacitance(Cs+Cd) : 150pF±10% 4. Discharge Resistance(Rd) : 330Ω±10% 5. Discharge, mode of operation : Single Discharge (time between successive discharges at least 1 sec) (Tolerance if the output voltage indication : ±5%)											
6	Vibration Test (Packaged)	1. Sine wave 10 ~ 55 Hz frequency (1 min/sweep) 2. The amplitude of vibration : 1.5 mm 3. Each direction (X、Y、Z) duration for 2 Hrs											
7	Drop Test (Packaged)	<table><tr><th>Packing Weight (Kg)</th><th>Drop Height (cm)</th></tr><tr><td>0 ~ 45.4</td><td>122</td></tr><tr><td>45.4 ~ 90.8</td><td>76</td></tr><tr><td>90.8 ~ 454</td><td>61</td></tr><tr><td>Over 454</td><td>46</td></tr></table>		Packing Weight (Kg)	Drop Height (cm)	0 ~ 45.4	122	45.4 ~ 90.8	76	90.8 ~ 454	61	Over 454	46
		Packing Weight (Kg)	Drop Height (cm)										
		0 ~ 45.4	122										
		45.4 ~ 90.8	76										
		90.8 ~ 454	61										
Over 454	46												
Drop Direction :※1 corner / 3 edges / 6 sides each 1time													

5. PRECAUTION RELATING PRODUCT HANDLING

5.1 SAFETY

- 5.1.1 If the LCD panel breaks , be careful not to get the liquid crystal to touch your skin.
- 5.1.2 If the liquid crystal touches your skin or clothes , please wash it off immediately by using soap and water.

5.2 HANDLING

- 5.2.1 Avoid any strong mechanical shock which can break the glass.
- 5.2.2 Avoid static electricity which can damage the CMOS LSI—When working with the module , be sure to ground your body and any electrical equipment you may be using.
- 5.2.3 Do not remove the panel or frame from the module.
- 5.2.4 The polarizing plate of the display is very fragile. So , please handle it very carefully ,do not touch , push or rub the exposed polarizing with anything harder than an HB pencil lead (glass , tweezers , etc.)
- 5.2.5 Do not wipe the polarizing plate with a dry cloth , as it may easily scratch the surface of plate.
- 5.2.6 Do not touch the display area with bare hands , this will stain the display area.
- 5.2.7 Do not use ketonics solvent & aromatic solvent. Use with a soft cloth soaked with a cleaning naphtha solvent.
- 5.2.8 To control temperature and time of soldering is $320 \pm 10^{\circ}\text{C}$ and 3-5 sec.
- 5.2.9 To avoid liquid (include organic solvent) stained on LCM .

5.3 STORAGE

- 5.3.1 Store the panel or module in a dark place where the temperature is $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ and the humidity is below 65% RH.
- 5.3.2 Do not place the module near organics solvents or corrosive gases.
- 5.3.3 Do not crush , shake , or jolt the module.

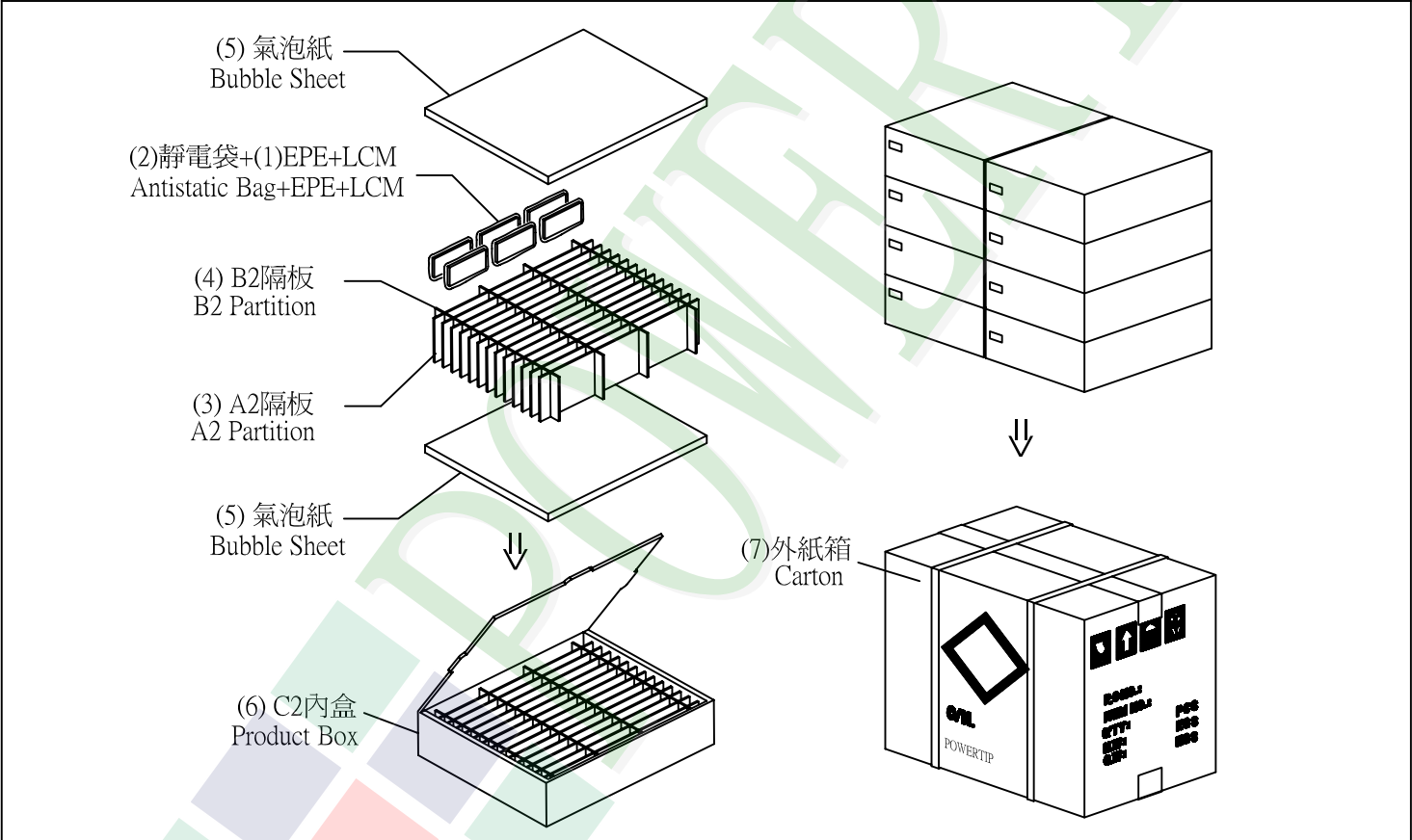
5.4 TERMS OF WARRANTY

- 5.4.1 Applicable warrant period
The period is within thirteen months since the date of shipping out under normal using and storage conditions.
- 5.4.2 Unaccepted responsibility
This product has been manufactured to your company's specification as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment , we cannot take responsibility if the product is used in nuclear power control equipment , aerospace equipment , fire and security systems or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required

[illegible]

Ver.001		<div>LCM包裝規格書</div> <div>LCM Packaging Specifications</div>	Approve	Check	Contact
Documents NO.	JPKG-PE1602WRT-017-L-Q		Ryan	Terry	Air

1.包裝材料規格表 (Packaging Material) : (per carton)						
No.	Item	Model	Dimensions (mm)	1Pcs Weight	Quantity	Total Weight
1	成品 (LCM)	PE1602WRT-017-L-Q	70 X 32 X 14	0.017	240	4.08
2	粉紅色防靜電EPE泡棉(1)	OTFOAM00023ABA	70 X 50 X 10	0.0009	240	0.216
3	靜電袋(2)Antistatic Bag	BAG100100ARABA	100 X 100	0.0011	240	0.264
4	A2隔板(3)A2 Partition	BX29300070BMBA	293 X 70 X 2.5	0.009	88	0.792
5	B2隔板(4)B2 Partition	BX24500070BLBA	245 X 70 X 2.5	0.0118	32	0.3776
6	氣泡紙(5)Bubble Bag	BAG280240BWABA	280 X 240	0.006	16	0.096
7	C2內盒(6)Product Box	BX31025580AABA	310 X 255 X 80	0.16	8	1.28
8	外紙箱(7)Carton	BX52732536CCBA	527 X 325 X 360	0.83	1	0.83
9						
2.一 整箱總重量 (Total LCD Weight in carton) : 7.94 Kg±10% 取小數2位						
3.單箱數量規格表 (Packaging Specifications and Quantity) :						
(1)Quantity Of Spacer : A2-1隔板 X 11 , B2-2隔板 X 4						
(2)Total LCM quantity in carton : quantity per box 30 x no of boxes 8 = 240						



特 記 事 項 (REMARK)		
4. Label Specifications : 標籤依廠內標準作業	5. LCM排放示意圖(前後間隔不放置): 5. LCM placed as figure showing: (First and last slot should be empty)   模組(LCM) X 1pcs.	6.模組的A,K需插入EPE泡棉內, 模組的PIN需緊靠EPE泡棉的邊緣.