

	SPECIFICATIONS	
CUSTOMER	- CNO003	
SAMPLE CODE	SE240128W	RF-002-KQ
MASS PRODUCTION CODE	PE240128W	RF-002-KQ
SAMPLE VERSION	. 05	
SPECIFICATIONS EDITION	. 011	
DRAWING NO. (Ver.)	: HLMD-PE2	40128WRF-002-KQ_003
PACKAGING NO. (Ver.)	: HPKG-PE2	40128WRF-002-KQ_001
		Date:
Approved	Checked	(
Approved	<b>Checked</b> 張久慧	Date: 2012.07.17
	張久慧 for design input	Date: Designer



# **RECORDS OF REVISION**

Ver.	Edi.	Description	Page	Design by
01	001	New Drawing	-	張恒
01	002	It has changed the content of Drawing	-	張恒
01	003	It has changed the Type of FPC	-	張恒
01	004	It has changed the length of FPC	-	張恒
01	005	New Sample	-	魏永超
02	006	Low temperature display improvement, include B/L & LCD	-	Wesley
02	007	Add Pull Tape	LCM Drawing	Wesley
03	008	Add Silicone	-	Wesley
04	009	Add tape on B/L Remove the Silicone of the sample Ver.03	LCM Drawing	Wesley
05	010	Change the supplier of FPC	-	汪秀俊
05	011	Add EEPROM Read Operation Instruction	21	劉進
	X			
X				
	01 01 01 01 01 02 02 02 02 03 04 05	01       001         01       002         01       003         01       003         01       004         01       005         02       006         02       007         03       008         04       009         05       010	Image: Constraint of the sample ver.0301001002It has changed the content of Drawing01002It has changed the Type of FPC01003It has changed the length of FPC01004It has changed the length of FPC01005New Sample02006Low temperature display improvement, include B/L & LCD02007Add Pull Tape03008Add Silicone04009Add tape on B/L Remove the Silicone of the sample Ver.0305010Change the supplier of FPC	11101001New Drawing-01002It has changed the content of Drawing-01003It has changed the Type of FPC-01004It has changed the length of FPC-01005New Sample-02006Low temperature display improvement, include B/L & LCD-02007Add Pull TapeLCM Drawing03008Add Silicone-04009Add tape on B/L Remove the Silicone of the sample Ver.03Drawing05010Change the supplier of FPC-



# Contents

# **1. SPECIFICATIONS**

- **1.1 Features**
- **1.2 Mechanical Specifications**
- **1.3** Absolute Maximum Ratings
- **1.4 DC Electrical Characteristics**
- **1.5 Optical Characteristics**
- **1.6 Backlight Characteristics**
- **2. MODULE STRUCTURE** 
  - 2.1 Counter Drawing
  - 2.2 Interface Pin Description
  - **2.3** Timing Characteristics
  - 2.4 Power supply circuit
  - 2.5 EEPROM Read Operation Instruction

# **3. QUALITY ASSURANCE SYSTEM**

- 3.1 Quality Assurance Flow Chart
- **3.2** Inspection Specification

# 4. RELIABILITY TEST

4.1 Reliability Test Condition

# **5. PRECAUTION RELATING PRODUCT HANDLING**

- 5.1 Safety
- 5.2 Handling
- 5.3 Storage
- 5.4 Terms of Warranty

## Appendix: 1. LCM Drawing 2. Packing Specification



### **1. SPECIFICATIONS**

#### **1.1 Features**

Item	Standard Value
Display Type	240*128 Dots
LCD Type	FSTN,Positive,White,Transflective, Extended Temp.
Driver Condition	LCD Module :1/160Duty,1/14Bias
Viewing Direction	12 O'clock
Backlight	White LED Backlight
Weight	41g
Interface	Support 8 Bit Parallel interface with 8080 or 6800 series MPU
Other(controller / driver IC)	SITRONIX - ST7529-G
	THIS PRODUCT CONFORMS THE ROHS OF PTC
ROHS	Detail information please refer web side :
	http://www.powertip.com.tw/news/LatestNews.asp

# 1.2 Mechanical Specifications

Item	Standard Value	Unit
Outline Dimension	74.5(L)*54.5 (W)*9.8 (H)(max)	mm
Viewing Area	68.0(L)* 40.0(W)	mm
Active Area	61.18(L)* 36.46(W)	mm
Dot Size	0.235(W)*0.265 (L)	mm
Dot Pitch	0.255(W)*0.285 (L)	mm

Note : For detailed information please refer to LCM drawing

### **1.3 Absolute Maximum Ratings**

Item	Symbol	Condition	Min.	Max.	Unit
Power Supply Voltage	V <sub>DD</sub>	_	-0.5	4.0	V
LCD Driver Supply Voltage	V <sub>LCD</sub>	_	-0.5	20.0	V
Input Voltage	V <sub>IN</sub>	_	-0.5	V <sub>DD</sub> +0.5	V
Operating Temperature	T <sub>OP</sub>	_	-30	80	°C
Storage Temperature	$T_{ST}$	_	-35	80	°C
Storage Humidity	$H_{D}$	Ta < 60 °C	-	90	%RH



# **1.4 DC Electrical Characteristics**

		VI	$DD = 3.0 \pm 0.0$	3V,Vss=	=0V,Ta = 2	25℃	
Item	Symbol	Condition	Min.	Тур.	Max.	Unit	
Logic Supply Voltage	V <sub>DD</sub>	$Ta = 25^{\circ}C$	2.7	3.0	3.3	V	
"H" Input Voltage	V <sub>IH</sub>	$Ta = 25^{\circ}C$	0.7Vdd	-	Vdd	V	
"L" Input Voltage	V <sub>IL</sub>	$Ta = 25^{\circ}C$	Vss	-	0.3 Vdd	V	
High-level Output Current	I <sub>OH</sub>	VDD=2.7V VOH=2.2V	0.5	-	-	mA	
Low-level Output Current	I <sub>OL</sub>	VDD=2.7V VOL=0.5V	-	-	-0.5	mA	
Supply Current	I	VDD=3.0V;VOP=14V; Pattern= Full display	-	0.13	-	mA	
Supply Current	I <sub>DD</sub>	Vdd=3.0V;Vop= 14V Pattern= Horizontal line*1		0.15	1.5	ША	
	V <sub>OP</sub>	-30°C	14.9	15.1	15.3		
LCM Driver Voltage		25°C	13.8	14	14.2	V	
	*2	80°C	13.5	13.7	13.9		

NOTE: \*1 The Maximum current display

\*2 The VOP test point is  $V_0$ - $V_{SS}$ .



## **1.5 Optical Characteristics**

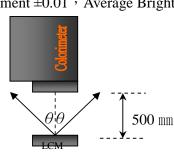
			LCD P	anel $: 1/16$	$50$ Duty $\cdot 1/$	$14Bias \cdot V$	$I_{\text{LCD}} = 14$	V · Ta = 25°
Item		Symbol	Conditions	Min.	Тур.	Max.	Unit	Reference
Response Time	Rise	tr		-	130	195	ma	Note2
Response Time	Fall	tf		-	290	435	ms	Note2
	Тор	$\Theta Y+$	C <u>&gt;</u> 2.0,	-	40	-		
Viewing angle	Bottom	ΘY-	Ø =90°	-	40	-	Dec	Notes 1
range	Left	ΘX-		-	40	-	Deg.	Notes 1
	Right	ΘX+		-	40	-		
Contrast Rat	io	С	$\theta = 0^{\circ},$ $\varnothing = 90^{\circ}$	-	3	-	-	Note 3
Average Bright (with LCD)		IV		125		-	cd/m <sup>2</sup>	
CIE Color Coor	dinate	Х		0.25	0.30	0.35		Note 4
(With LCD)	*1	Y		0.27	0.32	0.37		
Uniformity <sup>3</sup>	*2	∆B		70	-	-	%	

1/1 (0)

Note 4 :

- 1 : △B=B(min) / B(max) \* 100%
- 2: Measurement Condition for Optical Characteristics:
  - a : Environment: 25°C±5°C / 60±20%R.H , no wind , dark room below 10 Lux at typical lamp current and typical operating frequency.
  - b : Measurement Distance:  $500 \pm 50 \text{ mm} \rightarrow (\theta = 0^{\circ})$
  - c : Equipment: TOPCON BM-7 fast , (field  $1^{\circ}$ ), after 10 minutes operation.
  - d : The uncertainty of the C.I.E coordinate measurement  $\pm 0.01$  , Average Brightness  $\pm 4\%$

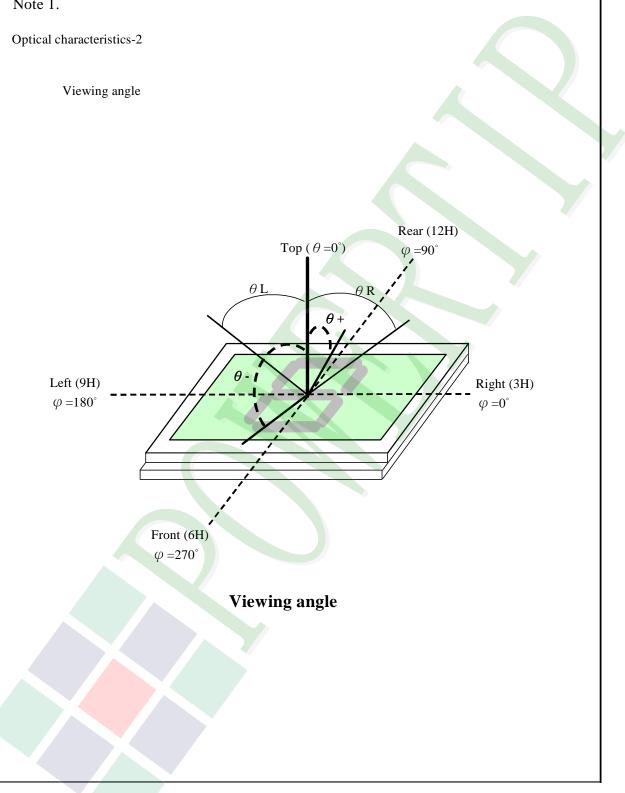




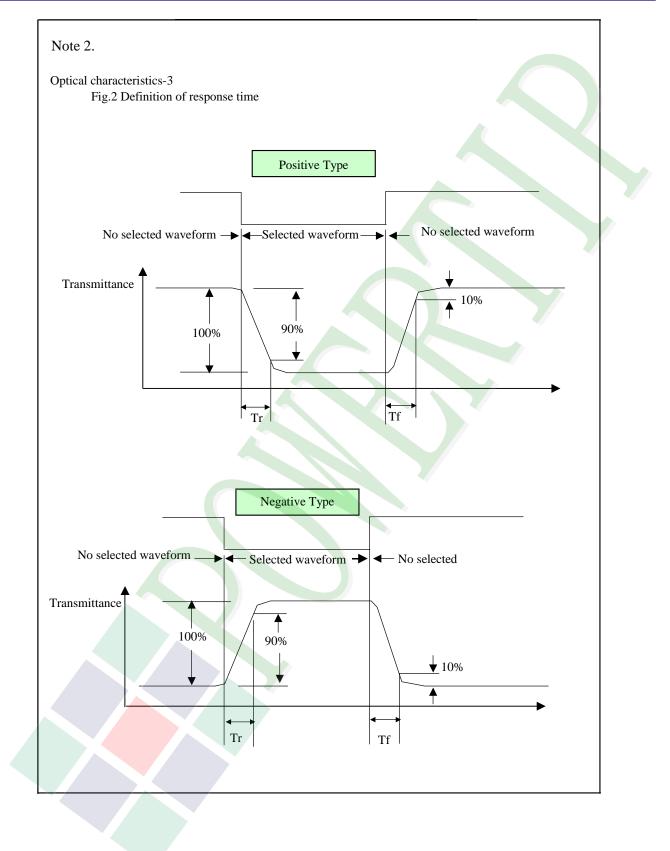
Colorimeter=BM-7 fast

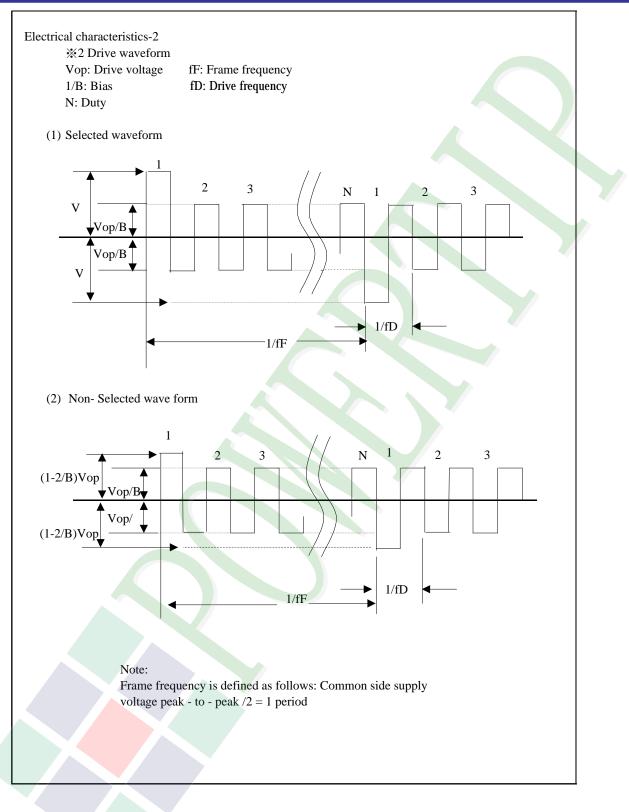




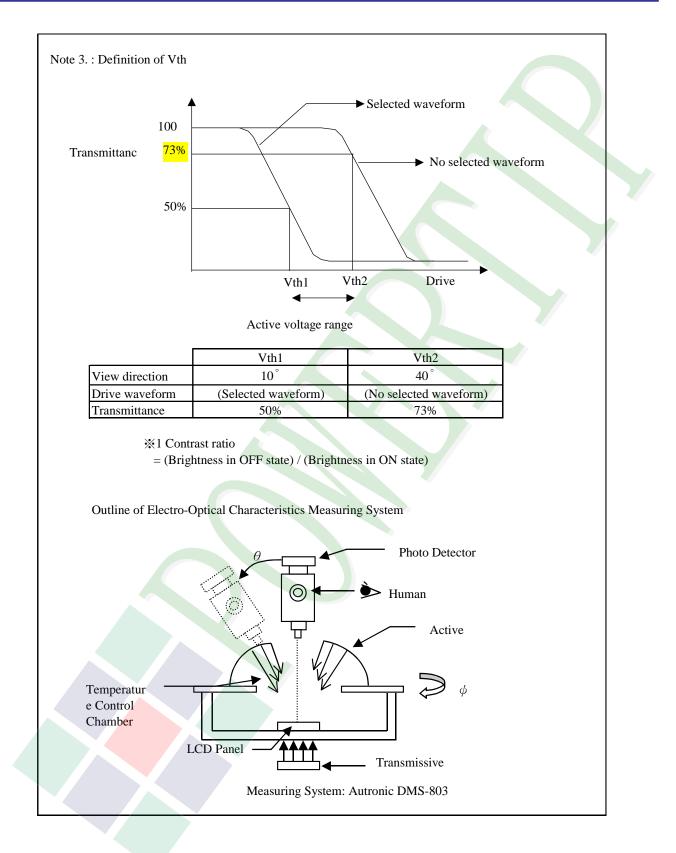














# **1.6 Backlight Characteristics**

LCD Module with LED Backlight

Maximum Ratings

0					
Item	Symbol	Conditions	Min.	Max.	Unit
Forward Current	IF	Ta =25°C	-	90	mA
Reverse Voltage	VR	Ta =25°℃	-	5	V
Power Dissipation	PD	Ta =25°C	Ē	420	mW

#### Electrical / Optical Characteristics

Electrical / optical characteri						
Item	Symbol	Conditions	Min.	Тур.	Max.	Unit
Forward Voltage	VF	IF= 90mA	2.3	3.3	3.5	V
Average Brightness (without LCD)	IV	IF= 90mA	800		-	cd/m <sup>2</sup>
CIE Color Coordinate	Х	IF= 90mA	0.24	0.27	0.30	
(Without LCD)	Y	II'- 90111A	0.25	0.28	0.31	-
Color			White			

PE240128WRF-002-KQ



# **2. MODULE STRUCTURE** 2.1 Counter Drawing 2.1.1 LCM mechanical diagram \*See appendix 2.1.2 Block diagram A٠ LED Backlight K٠ COMO 240\*128 DOTS сойба LCD PANEL COM64 COM127 SEGO . . . . . . . . . . SEG239 SEG239 SEGO COM63 COM80 ST7529 COMO COM143



# 2.2 Interface Pin Description

Pin No.	Symbol	Function						
		Register select input pin						
1	A0	– A0 = "H": C	00 to D8 or SI	are display data				
		– A0 = "L": D	0 to D8 or SI	are control data				
		Read / Write e	Read / Write execution control pin					
		MPU Type	RW_WR	Description				
		6800	RW	Read / Write control input pin				
				RW = "H" : read				
2	RW_WR			RW = "L" : write				
		8080	/WR	Write enable clock input pin	-			
				The data on DB0 to DB8 are latched at the				
				rising edge of the /WR signal.				
3	D0				1			
4	D1							
5	D2	_						
6	D3	They connec	t to the stand	ard 8-bit MPU bus via the 8 bit bi-directional bus	s. Wher			
		the following interface is selected and the XCS pin is high, the following pins						
		the following	interface is se	elected and the XCS pin is high, the following p	ins			
7	D4	•		elected and the XCS pin is high, the following p which should be fixed to VDD or VSS.	ins			
		•			ins			
7	D4	•			ins			
7 8	D4 D5	•			ins			
7 8 9	D4 D5 D6	become high		which should be fixed to VDD or VSS.	ins			
7 8 9	D4 D5 D6	become high	impedance, v	which should be fixed to VDD or VSS.	ins			
7 8 9	D4 D5 D6	become high	impedance, v	which should be fixed to VDD or VSS.	ins			
7 8 9	D4 D5 D6	become high Read / Write e	execution contr RW_WR	which should be fixed to VDD or VSS.	ins 			
7 8 9 10	D4 D5 D6 D7	become high Read / Write e	execution contr RW_WR	which should be fixed to VDD or VSS.  ol pin  Description  Read / Write control input pin	ins			
7 8 9	D4 D5 D6	become high Read / Write e	execution contr RW_WR	which should be fixed to VDD or VSS.          ol pin         Description         Read / Write control input pin         -RW = "H": When E is "H", D0 to D8 are in				
7 8 9 10	D4 D5 D6 D7	become high Read / Write e	execution contr RW_WR	which should be fixed to VDD or VSS. ol pin Description Read / Write control input pin -RW = "H": When E is "H", D0 to D8 are in an output status.				
7 8 9 10	D4 D5 D6 D7	become high Read / Write e	execution contr RW_WR	which should be fixed to VDD or VSS. ol pin Description Read / Write control input pin -RW = "H": When E is "H", D0 to D8 are in an output status. -RW = "L": The data on D0 to D8 are latched at				
7 8 9 10	D4 D5 D6 D7	become high Read / Write e MPU Type 6800	execution contr RW_WR E	which should be fixed to VDD or VSS. ol pin Description Read / Write control input pin -RW = "H": When E is "H", D0 to D8 are in an output status. -RW = "L": The data on D0 to D8 are latched at the falling edge of the E signal.				
7 8 9 10	D4 D5 D6 D7	become high Read / Write e MPU Type 6800	execution contr RW_WR E	which should be fixed to VDD or VSS. ol pin Description Read / Write control input pin -RW = "H": When E is "H", D0 to D8 are in an output status. -RW = "L": The data on D0 to D8 are latched at the falling edge of the E signal. Read enable clock input pin				
7 8 9 10	D4 D5 D6 D7	become high Read / Write e MPU Type 6800 8080	execution contr RW_WR E /RD	which should be fixed to VDD or VSS. ol pin Description Read / Write control input pin -RW = "H": When E is "H", D0 to D8 are in an output status. -RW = "L": The data on D0 to D8 are latched at the falling edge of the E signal. Read enable clock input pin When /RD is "L", D0 to D8 are in an output				

Pin No.	Symbol			Function
13	IF1	IF1	IF3	MPU interface type
14	IF3	L H	H	80 series 8-bit parallel     68 series 8-bit parallel
15	XCS		n I/O is enabl	ed only when XCS is "L". When chip select is a high impedance.
16	VSS	Power supply (	VSS=0)	
17	VDD	Power supply (	VDD=3.0V)	
18	C7P	DC / DC voltage the $\leq$ 7X VLCI	-	Connect a capacitor between this terminal and rminal.
19	C1N	-		Connect a capacitor between this terminal and C5P; $\geq$ 8X also C7P terminal.
20	C5P	DC / DC voltagethe $\leq$ 5X VLCI		Connect a capacitor between this terminal and terminal.
21	C3P	DC / DC voltagethe $\leq 3X$ VLCI		Connect a capacitor between this terminal and 1 terminal.
22	C1N1		je converter.	Connect a capacitor between this terminal and
23	C1P	DC / DC voltag		Connect a capacitor between this terminal and
24	C2P	DC / DC voltag the 2X VLCD;		Connect a capacitor between this terminal and rminal.
25	C2N	DC / DC voltagethe $\leq 2X VLCI$		Connect a capacitor between this terminal and terminal.
26	C4P	DC / DC voltagethe $\leq 4X VLCI$		Connect a capacitor between this terminal and terminal.
27	C2N1		je converter.	Connect a capacitor between this terminal and
28	С6Р		je converter.	Connect a capacitor between this terminal and
29	VLCDIN	An external LC this case, VLC	D supply volt DOUT has to	age can be supplied using the VLCDIN pad. In be left open, and the internal voltage generator ero. (SET register V B=0)



Pin No.	Symbol	Function
30	VLCDOUT	If the internal voltage generator is used, the V LCDIN & VLCDOUT must be connected together. If an external supply is used, this pin must be left open.
31	V4	LCD driver supply voltages
32	V3	V0In & V0out should be connected together in FPC area. Voltages should have the following relationship:
33	V2	$V0 \ge V1 \ge V2 \ge V3 \ge V4 \ge VSS$ When the internal power circuit is active, these voltages are generated as the following table according to the state of LCD bias.
34	V1	LCD Bias         V1         V2         V3         V4           1/N Bias         (N-1) / N x V0 (N-2) / N x V0 (2/N) x V0         (1/N) x V0
35	VOOUT	NOTE: N = 5 to 14
36	VOIN	
37	А	
38	A	Power supply for LED backlight Anode input
39	K	Power supply for LED backlight Cathnode input
40	K	



# 2.3 Timing Characteristics

# L A0 -taws tans XCS tcycs tcclR,tcclw WR, RD tcchr, tcchw**t**DH8 tosa D0 to D7 (Write) tACCS tons D0 to D7 (Read)

### System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

 $(VDD = 3.3V, Ta = 25^{\circ}C)$ 

				(	VDD = 5.5 V	, 14 20	
Item	Signal	Symbol	Condition	Rat	ting	Units	
nem	Signal	Symbol	Condition	Min.	Max.	Units	
Address hold time		tAH8		20			
Address setup time	A0	tAW8		20	—		
System cycle time		tCYC8		200	_		
Enable L pulse width (WRITE)	WR	tCCLW		100	—		
Enable H pulse width (WRITE)	W K	tCCHW		100			
Enable L pulse width (READ)	RD	tCCLR		100		ns	
Enable H pulse width (READ)	KD	tCCHR		100			
WRITE Data setup time		tDS8		150			
WRITE Address hold time	D0 to D7	tDH8		20			
READ access time	D0 10 D7	tACC8	CL = 100  pF		40		
READ Output disable time		tOH8	CL = 100  pF		30		



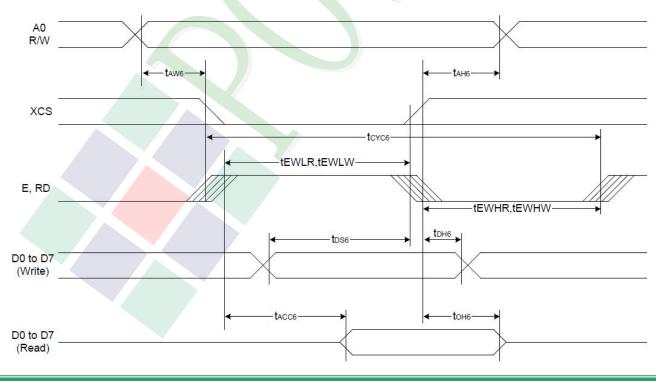
 $<sup>(</sup>VDD = 2.7V, Ta = 25^{\circ}C)$ 

lterre	Cimral	Complexed	Condition	Rati	1		
ltem	Signal Symbol		Condition	Min.	Max.	Units	
Address hold time		tAH8	-	20	-		
Address setup time	A0	tAW8	-	30	-	1	
System cycle time		tCYC8	_	250	-		
Enable L pulse width (WRITE)	WD	tCCLW	-	150	-		
Enable H pulse width (WRITE)	WR	tCCHW	-	100			
Enable L pulse width (READ)	RD	tCCLR	-	150	-	ns	
Enable H pulse width (READ)	KD	tCCHR	-	100	-	]	
WRITE Data setup time		tDS8	-	200	-	]	
WRITE Address hold time	D0 to D7	tDH8	-	20	-	]	
READ access time	D0 to D7	tACC8	CL = 100 pF	-	40		
READ Output disable time	1	tOH8	CL = 100 pF		30	]	

\*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf)  $\leq$  (tCYC8 - tCCLW - tCCHW) for (tr + tf)  $\leq$  (tCYC8 - tCCLR - tCCHR) are specified.

\*2 All timing is specified using 20% and 80% of VDD as the reference.

\*3 tCCLW and tCCLR are specified as the overlap between XCS being "L" and WR and RD being at the "L" level.



## I System Bus Read/Write Characteristics 1 (For the 6800 Series MPU)



 $(VDD = 3.3V, Ta = 25^{\circ}C)$ 

Item	Signal	Symbol	Condition	Rat	ing	Units
пеш	Signal	Symbol	Condition	Min.	Max.	Onits
Address hold time		tAH6		20	—	
Address setup time	A0	tAW6		20		
System cycle time		tCYC6		200	_	
Enable L pulse width (WRITE)	WR	tCCLW		100	_	
Enable H pulse width (WRITE)	W K	tCCHW		100		
Enable L pulse width (READ)	RD	tCCLR		100	—	ns
Enable H pulse width (READ)	KD	tCCHR		100	_	
WRITE Data setup time		tDS6		150	_	
WRITE Address hold time	D0 to D7	tDH6		20	—	
READ access time	D0 10 D7	tACC6	CL = 100 pF		40	
READ Output disable time		tOH6	CL = 100  pF		30	

(VDD = 2.7V, Ta = 25°C)

l <b>4</b>	Cirrus	Cumulant	Condition	Rati	ng	Unite
ltem	Signal	Symbol	Condition	Min.	Max.	Units
Address hold time	AO	tAH6	-	20	-	
Address setup time	AU	tAW6	-	30	-	
System cycle time		tCYC6	-	250	-	
Enable L pulse width (WRITE)	E	tEWLW	-	150	-	
Enable H pulse width (WRITE)		tEWHW	-	100	-	
Enable L pulse width (READ)	RD	tEWLR	-	150	-	ns
Enable H pulse width (READ)	RD	tEWHR	-	100	-	
WRITE Data setup time		tDS6	-	200	-	
WRITE Address hold time	D0 to D7	tDH6	-	20	-	]
READ access time	001007	tACC6	CL = 100 pF	-	40	]
READ Output disable time		tOH6	CL = 100 pF	-	30	

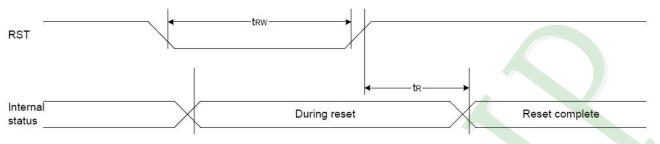
\*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast,  $(tr + tf) \leq (tCYC6 - tEWLW - tEWHW)$  for  $(tr + tf) \leq (tCYC6 - tEWLR - tEWHR)$  are specified.

\*2 All timing is specified using 20% and 80% of VDD as the reference.

\*3 tEWLW and tEWLR are specified as the overlap between XCS being "L" and E.



### I Reset Timing



 $(VDD = 3.3V, Ta = -20 \text{ to } 70^{\circ}C)$ 

Item	Signal	Symbol	Condition		Rating		Units
Item	Signai	Symbol	Condition	Min.	Тур.	Max.	Units
Reset time		tR			_	1.0	us
Reset "L" pulse width	/RES	tRW		1.0	—		us

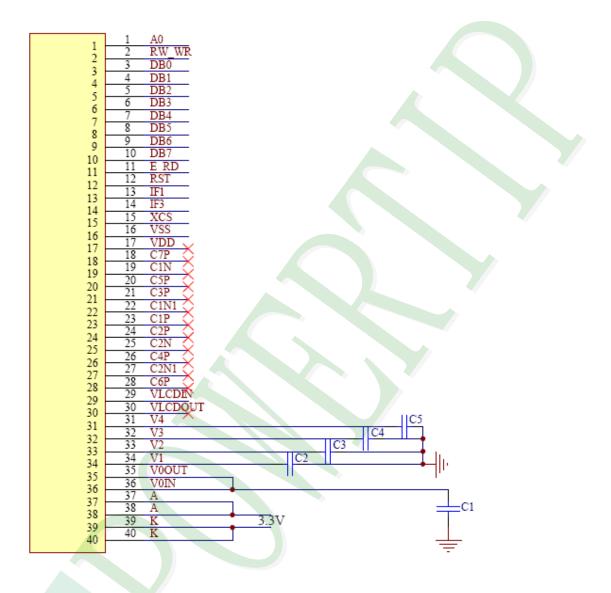
 $(VDD = 2.7V, Ta = -20 \text{ to } 70^{\circ}C)$ 

ltem	Signal	Symbol	Condition		Rating		Units
nem	Signai	Symbol	Condition	Min.	Тур.	Max.	Units
Reset time		tR	-	-	-	1.5	us
Reset "L" pulse width	RST	tRW		1.5	-	-	us

Note : For detailed information please refer to IC datasheet : ST7529 Ver 2.1a.



## 2.4 Power supply circuit



Note: The regulating capacitance on V0 ~ V4 should be between 1.0 to 2.2  $\mu$  F.

## 2.5 EEPROM Read Operation Instruction

Read EEPROM after reset must be done when using ST7529. If ST7529 did not read EEPROM for VOP calibration, that will cause VOP variation and affect the display quality. The following instruction is a example for EEPROM read operation.

```
void ReadEEPROM( void )
{
Write( COMMAND, 0x0030 ); // Ext = 0
Write( COMMAND, 0x0007 ); // Initial code (1)
Write( DATA, 0x0019 );
Write( DATA, 0x0019 ); // Ext = 1
Write( COMMAND, 0x0031 ); // Ext = 1
Write( COMMAND, 0x00CD ); // EEPROM ON
Write( DATA, 0x0000 ); // Entry "Read Mode"
Delay( 100ms ); // Waite for EEPROM Operation ( 100ms )
Write( COMMAND, 0x00FD ); // Start EEPROM Reading Operation
Delay( 100ms ); // Waite for EEPROM Operation ( 100ms )
Write( COMMAND, 0x00CC ); // Exist EEPORM Mode
Write( COMMAND, 0x0030 ); // Ext = 0
}
```

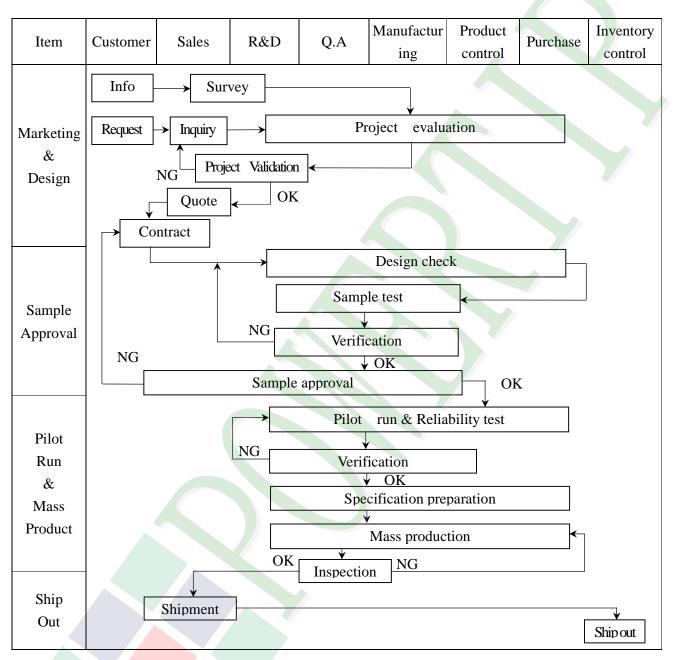
# Note :

1. The EEPROM must be read in the initial flow for calibration.

2. When "Reading" value from EEPROM, the voltage of VLCDIN (PIN29) must be more than 6V. For detailed information please refer to 8.2.1 EEPROM Setting Flow on page 52 of the ST7529 datasheet Ver 2.1a.

# 3. QUALITY ASSURANCE SYSTEM

## 3.1 Quality Assurance Flow Chart





Item	Customer	Sales	R&D	Q.A	Manufactu ring	Product control	Purchase	Inventory control
Sales Service	Info	➤ Claim	[	Trackin	Failure an Corrective			
Q.A Activity	1. ISO 9001 3. Equipmer 5. Standardi	nt calibratio	n		ocess improv Education An			

#### **Inspection Specification** 3.2

Scope : The document shall be applied to LCD Module for Monotype and Color STN(Ver. B01).

◆Inspection Standard : MIL-STD-105E Table Normal Inspection Single Sampling Level Ⅱ.

◆Equipment : Gauge 、 MIL-STD 、 Powertip Tester 、 Sample

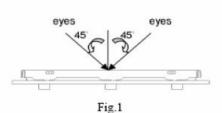
◆Defect Level: Major Defect AQL:0.4 ; Minor Defect:AQL: 1.5.

♦OUT Going Defect Level : Sampling .

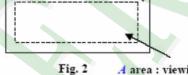
### Manner of appearance test :

Specification:

- (1). The test be under 20W×2 fluorescent light ' and distance of view must be at 30 cm.
- (2). Standard of inspection : (Unit : mm)
- (3). The test direction is base on about around 45° of vertical line. (Fig. 1)
- (4). Definition of area . (Fig. 2)



**B** area : Outside of viewing area



A area : viewing area

NO	Item	Criterion	Level
		1. 1 The part number is inconsistent with work order of Production.	Major
01	Product condition	1. 2 Mixed production types.	Major
		1.3 Assembled in inverse direction.	Major
02	Quantity	2. 1 The quantity is inconsistent with work order of production.	Major
03	Outline dimension	3.1 Product dimension and structure must conform to Structure diagram.	Major
		4. 1 Missing line character and icon.	Major
		4. 2 No function or no display.	Major
04	Electrical Testing	4, 3 Output data is error.	Major
		4. 4 LCD viewing angle defect.	Major
		4.5 Current consumption exceeds product specifications.	Major

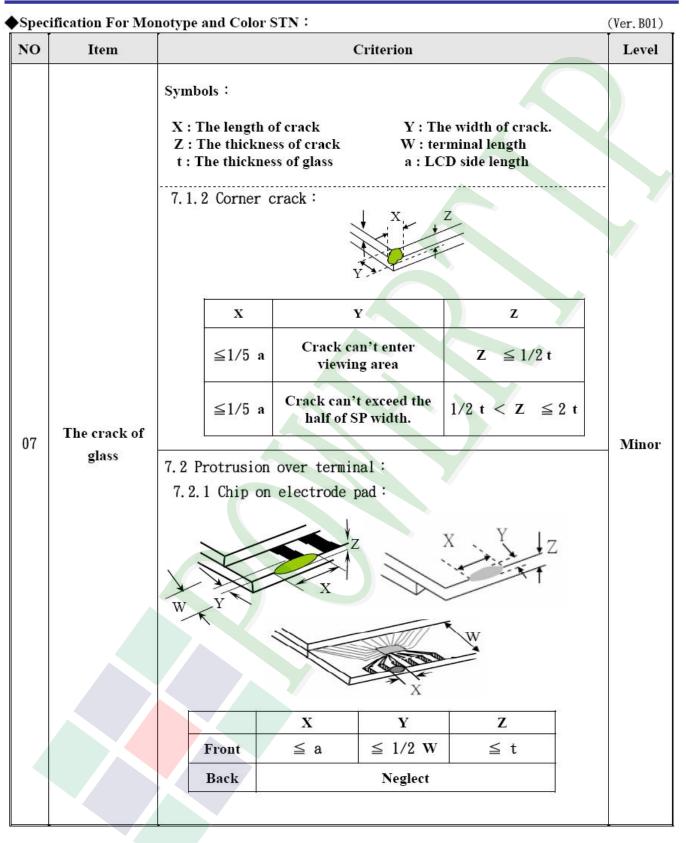


◆Spe	cification For Mono	type and Color STN :				(Ver.B01)		
NO	Item	Criterion						
	Black or white dot 、scratch 、 contamination	4 white or black spots pr	<ul> <li>5. 1. 1 display only :</li> <li>• White and black spots on display ≤ 0. 30 mm, no more than 4 white or black spots present.</li> <li>• Densely spaced : NO more than two spots or lines within 3 mm.</li> </ul>					
		Dimension		Acceptance	(O'ty)			
	Round type	(diameter : $\Phi$ )		A area	B area			
	- <b>&gt;</b>  ,,   <b>4</b> -,	$\Phi \leq 0.10$	Acce	ept no dense				
05	• <u>x</u> <u>v</u>	$0.10 < \Phi \leq 0.20$						
05		$0.20 < \Phi \leq 0.30$		2	Ignore	Minor		
	Φ=(x+y)/2	Total quantity		4				
		5. 1. 3 Line type: Dimension Acceptance (Q'ty)		otance (Q'ty)				
	Line type	Length (L) Width (W) A area		B area				
		$$ $W \le 0$ $L \le 3.0$ $0.03 < W \le 0$ $L \le 2.5$ $0.05 < W \le 0$	0. 05	Accept no de	nse Ignore			
		W >0	). 075 As round type		round type			
						_		
		Dimension		Acceptan	ce (Q'ty)			
		(diameter : $\Phi$ )		A area	B area	$\left  \right $		
		$\Phi \leq 0.20$	Ac	cept no dense	_			
06	Polarizer Bubble	$0.20 < \Phi \le 0.50$		3		Minor		
	Lubble	$0.50 < \Phi \le 1.00$		2	Ignore			
		$\Phi > 1.00$			_			
		Total quantity	4					

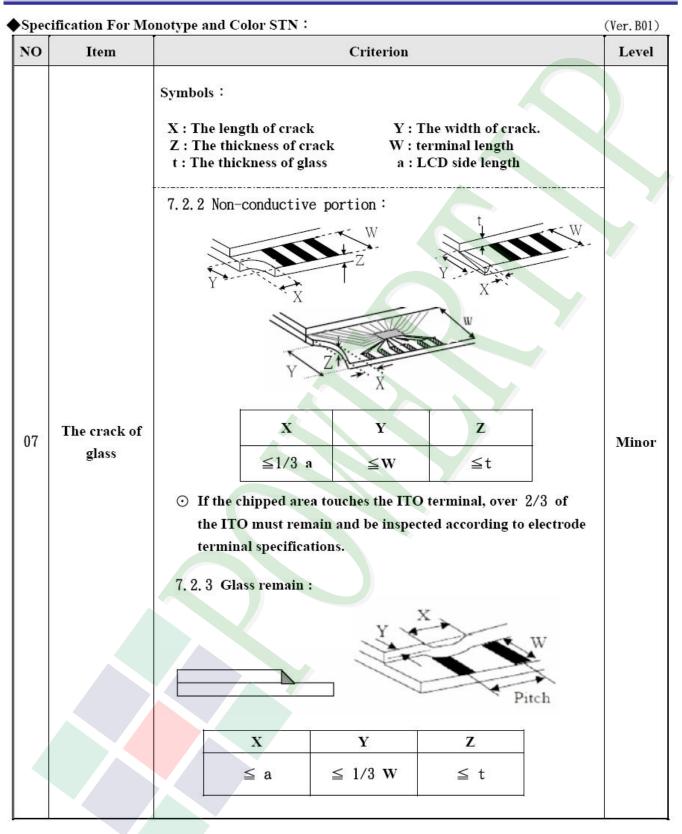


♦Speci	fication For Mono	type and Color STN :		(Ver.B01)
NO	Item	Criterio	n	Level
		Z : The thickness of crack W	Y : The width of crack. V : terminal length 1 : LCD side length	
		7.1 General glass chip : 7.1.1 Chip on panel surface and crac	ck between panels:	
		Y Z Z	Y	
07	The crack of glass	SP	SP [NG]	Minor
		[OK] Seal width	Y	
			Z	
		≤ a Crack can't enter viewing area	≦1/2 t	
		≤ a Crack can't exceed th half of SP width.	$\frac{1}{2} t < \mathbf{Z} \leq t$	











Speci	ification For Mo	notype and Color STN :	(Ver.B01)
NO	Item	Criterion	Level
		8. 1 Backlight can't work normally.	Major
08	Backlight elements	8. 2 Backlight doesn't light or color is wrong.	Major
		8. 3 Illumination source flickers when lit.	Major
		9. 1 Pin type must match type in specification sheet.	Major
		9. 2 No short circuits in components on PCB or FPC.	Major
09	General appearance	9. 3 Product packaging must the same as specified on packaging specification sheet.	Minor
		9. 4 The folding and peeled off in polarizer are not acceptable.	Minor
		9.5 The PCB or FPC between B/L assembled distance (PCB or FPC) is $\leq 1.5$ mm.	Minor



# 4. RELIABILITY TEST

## 4.1 Reliability Test Condition

NO.	TEST ITEM		TEST CO	ONDITION					
4	High Temperature	Keep in +80	) ±2℃ 96 hrs						
1	Storage Test	Surroundin	g temperature, then st	orage at normal conditio	n 4hrs.				
2	Low Temperature	Keep in -35	± <b>2°</b> ℃ 96 hrs						
2	Storage Test	Surrounding	g temperature, then st	orage at normal conditio	n 4hrs.				
	High Temperature /	-	°C / 90% R.H duration						
3	High Humidity			orage at normal conditio	on <b>4</b> hrs.				
	Storage Test	(Excluding	(Excluding the polarizer)						
			• •	°C → 80 → +25°C					
4	<b>Temperature Cycling</b>		( <b>30</b> mins) ( <b>5</b> mins)	(30mins) (5mins)					
-	Storage Test		10 (	Cycle					
		Surroundin	g temperature, then ste	orage at normal conditio	on <b>4</b> hrs.				
		Air Discharge: Contact Discharge:							
		Apply 2 KV	with <b>5</b> times	Apply 250 V with 5 tin	nes				
		U	or each polarity +/-	discharge for each pola	rity +/-				
	ESD Test	1. Temperature ambiance : 15°C ~ 35°C							
5		2. Humidity relative : $30\% \sim 60\%$							
•		3. Energy Storage Capacitance(Cs+Cd) : 150pF±10%							
		4. Discharge Resistance(Rd) : <b>330</b> Ω± <b>10%</b>							
		5. Discharge, mode of operation : Single Discharge (time between successive discharges at least 1 sec)							
				6	least 1 sec)				
			f the output voltage in						
-	Vibration Test		ve 10~55 Hz frequenc						
6	(Packaged)	-	blitude of vibration :1.						
		3. Each di	rection $(X \cdot Y \cdot Z)$ due	ration for <b>2</b> Hrs					
			Packing Weight (Kg	) Drop Height (cm)					
			0 ~ 45.4	122					
-	Drop Test		45.4 ~ 90.8	76					
7	(Packaged)		90.8 ~ 454	61					
			Over 454	46					
		Dava D'			1				
		Drop Direct	ion :※1 corner / <b>3</b> edg	es / o sides each Ttime					

# **5. PRECAUTION RELATING PRODUCT HANDLING**

# **5.1 SAFETY**

- 5.1.1 If the LCD panel breaks , be careful not to get the liquid crystal to touch your skin.
- 5.1.2 If the liquid crystal touches your skin or clothes , please wash it off immediately by using soap and water.

# **5.2 HANDLING**

- 5.2.1 Avoid any strong mechanical shock which can break the glass.
- 5.2.2 Avoid static electricity which can damage the CMOS LSI—When working with the module , be sure to ground your body and any electrical equipment you may be using.
- 5.2.3 Do not remove the panel or frame from the module.
- 5.2.4 The polarizing plate of the display is very fragile. So , please handle it very carefully ,do not touch , push or rub the exposed polarizing with anything harder than an HB pencil lead (glass , tweezers , etc.)
- 5.2.5 Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.
- 5.2.6 Do not touch the display area with bare hands , this will stain the display area.
- 5.2.7 Do not use ketonics solvent & aromatic solvent. Use with a soft cloth soaked with a cleaning naphtha solvent.
- 5.2.8 To control temperature and time of soldering is  $320\pm10^{\circ}$ C and 3-5 sec.
- 5.2.9 To avoid liquid (include organic solvent) stained on LCM .

# **5.3 STORAGE**

- 5.3.1 Store the panel or module in a dark place where the temperature is  $25^{\circ}C \pm 5^{\circ}C$  and the humidity is below 65% RH.
- 5.3.2 Do not place the module near organics solvents or corrosive gases.
- 5.3.3 Do not crush , shake , or jolt the module.

## **5.4 TERMS OF WARRANTY**

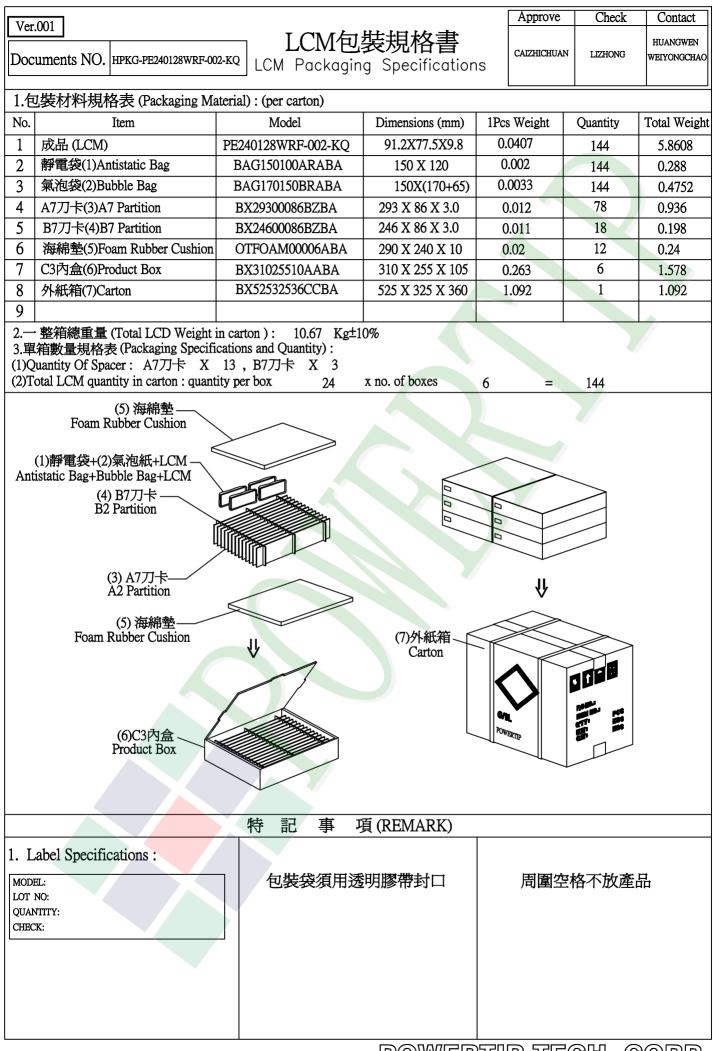
5.4.1 Applicable warrant period

The period is within thirteen months since the date of shipping out under normal using and storage conditions.

5.4.2 Unaccepted responsibility

This product has been manufactured to your company's specification as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we cannot take responsibility if the product is used in nuclear power control equipment, aerospace equipment, fire and security systems or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required.

0 REV	₽	ω		003	004	N	
NEW DRAWING	Modify the pin definition	Modify FPC	Modify FPC length			70  G  40  N = 2	A
REV BY	ition and storage temperature					74.5 68.0(V,A) 61.18(A,A) 72.0(LCD) 61.18(A,A) 72.0(LCD) 72.0128 DOTS 72.00 72.0128 DOTS 7.1000 7.100 7.100 7.1000 7.100 7.1000	Β
李小云 ( REVISER		_	i aliy yulixiali 李小示	_		TS TS TS TS TS TS TS TS TS TS TS TS TS T	C
08.8.03 DATE	08.8.13	08.8.22	08.10.27	09.10.22			
CD MODULE	ППСЕ:	HLMD-PE240128WRF-002-KQ	DRAWING NAME :	PE240128WRF-002-KQ	PART NO:	Stiffener 0.3±0.05 0.255 0.255 DOTS DETAL SCALE:20/1	C
		_		002-KQ		0.265- 0.285- 0.285- 0.5 <u>5</u> 0.5 <u>0</u> 0.5 <u>0</u> 0000000000000000000000000000000000	Г
Approve	Check		Design			±0.	
Ryan	Eddy	rang yunxan	Tang yunyian	Ĩ	久正光	B2.0 B2.0	т
Page			⊕ Д	Ξ	電股	1.4±0.1 2.8±0.1 4±0.3 4±0.3 5 5	
			- (3) Surface		位有	6.1±0.5 	G.
ity 63 ~		7		CORPORATIO	限公	Scale: 2/1 Scale:	
250 1000	~ 16 =	^	erance so Precision	N	, <u>⊐</u> []	<u> </u>	I



POWERTIP TECH. CORP.