

Product Specification

Part Name : OEL Display Module
Customer Part ID :
WiseChip Part ID : US-0011GMJAG01
Doc No. : SAS1-05013-A

Customer:

Approved by

CONFIDENTIAL

From: WiseChip Semiconductor Inc.

Approved by

WiseChip Semiconductor Inc.

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Notes:

1. Please contact WiseChip Semiconductor Inc. before assigning your product based on this module specification
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by WiseChip Semiconductor Inc. for any intellectual property claims or other problems that may result from application based on the module described herein.



Revised History

Part Number	Revision	Revision Content	Revised on
US-0011GMJAG01	A	New	December 22, 2016
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1. Basic Specifications

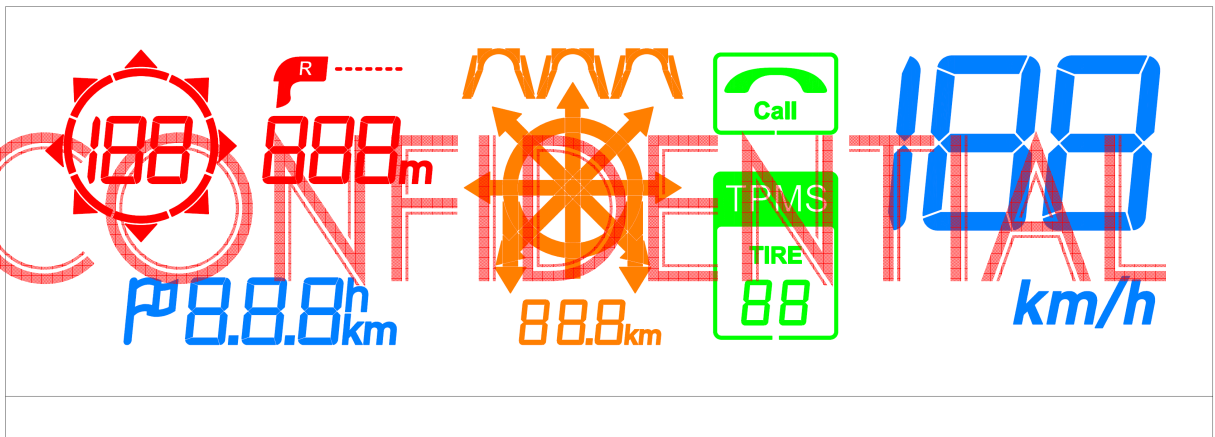
1.1 Display Specifications

- 1) Display Mode : Transparent Passive Matrix
- 2) Display Color : Area color (Red · Orange · Green · Light Blue)

1.2 Mechanical Specifications

- 1) Outline Drawing : According to the annexed outline drawing
- 2) Number of Segment : 231 Icons
- 3) Panel Size : 106.0 × 37.90 × 1.40 (mm)
- 4) Active Area : 100.0 × 27.30 (mm)
- 5) Weight : TBD ± 10%

1.3 Pixel Construction



1.5 Pin Definition

Pin Number	Symbol	I/O	Function
Power Supply			
1	VCC	P	Power Supply for OEL Panel This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and GND when the converter is used. It must be connected to external source.
3	IC3_VDDL	P	Power Supply for IC3 internal logic Circuit A stabilization capacitor should be connected between this pin and GND.
4	VDD	P	Power Supply for I/O and Analog It must be connected to external source.
5	IC1_VDDL	P	Power Supply for IC1 internal logic Circuit A stabilization capacitor should be connected between this pin and GND.
6	IC2_VDDL	P	Power Supply for IC2 internal logic Circuit A stabilization capacitor should be connected between this pin and GND.
7, 10	GND	P	Ground of Logic Circuit A reference for the logic pins and must be connected to external ground. DGND and LGND are connected outside the LSI.
Interface			
2	RST	I	Power Reset for Controller & Driver (Schmidt Input) This pin is reset signal input. When the pin is low, initialization of the chip is executed.
8	SCL	I	I²C Bus Clock Signal The transmission of information in the I ² C bus is following a clock signal. Each transmission of data bit is taken place during a single clock period of this pin.
9	SDA	I/O	I²C Bus Data Signal This pin acts as a communication channel between the transmitter and the receiver.

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2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V _{DD}	-0.3	3.6	V	1, 2
Supply Voltage for Display	V _{CC}	0	15	V	1, 2
Operating Temperature	T _{OP}	-30	70	°C	
Storage Temperature	T _{STG}	-40	85	°C	

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

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3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics		Symbol	Conditions	Min	Typ	Max	Unit
Brightness	Red	L_{br}	Note 4	600	800	-	cd/m ²
	Orange		Note 4	500	600	-	cd/m ²
	Green		Note 4	500	600	-	cd/m ²
	Light Blue		Note 4	600	800	-	cd/m ²
CIE	Red	CIE_x	CIE1391	0.60	0.64	0.68	-
		CIE_y		0.30	0.34	0.38	-
	Orange	CIE_x	CIE1391	0.52	0.56	0.60	-
		CIE_y		0.39	0.43	0.47	-
	Green	CIE_x	CIE1391	0.29	0.33	0.37	-
		CIE_y		0.58	0.62	0.66	-
	Light Blue	CIE_x	CIE1391	0.12	0.16	0.20	-
		CIE_y		0.22	0.26	0.30	-
Transmittance	T	Wavelength 550nm	40	50	-	%	
Dark Room Contrast	CR		5000	10000	-	-	
Viewing Angle			-	Free	-	degree	

* Optical measurement taken at $V_{DD} = 3V$, $V_{CC} = 12.0V$.
Software configuration follows Section 4.5 Initialization.

3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}		2	3.0	3.3	V
Supply Voltage for Display	V_{CC}	Note 4	11.5	12.0	12.5	V
High Level Input	V_{IH}	$I_{OUT} = 100\mu A$, 3.3MHz	$0.8 \times V_{DD}$	-	V_{DD}	V
Low Level Input	V_{IL}	$I_{OUT} = 100\mu A$, 3.3MHz	0	-	$0.2 \times V_{DD}$	V
Operating Current for V_{DD}	I_{DD}			1.5	2.0	mA
Operating Current for V_{CC}	I_{CC}			180	225	mA

Note 3: Brightness (L_{br}) and Supply Voltage for Display (V_{DISP}) are subject to the change of the panel characteristics and the customer's request.

Note 4: $V_{DD} = 3.0V$, $V_{CC} = 12.0V$, 100% Display Area Turn on.

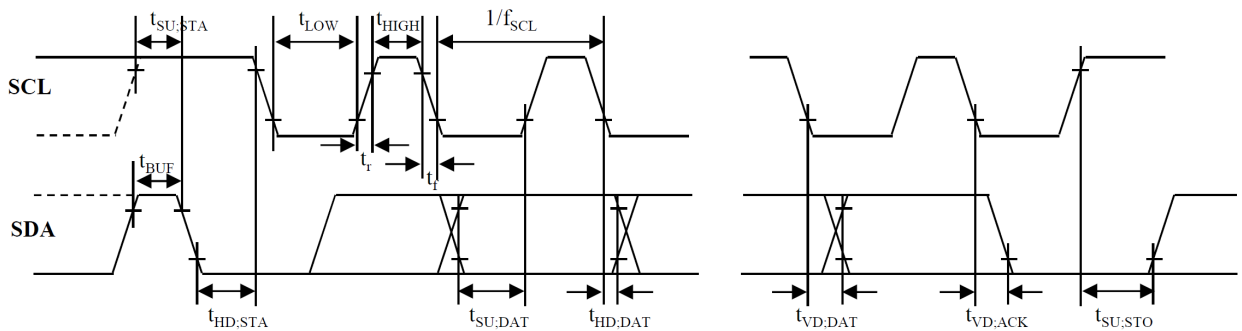
* Software configuration follows Section 4.5 Initialization.

3.3 AC Characteristics

 ($V_{DD} = 2.8V, V_{CC} = 12V, T_{OP} = -30\sim 70^{\circ}C$)

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	SCL clock Frequency	0	100	0	400	KHz
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	μs
$t_{HD;STA}$	Hold time (repeated) START condition	4.0	-	0.6	-	μs
$t_{SU;STA}$	Set-up time from a repeated START condition	4.7	-	0.6	-	μs
$t_{SU;STO}$	Set-up time for STOP condition	4.0	-	0.6	-	μs
$t_{SU;DAT}$	Data set-up time	250	-	100	-	ns
$t_{HD;DAT}$	Data Hold time	0	-	0	-	ns
$t_{VD;ACK}$	Data valid acknowledge time	0.3	3.45	0.1	0.9	μs
$t_{VD;DAT}$	Data valid time	300	-	50	-	ns
t_{LOW}	LOW Period of the SCL clock	4.7	-	1.3	-	μs
t_{HIGH}	HIGH Period of the SCL clock	4.0	-	0.6	-	μs
t_f	Fall time of both SDA and SCL clock	-	300	-	300	ns
t_r	Rise time of both SDA and SCL clock	-	1000	-	300	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	0	50	0	50	ns

- All the timing reference is 10% and 90% of V_{DD} .



4. Functional Specification

4.1 Commands

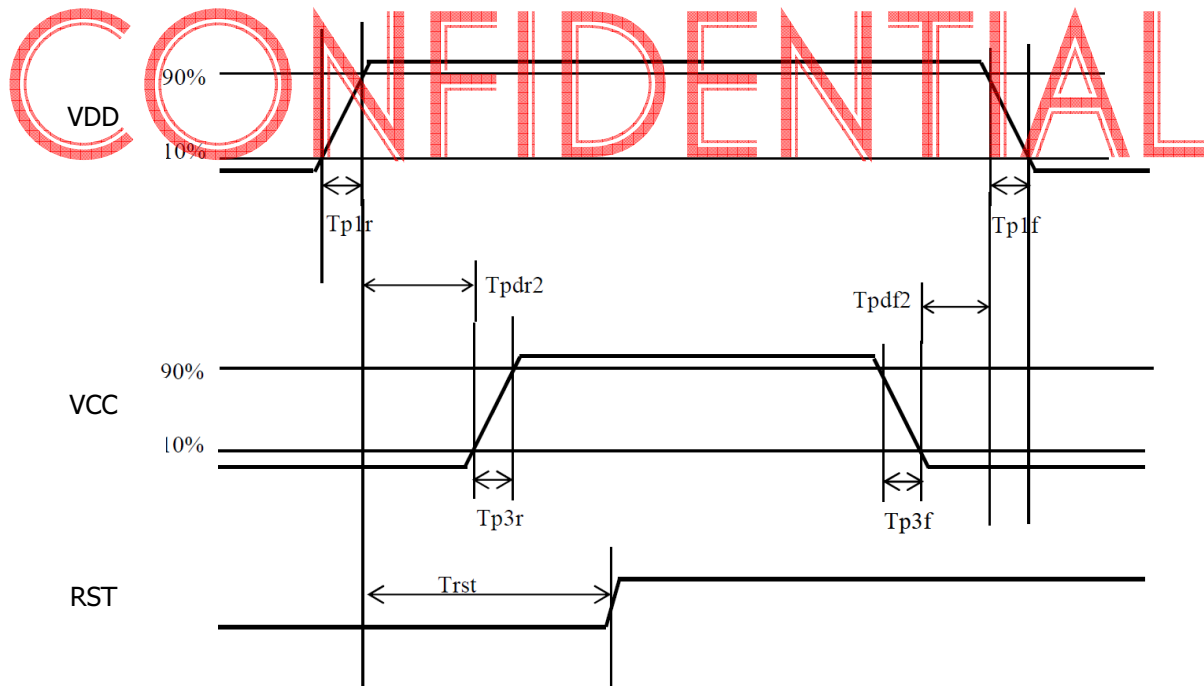
Refer to the Technical Manual for the LD7138

4.2 Power Sequence

($V_{DD} = 2.8V, V_{CC} = 12V, T_a = 25^\circ C$)

Parameter	Symbol	Related Pin	Standard Mode			Unit
			Min.	Typ.	Max.	
VDD on Slope VDD off Slope	T_{p1r} T_{p1f}	VDD	0.2	1	5	ms/V
VCC On Slope VCC off Slope	T_{p3r} T_{p3f}	VCC	0.2	1	5	ms/V
From VDD to VCC delay	T_{pdr2}	VDD, VCC	2	-	-	ms
From VCC to VDD delay	T_{pdf2}	VDD, VCC	2	-	-	ms
From VDD to H/W Reset Release	T_{rst}	VDD, RST	30	-	-	ms

- All the timing reference is 10% and 90% of V_{DD} .

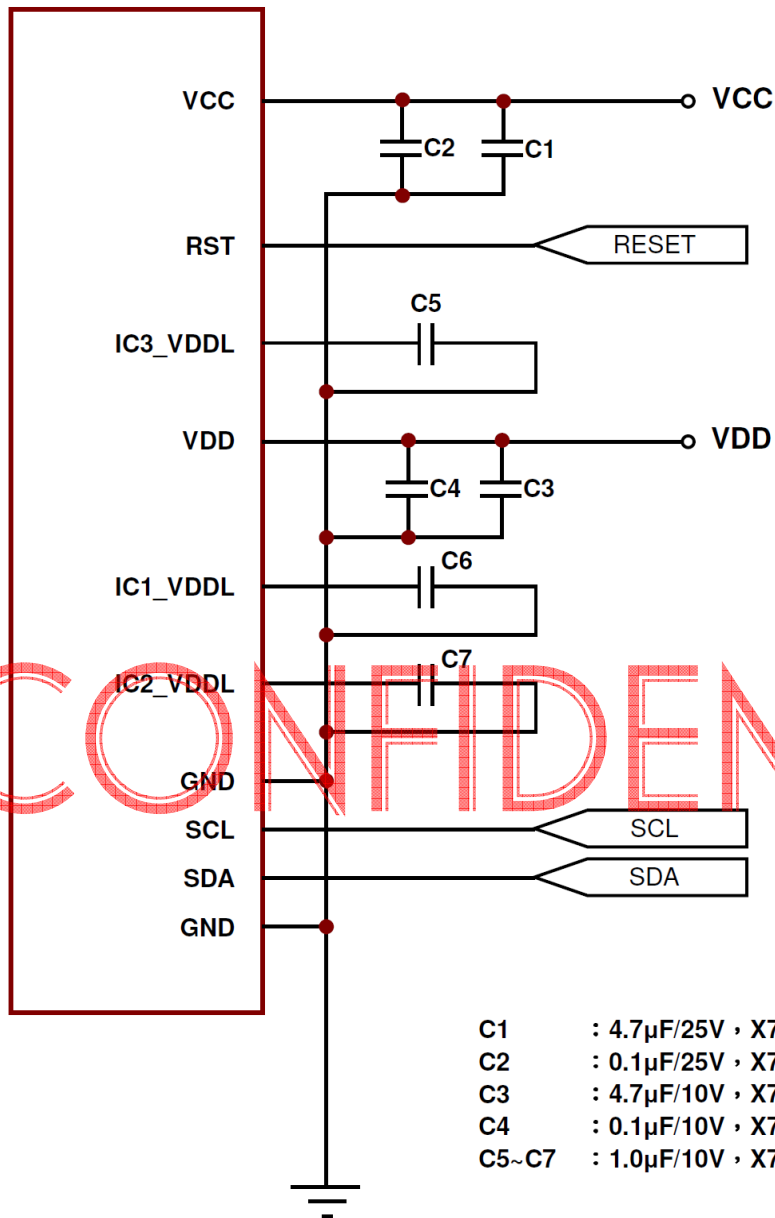


4.3 Reset Circuit

When RST input was pulled low over 1000ns, the chip is initialized with the following status:

1. Display OFF
2. Clock Oscillation Halt
3. Register writing is impossible (IF operation halt)
4. Internal register (Except the Graphic Data) value is initialized.

4.4 Application Circuit





4.5 Actual Application Example

Command usage and explanation of an actual example

<Initialization>

Please contact us for further information

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If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

5. Reliability

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-30°C, 240 hrs	
High Temperature Storage	85°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ↔ 85°C, 24 cycles 60 mins dwell	

* No moisture condensation is observed during tests.

5.2 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

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6. Outgoing Quality Control Specifications

6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

- Temperature: $23 \pm 5^{\circ}\text{C}$
- Humidity: $55 \pm 15\% \text{ RH}$
- Fluorescent Lamp: 30W
- Distance between the Panel & Lamp: $\geq 50\text{cm}$
- Distance between the Panel & Eyes of the Inspector: $\geq 30\text{cm}$
- Finger glove (or finger cover) must be worn by the inspector.
- Inspection table or jig must be anti-electrostatic.

6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

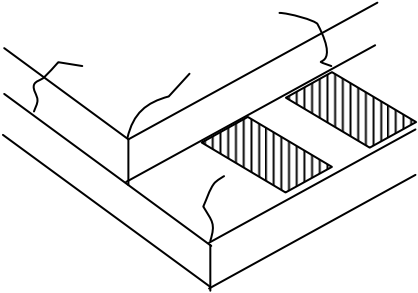

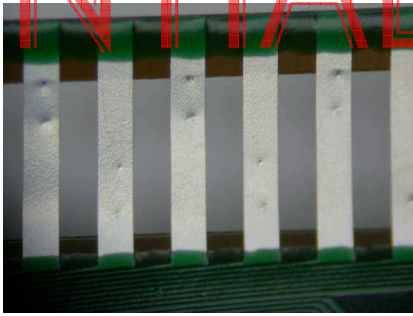
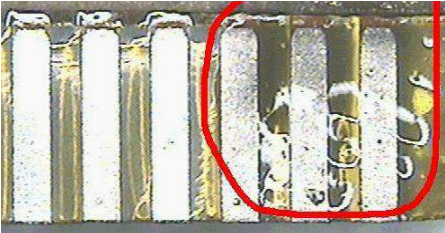
6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.5	Defects in Cosmetic Check (Display Off)

6.3.1 Cosmetic Check (Display Off) in Non-Active Area

Check Item	Classification	Criteria
Panel General Chipping	Minor	<p>$X > 6 \text{ mm}$ (Along with Edge) $Y > 1 \text{ mm}$ (Perpendicular to edge)</p>

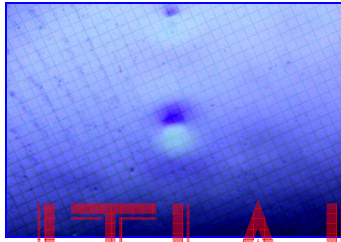
6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	<p>Any crack is not allowable.</p> 
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Prober Mark	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

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6.3.2 Cosmetic Check (Display Off) in Active Area

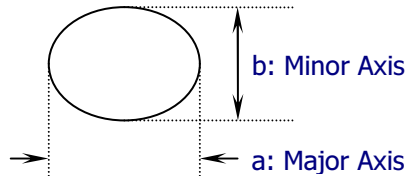
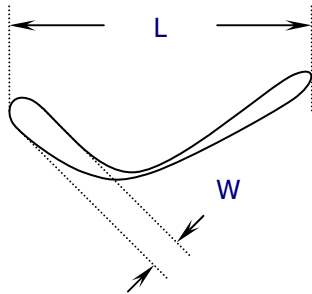
It is recommended to execute in clear room environment (class 10k) if actual in necessary.

Check Item	Classification	Criteria
Any Dirt & Scratch on Panel's Protective Film	Acceptable	Ignore for not Affect the Panel
Scratches, Fiber, Line-Shape Defect (On Panel)	Minor	$W \leq 0.1$ Ignore $W > 0.1$ $L \leq 3$ $n \leq 2$ $L > 3$ $n = 0$
Dirt, Black Spot, Foreign Material, (On Panel)	Minor	$\Phi \leq 0.1$ Ignore $0.1 < \Phi \leq 0.3$ $n \leq 2$ $0.3 < \Phi$ $n = 0$
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	$\Phi \leq 0.5$ → Ignore if no Influence on Display $0.5 < \Phi$ $n = 0$ 
Fingerprint, Flow Mark (On Panel)	Minor	Not Allowable

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* Protective film should not be tear off when cosmetic check.

** Definition of W & L & Φ (Unit: mm): $\Phi = (a + b) / 2$



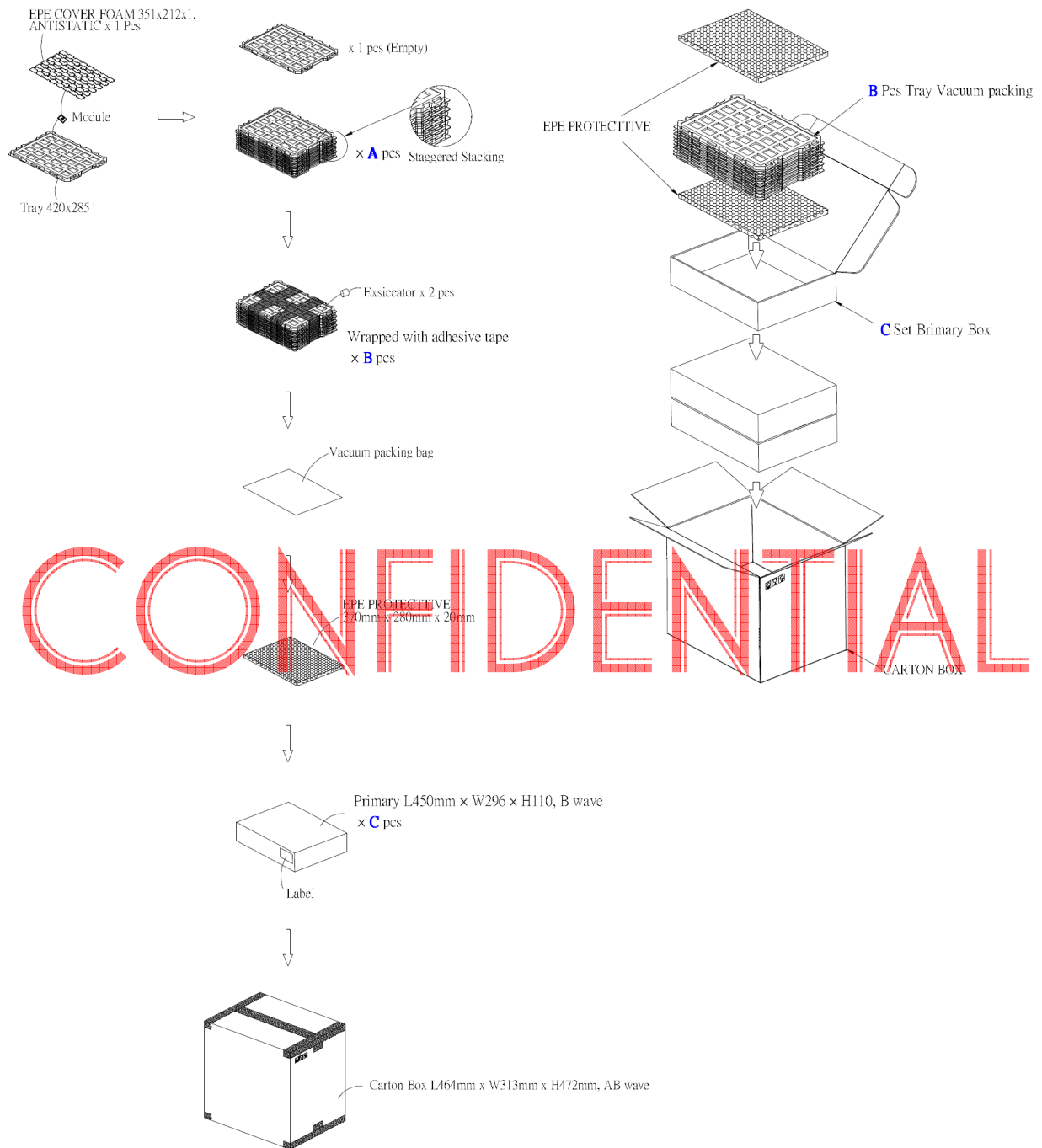


6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	Not Allowable
Missing Segment	Major	
Wrong Display	Major	

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7. Package Specifications



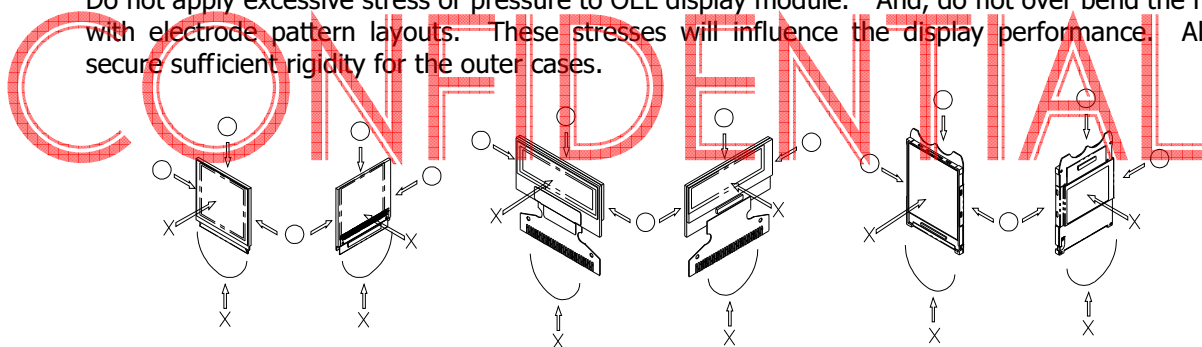
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Item	Quantity	
Module	TBD	per Primary Box
Holding Trays (A)	TBD	per Primary Box
Total Trays (B)	TBD	per Primary Box (Including 1 Empty Tray)
Primary Box (C)	1~4	per Carton (4 as Major / Maximum)

8. Precautions When Using These OEL Display Modules

8.1 Handling Precautions

- 1) Since the display panel is being made of glass, do not apply mechanical impacts such as dropping from a high position.
- 2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
- 3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
- 4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
- 5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
 - * Scotch Mending Tape No. 810 or an equivalent
 Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy. Also, pay attention that the following liquid and solvent may spoil the polarizer:
 - * Water
 - * Ketone
 - * Aromatic Solvents
- 6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



- 7) Do not apply stress to the driver IC and the surrounding molded sections.
- 8) Do not disassemble nor modify the OEL display module.
- 9) Do not apply input signals while the logic power is off.
- 10) Pay sufficient attention to the working environments when handling OEL display modules to prevent occurrence of element breakage accidents by static electricity.
 - * Be sure to make human body grounding when handling OEL display modules.
 - * Be sure to ground tools to use or assembly such as soldering irons.
 - * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
 - * Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.
- 11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
- 12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

8.2 Storage Precautions

- 1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high

humidity environment or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from WiseChip Semiconductor Inc.)

At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.

- 2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

8.3 Designing Precautions

- 1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
- 2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the V_{IL} and V_{IH} specifications and, at the same time, to make the signal line cable as short as possible.
- 3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (V_{DD}). (Recommend value: 0.5A)
- 4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
- 5) As for EMI, take necessary measures on the equipment side basically.
- 6) When fastening the OEL display module, fasten the external plastic housing section.
- 7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
- 8) The electric potential to be connected to the rear face of the IC chip should be as follows: ML9380A
 - * Connection (contact) to any other potential than the above may lead to rupture of the IC.

8.4 Precautions when disposing of the OEL display modules

- 1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

8.5 Other Precautions

- 1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur. Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
- 2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
 - * Pins and electrodes
 - * Pattern layouts such as the TCP & FPC
- 3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
 - * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
 - * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
- 4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
- 5) We recommend you to construct its software to make periodical refreshment of the operation



statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

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Warranty:

The warranty period shall last twelve (12) months from the date of delivery. Buyer shall be completed to assemble all the processes within the effective twelve (12) months. WiseChip Semiconductor Inc. shall be liable for replacing any products which contain defective material or process which do not conform to the product specification, applicable drawings and specifications during the warranty period. All products must be preserved, handled and appearance to permit efficient handling during warranty period. The warranty coverage would be exclusive while the returned goods are out of the terms above.

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