Product Specification

Part Name: OEL Display Module
Part ID: UG-6028GDEAF01
Doc No.: SAS1-I003-B

Customer:
Approved by

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From: Univision Technology Inc.
Approved by

Univision Technology Inc.
8, Kebei RD 2, Science Park, Chu-Nan, Taiwan 350, R.O.C.

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Revised History

Part Number	Revision	Revision Content	Revised on
UG-6028GDEAF01	A	New	April 11, 2006
UG-6028GDEAF01	B	Page 1 *Section 1.2 3)* Modify Panel Thickness 1.70 ➔ 1.60 Page 2 *Section 1.4* Update Mechanical Drawing from the Applicable COF Number & Pin Definition Modification Page 3~4 *Section 1.5* Update Pin Definition Description Page 5 *Section 1.6* Modify Application Circuit Page 6 *Section 2* Update Absolute Maximum Ratings Page 7 *Section 3.1 & 3.2* Reset Optics Characteristics to Section 3.1 Modify C.I.E. White (0.29±0.04, 0.33±0.04)➔(0.30±0.04, 0.33±0.04) Red (0.61±0.04, 0.36±0.04)➔(0.64±0.04, 0.34±0.04) Green (0.30±0.04, 0.64±0.04)➔(0.31±0.04, 0.62±0.04) Blue (0.14±0.04, 0.19±0.04)➔(0.14±0.04, 0.16±0.04) Modify Dark Room Contrast (Typ) >1000:1 ➔ >2000:1 Integrate DC Characteristics with General Electrical Characteristics Page 8~11 *Section 3.3* Update AC Characteristics Page 12 *Section 4.2.1* Update Power up Sequence Page 13 *Section 4.4* Update Initialization Page 20 *Section 7* Update Package Specifications	June 9, 2008

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1. Basic Specifications

1.1 Display Specifications

1) Display Mode: Passive Matrix
2) Display Color: 262,144 Colors (Maximum)
3) Drive Duty: 1/128 Duty

1.2 Mechanical Specifications

1) Outline Drawing: According to the annexed outline drawing
2) Number of Pixels: 160 (RGB) × 128
3) Panel Size: 35.80 × 30.80 × 1.60 (mm)
4) Active Area: 28.78 × 23.024 (mm)
5) Pixel Pitch: 0.06 × 0.18 (mm)
6) Pixel Size: 0.04 × 0.164 (mm)
7) Weight: 3.6 (g)

1.3 Active Area & Pixel Construction

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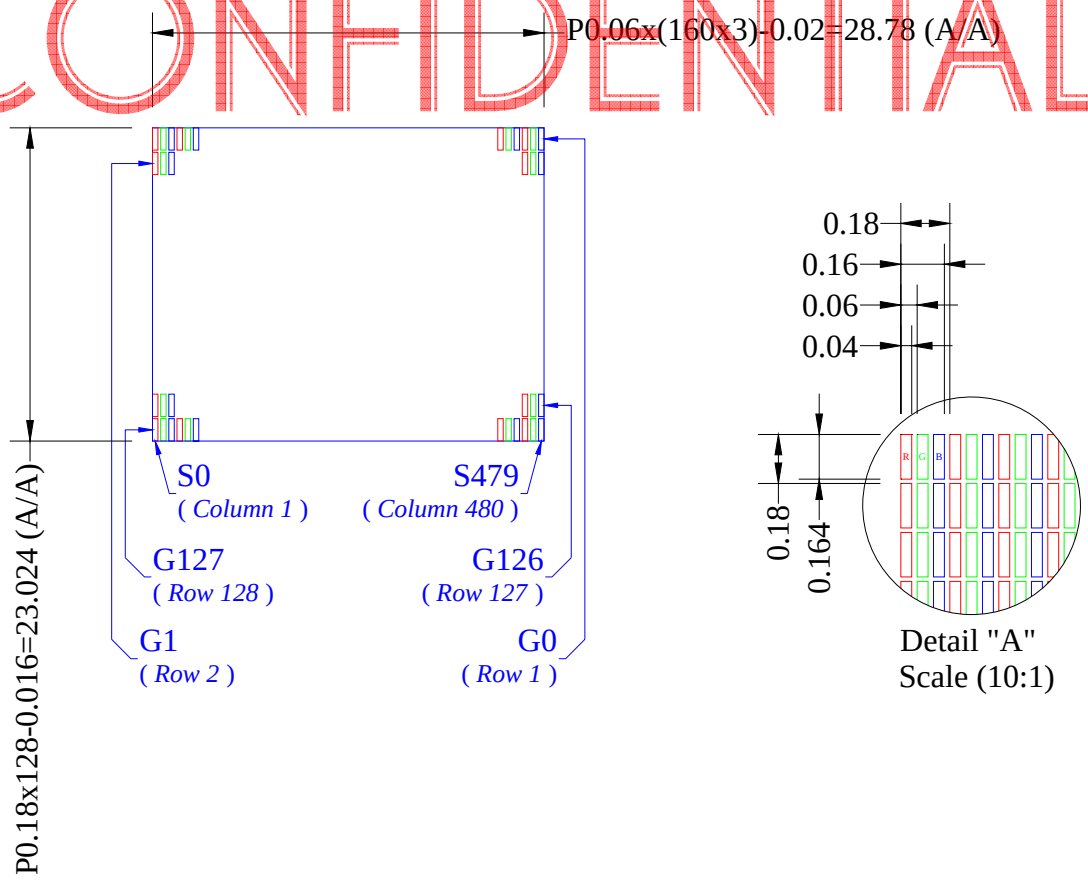
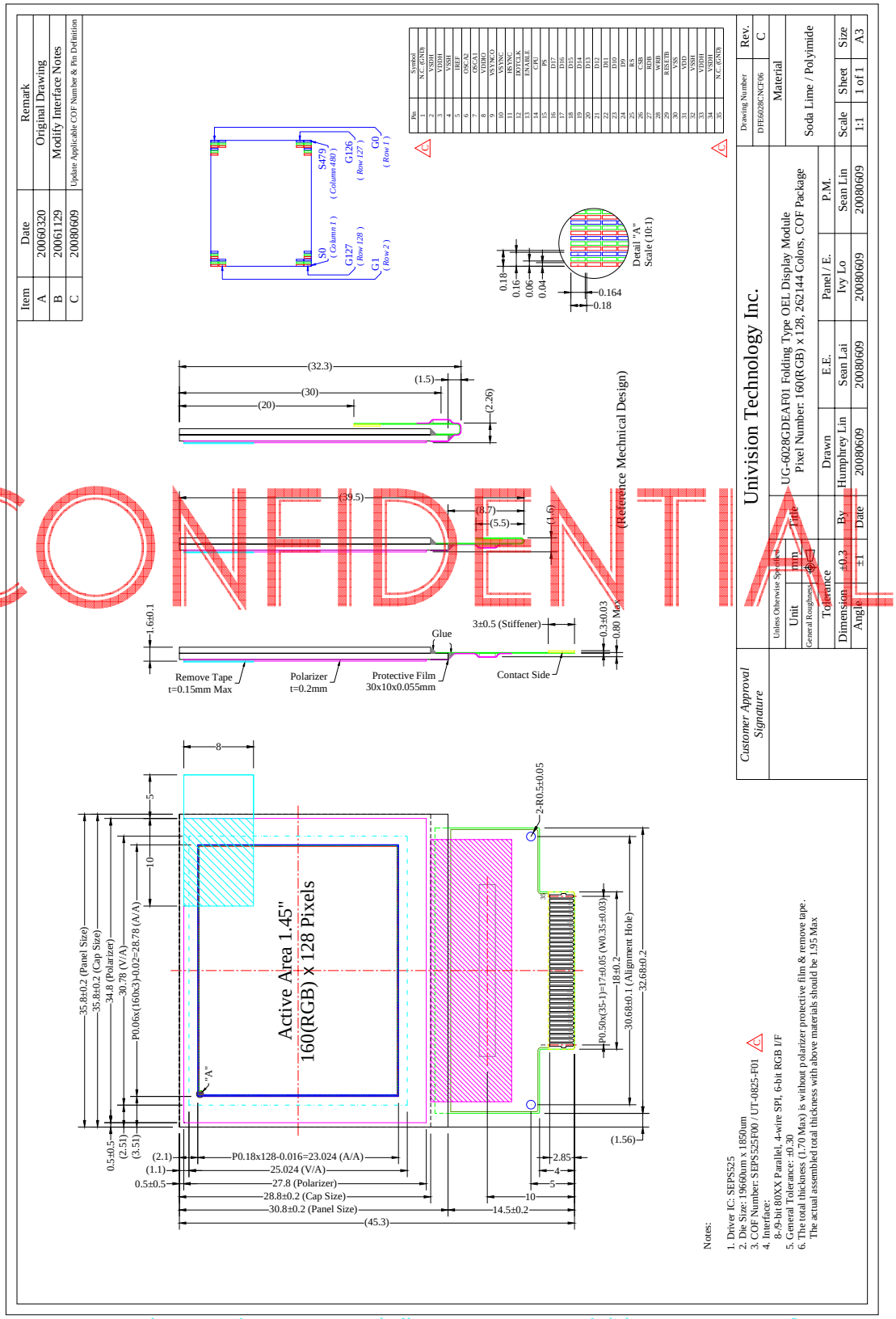


1.4 Mechanical Drawing



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1.5 Pin Definition

Pin Number	Symbol	Type	Function
Power Supply			
31	VDD.	P	*Power Supply for Logic Circuit* This is a voltage supply pin. It must be connected to external source.
8	VDDIO	P	*Power Supply for Interface Logic Level* This is a voltage supply pin. It should be match with MCU interface voltage level. It must always be equal or lower than VDD.
30	VSS	P	*Ground of Logic Circuit* A reference for the logic pins. It must be connected to external ground.
3, 33	VDDH	P	*Power Supply for OEL Panel* This is the most positive voltage supply pin of the chip. It must be connected to external source.
2, 34 4, 32	VSDH VSSH	P	*Ground of OEL Panel* These are the ground pins for analog circuits. It must be connected to external ground. VSDH: Segment (Data Driver) VSSH: Common (Scan Driver)
Driver			
5	IREF	I/O	*Current Reference for Brightness Adjustment* This pin is segment (data) current reference pin. A 68kΩ resistor should be connected between this pin and VSS.
7 6	OSCA1 OSCA2	I O	*Fine Adjustment for Oscillation* The frequency is controlled by external 10kΩ resistor between OSCA1 and OSCA2. The oscillator signal is used for system clock generation. When the external clock mode is selected, OSCA1 is used external clock input.
RGB Interface			
9	VSYNCO	O	*Vertical Synchronization Triggering Signal*
10	VSYNC	I	*Vertical Synchronization Input*
11	HSYNC	I	*Horizontal Synchronization Input*
12	DOTCLK	I	*Dot Clock Input*
13	ENABLE	I	*Video Enable Input*
MCU Interface			
14	CPU	I	*Select the CPU Type* Low: 80XX-Series MCU High: 68XX-Series MCU.
15	PS	I	*Select Parallel/Serial Interface Type* Low: Serial Interface High: Parallel Interface
29	RESETB	I	*Power Reset for Controller and Driver* This pin is reset signal input. When the pin is low, initialization of the chip is executed.

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1.5 Pin Definition (Continued)

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>Type</th><th>Function</th></tr>
<tr><td colspan="4">MCU Interface (Continued)</td></tr>
<tr><td>26</td><td>CSB</td><td>I</td><td>Chip Select
Low: SEPS525 is selected and can be accessed.
High: SEPS525 is not selected and cannot be accessed.</td></tr>
<tr><td>25</td><td>RS</td><td>I</td><td>Data/Command Control
Low: Command
High: Parameter/Data</td></tr>
<tr><td>27</td><td>RDB</td><td>I</td><td>Read or Read/Write Enable
68XX Parallel Interface: Bus Enabled Strobe (Active High)
80XX Parallel Interface: Read Strobe Signal (Active Low)
While using SPI, it must be connected to VDD or VSS.</td></tr>
<tr><td>28</td><td>WRB</td><td>I</td><td>Write or Read/Write Select
68XX Parallel Interface: Read (Low)/Write (High) Select
80XX Parallel Interface: Write Strobe Signal (Active Low)
While using SPI, it must be connected to VDD or VSS.</td></tr>
<tr><td>16~24</td><td>D17~D9</td><td>I/O</td><td>Host Data Input/Output Bus
These pins are 9-bit bi-directional data bus to be connected to the microprocessor’s data bus.
<table>
<tr><th>PS</th><th>Description</th></tr>
<tr><td>0</td><td>D[17]/SCL: Synchronous Clock Input
D[16]/SDI: Serial Data Input
D[15]/SDO: Serial Data Output</td></tr>
<tr><td>1</td><td>9-bit Bus: D[17:9]
8-bit Bus: D[17:10]</td></tr>
</table>
While using SPI, the unused pins must be connected to VSS.</td></tr>
<tr><td colspan="4">Reserve</td></tr>
<tr><td>1, 35</td><td>N.C. (GND)</td><td>-</td><td>Reserved Pin (Supporting Pin)
The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.</td></tr>
</table>

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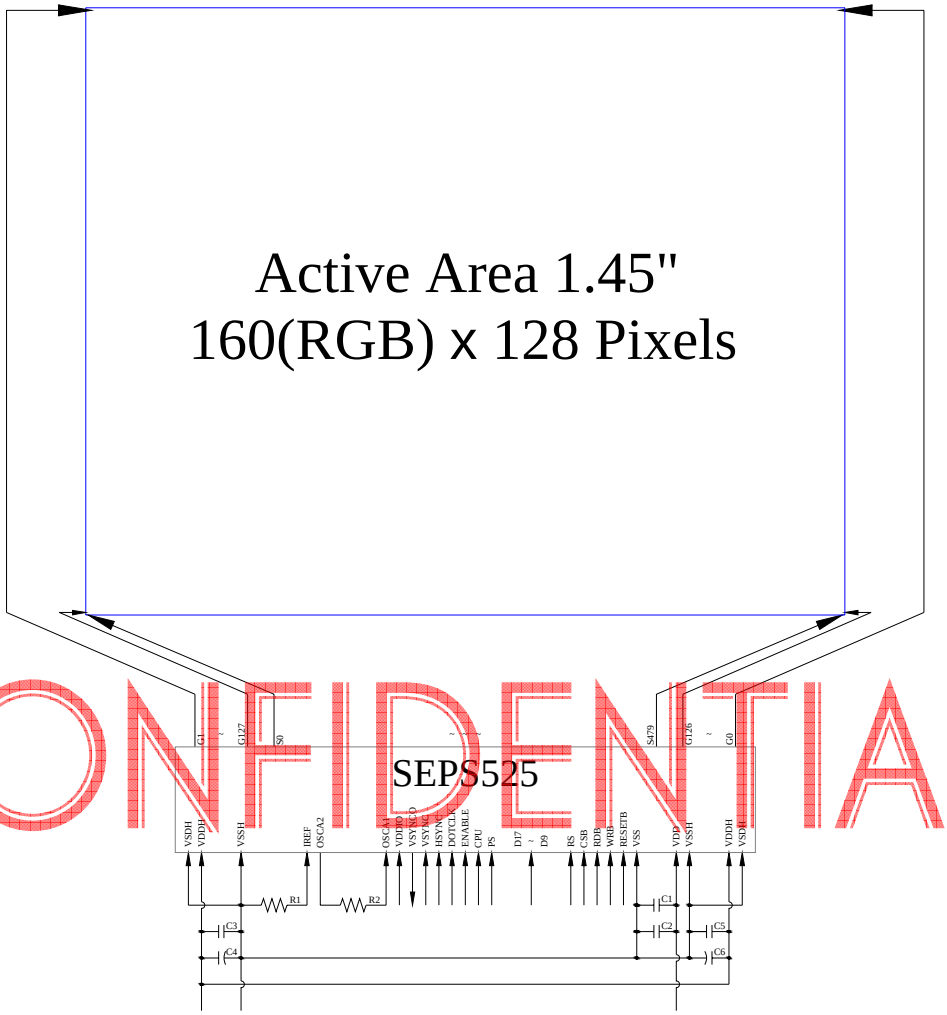
1.6 Block Diagram



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MCU Interface Selection: CPU, PS
Pins connected to MCU interface: D17~D9, RS, CSB, RDB, WRB, and RESETB
Pins connected to RGB interface: D17~D12, VSYNC, HSYNC, DOTCLK, and ENABLE

C1, C3, C5: 0.1μF
C2: 4.7μF
C4, C6: 4.7μF / 25V Tantalum Capacitor
R1: 68kΩ
R2: 10kΩ

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	4	V	1, 2
Supply Voltage for I/O Pins	V_{DDIO}	-0.3	4	V	1, 2
Supply Voltage for Display	V_{DDH}	-0.3	16	V	1, 2
Operating Temperature	T_{OP}	-30	70	°C	-
Storage Temperature	T_{STG}	-40	80	°C	-

Note 1: All the above voltages are on the basis of "VSS = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

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3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness (White)	L_{br}	With Polarizer (Note 3)	75	100	-	cd/m^2
C.I.E. (White)	(x) (y)	With Polarizer	0.26 0.29	0.30 0.33	0.34 0.37	
C.I.E. (Red)	(x) (y)	With Polarizer	0.60 0.30	0.64 0.34	0.68 0.38	
C.I.E. (Green)	(x) (y)	With Polarizer	0.27 0.58	0.31 0.62	0.35 0.66	
C.I.E. (Blue)	(x) (y)	With Polarizer	0.10 0.12	0.14 0.16	0.18 0.20	
Dark Room Contrast	CR		-	>2000:1	-	
View Angle			>160	-	-	degree

* Optical measurement taken at V_{DD} = 2.8V, V_{DDH} = 13V.
Software configuration follows Section 4.4 Initialization.

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3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}		2.6	2.8	3.3	V
Supply Voltage for I/O Pins	V_{DDIO}		1.6	2.8	3.3	V
Supply Voltage for Display	V_{DDH}	Note 3	12.5	13	13.5	V
High Level Input	V_{IH}		0.8×V_{DD}	-	V_{DD}	V
Low Level Input	V_{IL}		0	-	0.4	V
High Level Output	V_{OH1}	I_{OH} = -0.4mA	V_{DD}-0.4	-		V
	V_{OH2}	I_{OH} = -0.4mA				
Low Level Output	V_{OL1}	I_{OL} = -0.1mA		-	0.4	V
	V_{OL2}	I_{OL} = -0.1mA				
Operating Current for V_{DD}	I_{DD}	Note 4	-	2.5	3.5	µA
		Note 5	-	2.5	3.5	µA
Operating Current for V_{DDH}	I_{DDH}	Note 4	-	16	19	mA
		Note 5	-	27	32	mA

Note 3: Brightness (L_{br}) and Supply Voltage for Display (V_{DDH}) are subject to the change of the panel characteristics and the customer's request.
Note 4: V_{DD} = 2.8V, V_{DDH} = 13V, 50% Display Area Turn on.
Note 5: V_{DD} = 2.8V, V_{DDH} = 13V, 100% Display Area Turn on.

* Software configuration follows Section 4.4 Initialization.

3.3 AC Characteristics

3.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

(V_{DD} = 2.8V, T_a = 25°C)

Symbol	Description		Min	Max	Unit	Port
t_{AH6}	Address Setup Timing	(Read)	10	-	ns	CSB RS
		(Write)	10	-	ns	
t_{AS6}	Address Hold Timing	(Read)	5	-	ns	
		(Write)	5	-	ns	
t_{CYC6}	System Cycle Timing		200	-	ns	E
t_{ELR6}	Read "L" Pulse Width		90	-	ns	
t_{EHR6}	Read "H" Pulse Width		90	-	ns	
t_{CYC6}	System Cycle Timing		100	-	ns	
t_{ELW6}	Write "L" Pulse Width		45	-	ns	
t_{EHW6}	Write "H" Pulse Width		45	-	ns	
t_{RDD6}	Read Data Output Delay Time	* CL = 15pF	0	70	ns	D[17:9]
t_{RDH6}	Data Hold Timing		0	70	ns	
t_{DS6}	Data Setup Timing		40	-	ns	
t_{DH6}	Data Hold Timing		10	-	ns	

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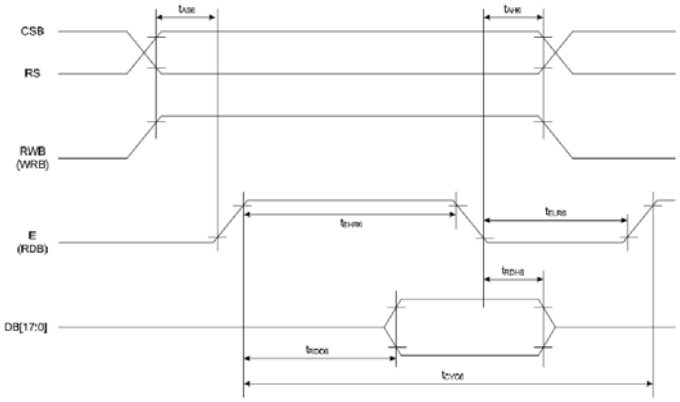
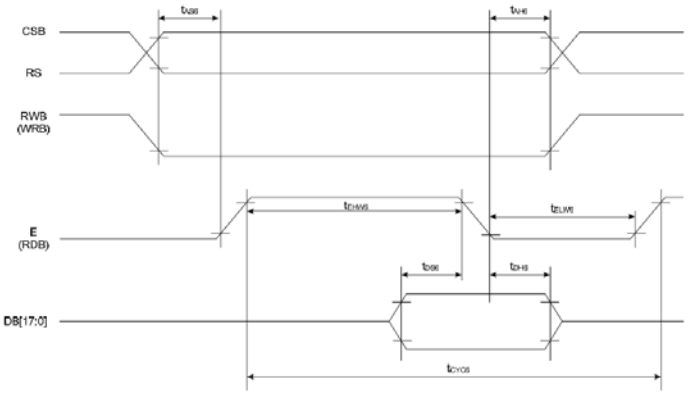
* All the timing reference is 10% and 90% of V_{DD}.



(Read Timing)



(Write Timing)

3.3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

(V_{DD} = 2.8V, T_a = 25°C)

Symbol	Description	Min	Max	Unit	Port
t_{AS8}	Address Setup Timing	5	-	ns	CSB RS
t_{AH8}	Address Hold Timing	5	-	ns	
t_{CYC8}	System Cycle Timing	200	-	ns	RDB
t_{RDLR8}	Read "L" Pulse Width	90	-	ns	
t_{RDHR8}	Read "H" Pulse Width	90	-	ns	
t_{CYC8}	System Cycle Timing	100	-	ns	WRB
t_{WRLW8}	Write "L" Pulse Width	45	-	ns	
t_{WRHW8}	Write "H" Pulse Width	45	-	ns	
t_{RDD8}	Read Data Output Delay Time * CL = 15pF	-	60	ns	D[17:9]
t_{RDH8}	Data Hold Timing	0	60	ns	
t_{DS8}	Data Setup Timing	30	-	ns	
t_{DH8}	Data Hold Timing	10	-	ns	

* All the timing reference is 10% and 90% of V_{DD}.

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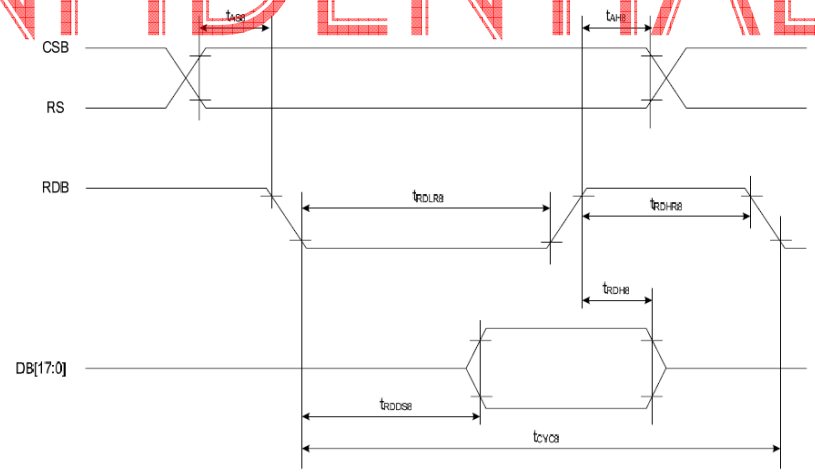
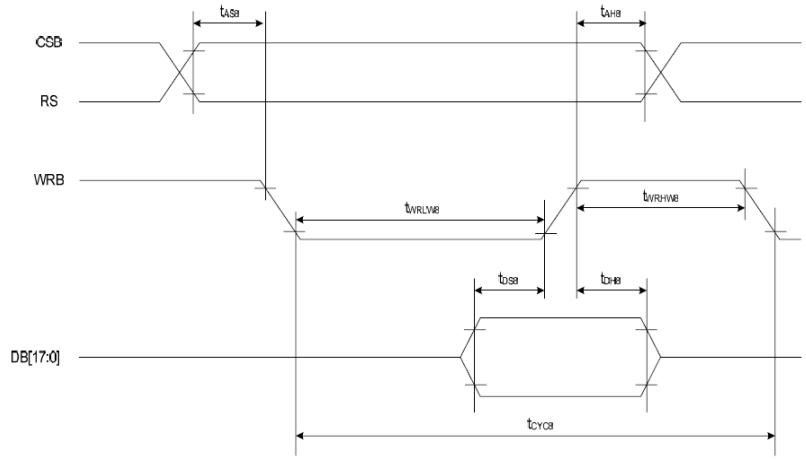


(*Read Timing*)



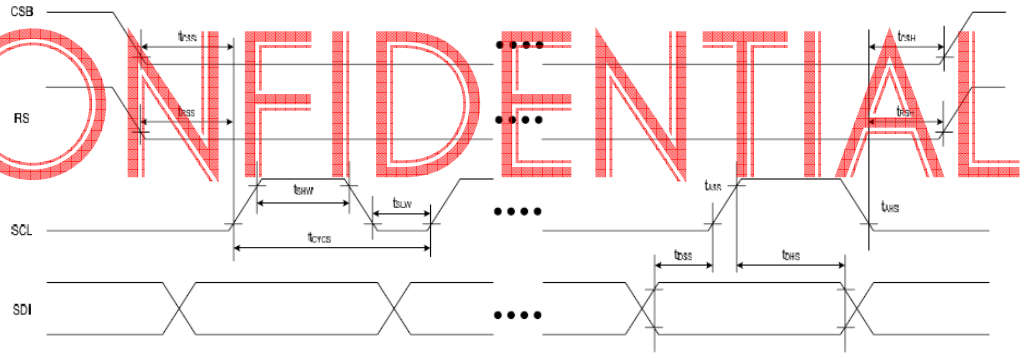
(*Write Timing*)

3.3.3 Serial Interface Timing Characteristics:

(V_{DD} = 2.8V, T_a = 25°C)

Symbol	Item	Min	Max	Unit	Port
t_{CYCS}	Serial Clock Cycle	60	-	ns	SCL
t_{SHW}	SCL "L" Pulse Width	25	-	ns	
t_{SLW}	SCL "H" Pulse Width	25	-	ns	
t_{DSS}	Data Setup Timing	25	-	ns	SDI
t_{DHS}	Data Hold Timing	25	-	ns	
t_{CSS}	CSB-SCL Timing	25	-	ns	CSB
t_{CSH}	CSB-Hold Timing	25	-	ns	
t_{RSS}	RS-SCL Timing	25	-	ns	RS
t_{RSH}	RS-Hold Timing	25	-	ns	

* All the timing reference is 10% and 90% of V_{DD}.



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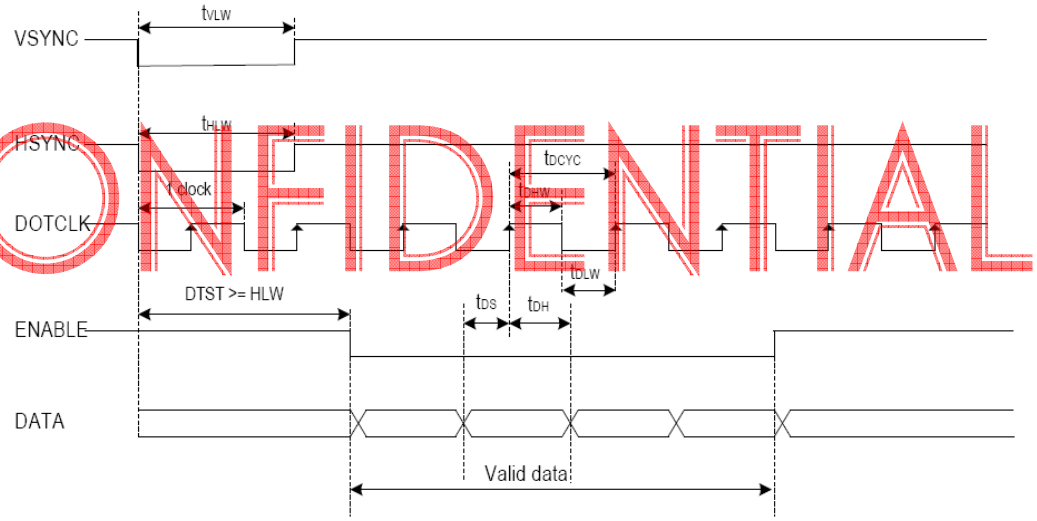
3.3.4 RGB Interface Timing Characteristics:

(V_{DD} = 2.8V, T_a = 25°C)

Symbol	Item	Min	Max	Unit	Port
t_{DCYC}	Dot Clock Cycle	100	-	ns	DOTCLK
t_{DLW}	Dot "L" Pulse Width	50	-	ns	
t_{DHW}	Dot "H" Pulse Width	50	-	ns	
t_{DS}	Data Setup Timing	5	-	ns	D[17:12]
t_{DH}	Data Hold Timing	5	-	ns	
t_{VLW}	Vsync Pulse Width	1	-	DOTCLK	VSYNC
t_{HLW}	Hsync Pulse Width	1	-	DOTCLK	HSYNC

* All the timing reference is 10% and 90% of V_{DD}.



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DTST: Setup Time for Data Transmission

* VSYNC, HSYNC, ENABLE, and D[17:12] should be transmitted by 3 clocks for one pixel (RGB).

4. Functional Specification

4.1. Commands

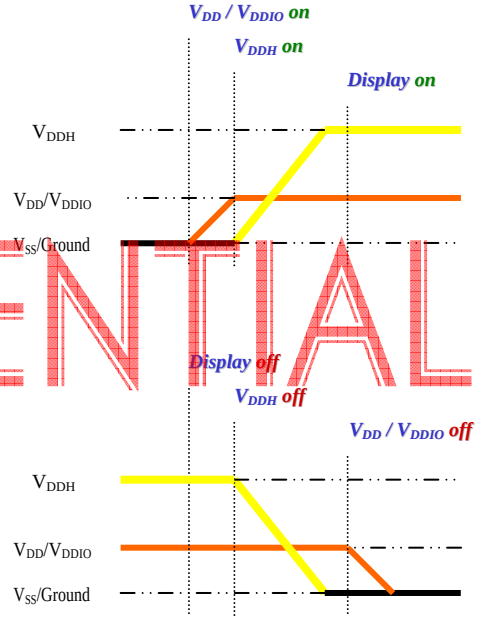
Refer to the Technical Manual for the SEPS525

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

4.2.1 Power up Sequence:

1. Power up V_{DD} / V_{DDIO}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{DDH}
6. Delay 100ms
   (when V_{DDH} is stable)
7. Send Display on command



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4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{DDH}
3. Delay 100ms
   (when V_{DDH} is reach 0 and panel is completely discharges)
4. Power down V_{DD} / V_{DDIO}

4.3 Reset Circuit

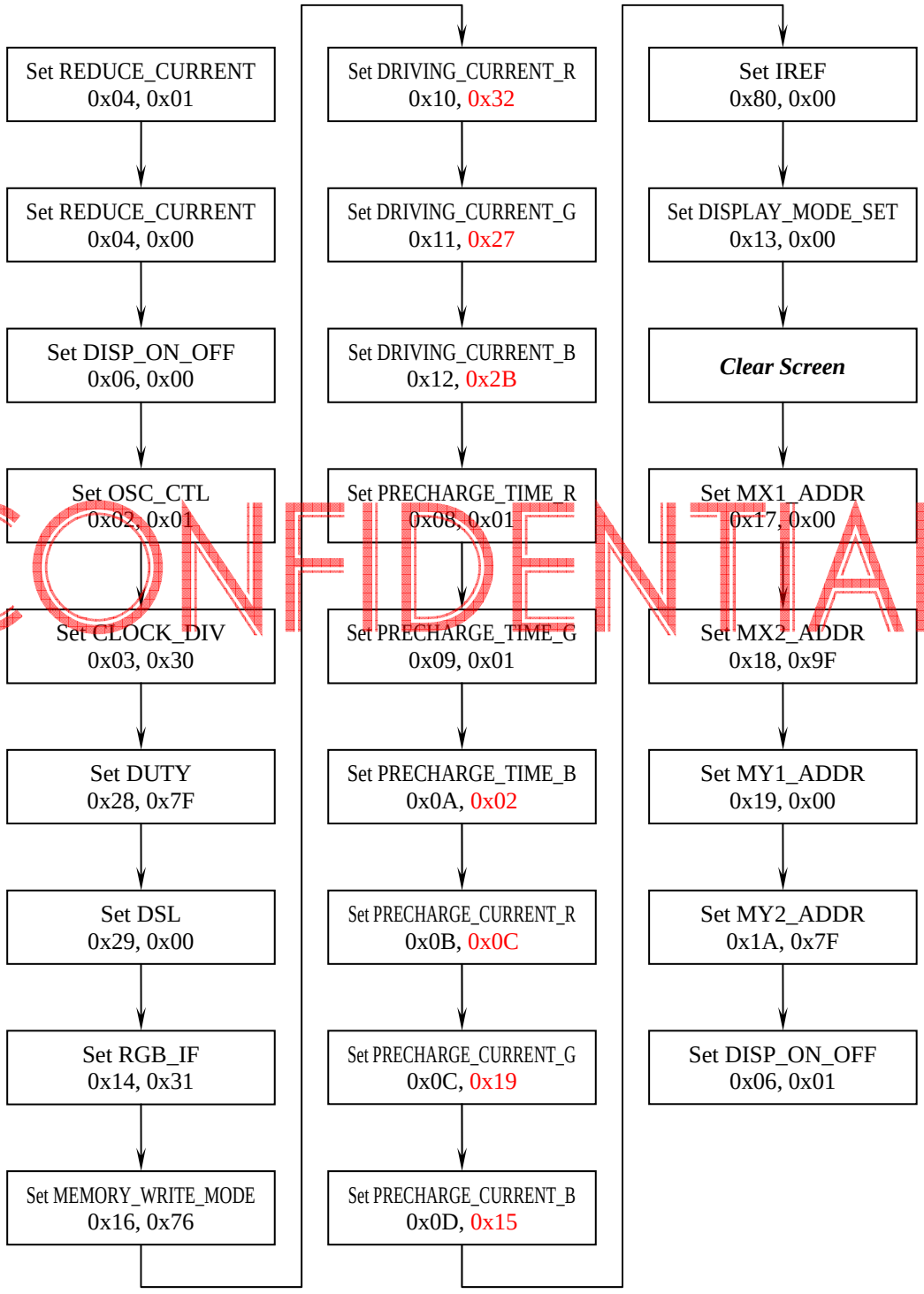
When RESETB input is low, the chip is initialized with the following status:

1. Frame Frequency: 90Hz
2. Oscillation: Internal Oscillator On
3. DDRAM Write Horizontal Address: MX1 = 0x00, MX2 = 0x9F
4. DDRAM Write Vertical Address: MY1 = 0x00, MY2 = 0x7F
5. Display Data RAM Write: HC = 1, VC = 1, HV = 0
6. RGB Data Swap: Off
7. Row Scan Shift Direction: G0, G1, … , G126, G127
8. Column Data Shift Direction: S0, S1, … , S478, S479
9. Display On/Off: Off
10. Panel Display Size: FX1 = 0x00, FX2 = 0x9F, FY1 = 0x00, FY1 = 0x7F
11. Display Data RAM Read Column/Row Address: FAC = 0x00, FAR = 0x00
12. Precharge Time (R/G/B): 0 Clock
13. Precharge Current (R/G/B): 0µA
14. Driving Current (R/G/B): 0µA

4.4 Actual Application Example

Command usage and explanation of an actual example

<Initialization>



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If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

5. Reliability

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-30°C, 240 hrs	
High Temperature Storage	80°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

5.2 Lifetime

End of lifetime is specified as 50% of initial brightness.

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Parameter	Min	Max	Unit	Condition	Notes
Operating Life Time	10,000	-	hr	100 cd/m^2, 50% Checkerboard	6
Storage Life Time	20,000	-	hr	T_a = 25°C, 50% RH	-

Note 6: The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

5.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.